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Introduction to Compact Models

1.1 Compact Models for Circuit Simulation

Compact models of a circuit element are simple mathematical descriptions of the behavior of that circuit element, which are used for computer-aided design (CAD) and analysis of integrated circuits (ICs). Compact models describe the device characteristics of a manufacturing technology by a set of physics-based analytical expressions with technology-dependent device model parameters that are solved by a circuit simulator for circuit analysis during IC design. *Compact modeling* refers to the art of generating compact models of an IC process technology by extracting elemental model parameters for accurate prediction of the behavior of the circuit elements of that technology in circuit simulation. In reality, the complete compact models include the modeling of each circuit element along with its parasitic components that run robustly for realistic assessment of the representative IC technology in circuit CAD [1,2].

Compact models of the circuit elements of an IC manufacturing technology have been the major part of electronic design automation (EDA) tools for circuit CAD since the invention of ICs in the year 1958 [3] and are playing an increasingly important role in the nanometer-scale system-on-chip design era. Today, compact models are the most important part of the process design kit [4,5], which is the interface between circuit designers and device technology. As the mainstream complementary metal-oxide-semiconductor (CMOS) technology is scaled down to the nanometer regime, a truly physical and predictive compact model for circuit CAD that covers geometry, bias, temperature, DC, AC, radio frequency (RF), and noise characteristics has become a major challenge for model developers and circuit designers [1]. A good compact model has to accurately capture all real-device effects and simultaneously produce them in a form suitable for maintaining high computational efficiency.

In the microelectronics industry, compact modeling includes (1) compact device models of the active devices such as bipolar junction transistors (BJTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) along

with the parasitic elements of the active devices; and (2) compact interconnect models of the resistors, capacitors, and inductors of the metallization layers connecting the active devices in the ICs.

1.1.1 Compact Device Models

Compact device models describe the terminal behavior of a device in terms of the current-voltage (*I–V*), capacitance-voltage (*C–V*), and the carrier transport processes within the device. Figure 1.1 shows the basic features of a typical compact device model of a representative IC technology. As shown in Figure 1.1, a compact model is made of a *core model* along with the various models to account for the effects of the geometry and physical phenomena in the device. For a metal-oxide-semiconductor (MOS) transistor, the core model describes *I–V* and *C–V* behavior of an ideal large MOSFET device [4] of a target technology. The core model represents about 20% of the model code in terms of both execution time and the number of lines in the code. The rest of the model code comprises multiple models that describe the numerous real-device effects that are responsible for the accuracy of the compact

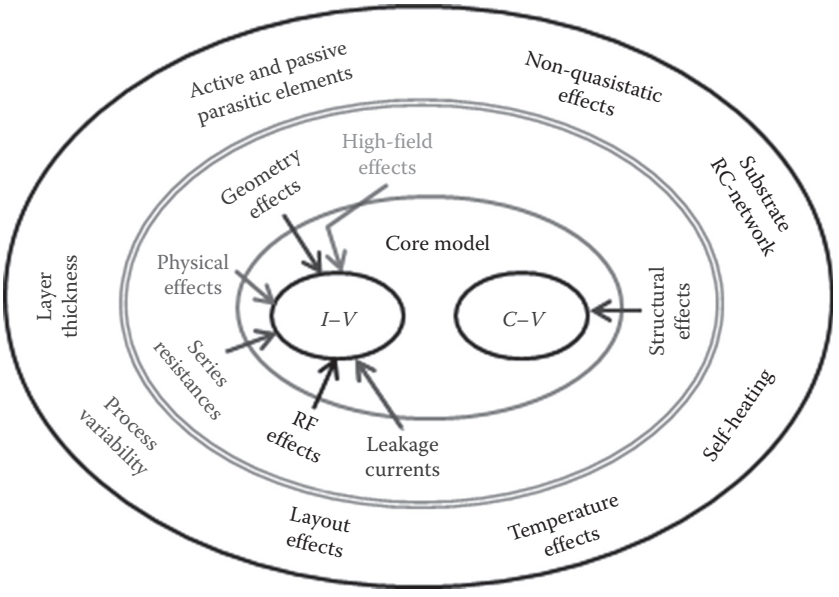

FIGURE 1.1
A typical composition of compact models of an IC technology: the core model includes the basic *I–V* and *C–V* behavior of a large geometry device in the inner circle; the core model is accompanied by the models for physical phenomena within the device and geometry and structural effects as shown in the middle circle; the final compact model with the geometrical and physical effects includes the external phenomena such as ambient temperature, layout effects, process variability, and NQS effects as shown in the outer circle of the model.

model. For MOSFET devices, device phenomena accompanying the core model include short-channel effects (SCEs), output conductance, quantum mechanical effects (QMEs), nonuniform doping effects, gate leakage current, band-to-band tunneling, noise, non-quasistatic (NQS) effect, intrinsic input resistance, and strain effect [4,6].

The compact model for circuit CAD is the bridge between the circuit design and processing groups and is a module of the extended technology CAD (TCAD) environment [7]. In the extended TCAD environment, the compact model plays an important role in developing next generation IC fabrication technology and assesses the manufacturability of IC fabrication processes by reverse modeling [7,8].

1.1.2 Compact Interconnect Models

Today's very-large-scale-integrated (VLSI) circuits consist of MOSFET devices and their interconnections, referred to as *interconnects*. In a typical VLSI chip, the active area is about 10% whereas the physical area is occupied by interconnect and isolation regions 6–10 times the active device area [9]. For this reason, the role of the interconnect is becoming increasingly important as the feature size is scaled down to decananometer regimes and the device density is increased on the chip. As VLSI technology shrinks below 22-nm geometries with Cu/low-*k* interconnections, parasitics due to interconnections are becoming a limiting factor in determining circuit performance. Therefore, accurate modeling of interconnect parasitic resistance (R), capacitance (C), and inductance (L) is essential in determining various on-chip interconnect-related issues, such as delay, cross talk, energy losses in R due to the current (I) flow or IR drop, and power dissipation. Accurate compact interconnect models are crucial for the design and optimization of advanced VLSI circuits for 22-nm CMOS technology and beyond. In addition, with the emergence of technologies such as carbon nanotubes and graphene nanoribbons, compact interconnection models that are suitable for these technologies are crucial for advanced circuit design. Currently available interconnect models, which are based on field solvers, are inadequate for accurate and meaningful analyses of today's chips, which house millions of devices. Interconnect models can accurately simulate on-chip global interconnections and speed-power optimization for advanced interconnect technologies. Modeling of these interconnect properties is thus important and must be included by the designer when checking circuit performance in circuit CAD. Though interconnect models are an essential part of optimizing VLSI circuit performance, interconnect modeling is outside the scope of this book; interested readers may refer Saha et al. [10] for recent development of interconnect models. In this treatise, compact modeling of field-effect transistors (FETs) and their parasitic components that are used in the mainstream VLSI circuit design are described.

1.2 Brief History of Compact Device Modeling

Since the 1960s, compact models for circuit CAD have continuously evolved [6]. After the invention of the bipolar transistor in 1947 [11,12], complete circuits including both active and passive devices were realized on monolithic silicon substrates by late 1950s. Computer simulation evolved as a practical way to predict circuit performance including nonlinearities because digital computers were capable of complex circuit analysis based on a network or matrix formulation. The 1950s and 1960s were dominated by BJT technology; the Ebers–Moll (EM) model has been the major large-signal compact model for bipolar transistors since its formulation in 1954 [13]. It is based directly on device physics and covers all operating regimes, that is, active, saturation, and cut-off operations of BJTs. However, various approximations limit the accuracy of the model. To overcome the limitation of the EM model, Gummel and Poon reported a BJT model based on *integrated charge control relations*, in 1970 [14]. The Gummel–Poon (GP) model offers a very clear and standardized description of existing physical effects in BJTs. Due to its simple yet physical model formulation, GP model remains the most popular BJT model till date. By the early 1970s, the circuit simulator had become a useful tool, essentially replacing the breadboarding of prototypes. The circuit CAD tool, *Simulation Program with Integrated Circuit Emphasis* (SPICE) from the University of California, Berkeley, became a widely used tool among the circuit design community [15]. Thus, with the introduction of SPICE, the compact model has become essential for circuit CAD. Meanwhile, the IC industry had reached an important juncture in its development. While the 1950s and 1960s were dominated by BJT technology, the 1970s saw MOS technology begin to overtake BJT technology in terms of functional complexity and level of integration. Thus, from simple basic compact MOSFET models, sophisticated models for FETs started to emerge. Today's sophisticated compact models for MOSFETs [4,16–20] evolved from models first developed 30 to 50 years ago [13,14,21–24]. A large number of developers have contributed to the evolution of compact modeling. In this section, we present only a brief history of the major development in the compact MOSFET modeling activities.

1.2.1 Early History of Compact MOSFET Modeling

In the early 1960s, MOSFET devices were introduced in fabricating ICs [25]. In order to understand the behavior of these emerging MOSFET devices, research effort on the development of semi-analytical models using simple device structures and simplified device physics started in the 1960s [21,26]. In 1964, Ihantola and Moll reported the design theory of MOSFET devices and developed the drain current (I_{ds}) equation to account for the varying bulk charge effect in the devices [21]. In the same year, Sah reported a simple theory of the MOSFET devices using valid approximations and simple

assumptions and derived I_{ds} equations for circuit analysis [26]. In these models, the device is considered to be turned on above a certain applied input voltage, referred to as the *threshold voltage* (V_{th}), and turned off at the input bias below V_{th}. This approach is known as *threshold voltage–based* or, *V_{th}-based compact modeling*.

With the great potential of MOSFET devices in ICs during 1960s, a detailed understanding of MOSFET device physics became critical. In 1966, Pao and Sah [22] reported an I_{ds} equation to describe MOSFET device characteristics under varying biasing conditions in terms of a physical parameter called the *surface potential* (ϕ_s), where ϕ_s describes the mode of operation of MOSFET devices under the applied biasing conditions. It is to be noted that V_{th} is defined at a particular value of ϕ_s above which the device starts conducting whereas ϕ_s defines the entire range of operation of MOSFETs from *off-state* to *on-state*, depending on the applied biasing conditions. The value of ϕ_s is calculated, iteratively, from an implicit expression derived from Poisson's equation and Gauss's law. This I_{ds} model is a double integral equation, commonly known as the Pao-Sah model, that can only be solved numerically. Inherently, it takes into account both the drift and diffusion components of I_{ds}, and is valid in all regions of device operation: from the subthreshold (below V_{th}) to strong inversion region (above V_{th}). This method is now known as *surface potential*–based or, ϕ_s-based compact modeling. Sah's ϕ_s-based modeling requires iterations and integration and is computationally demanding for circuit CAD. Thus, the Pao-Sah model is inefficient for circuit CAD due to its complexities involving integration and iterations to get I_{ds} at each value of applied voltage. Thus, the search for simplified models for circuit CAD began in the late 1960s.

In the late 1970s, SPICE emerged as an essential circuit CAD tool to perform accurate and efficient design and analysis of ICs under the EDA environment [27]. In order to use SPICE, accurate and efficient compact models are required to describe the behavior of the devices used in the circuits. Thus, the explicit development of MOSFET compact models for circuit CAD started with the widespread usage of SPICE and continues today as the mainstream MOSFET devices rapidly approach their fundamental scaling limit near the 10-nm regime [1,28–33].

The first approach used in developing I_{ds} model is to circumvent the iterative computation of ϕ_s from the implicit relation [22] using V_{th} as the boundary between the off-state or weakly conducting state, referred to as the *weak inversion region*, and on-state, called the *strong inversion region*, of MOSFET devices, that is, use V_{th}-based compact modeling. This approach results in two current equations, one for the weak inversion and the other for strong inversion [25,34]. In V_{th}-based modeling, a linear approximation is made between ϕ_s and the applied input voltage to eliminate ϕ_s and relate the input voltage to the output current I_{ds}. This approach results in a simple *I–V* equation in the parabolic form and was first used for circuit simulation in 1968 [34]. This is the first known compact MOSFET model for circuit CAD and is referred

to as the *Schichmann and Hodges* model. This model is implemented in SPICE as the MOS Level 1 model and is developed based on a number of simplifying assumptions and device physics appropriate for uniformly doped long-channel MOSFET devices. In addition, in MOS Level 1 model, the value of I_{ds} is zero below V_{th}, increases linearly above V_{th}, and remains constant above a drain saturation voltage (V_{dsat}). The MOS Level 1 model, though inaccurate, is widely used for hand calculation of *I–V* data and preliminary circuit simulation because of its simplicity and ease of use.

In order to account for the shortcomings of MOS Level 1 model such as small geometry effects, Ihantola and Moll [21] modified the device equation to use in SPICE as the MOS Level 2 model. The basic approach is to begin with the Level 1 model, and add equations and parameters to include the small geometry effects as corrections to the basic model. Unlike the Level 1 model, it is assumed that the depletion charge varies along the length of the channel; this results in a complex but more accurate expression for I_{ds} in SPICE Level 2 MOS model [35]. However, it is still not accurate for devices with submicron geometries.

In 1974, MOSFET scaling rule was established [36], and the MOSFET device and technology continued to evolve. As a result, the MOS device physics became complex, circuit density increased, and the device models were continually updated to account for emerging physics in scaled MOSFETs. The result is the evolution of MOS compact models. In 1978, Brews [23] reported a simplified model based on charge sheet approximation of the inversion charge density (Q_i) along with depletion approximation. With justified assumptions of Q_i, the total I_{ds} is shown to be the sum of the drift (I_{ds1}) and diffusion components (I_{ds2}). The values of ϕ_s at the source end (ϕ_{s0}) and drain end (ϕ_{sL}) of the devices required to calculate I_{ds} are obtained numerically by solving the implicit equation for ϕ_s along the channel at each applied biasing condition. In weak inversion, where ϕ_{s0} is almost equal to ϕ_{sL}, even a small error in the values of ϕ_{s0} and ϕ_{sL} can lead to a large error in the current I_{ds2}, which depends on the value of $(\phi_{sL}-\phi_{s0})$ [23]. Therefore, an accurate solution is required for the surface potential, particularly for weak inversion current calculations. There are several iterative schemes developed to solve the implicit equation for ϕ_s [37]. However, the available iterative schemes to solve this equation were relatively slow and did not include all regions of device operation while noniterative approximations did not extend to the accumulation region and were not sufficiently accurate, especially for computing the transcapacitances. Besides, the early ϕ_s-based models [23,37] consist of complex and lengthy expressions for currents, charges, and noise [38]. Thus, due to the complexity of the ϕ_s expression along with the lack of efficient techniques to compute ϕ_s, these models [23,37] were computationally challenging for circuit simulation in the early days of EDA environment. Therefore, search for different approaches continued to simplify the model for efficient solution of the model equations for circuit CAD in EDA environment.

In 1981, Level 3 MOS model was introduced for circuit CAD using SPICE2 [39]. Level 3 MOS model introduced many empirical parameters to model SCEs. However, the accuracy and scalability of the model for simulation of a wide range of channel length and width using one set of model parameters are not entirely satisfactory to the circuit designers. The short channel and narrow width effects are not modeled accurately in the MOS Level 1, 2, and 3 models and high field effects are not considered properly because of the limited understanding of the physics of small geometry devices at the time these models were developed. Thus, to keep parity with the continuous scaling down of MOSFETs, global effort continued for the development of accurate and efficient compact models for circuit CAD.

1.2.2 Recent History of Compact MOSFET Modeling

As the CMOS technology became the pervasive technology of ICs in 1970s, the complexities of MOSFET devices continued to increase. As a result, compact models based on simplified device physics became inadequate to analyze scaled geometry MOSFETs. The efforts for accurate and computationally efficient models continued using different approaches. The major modeling techniques used can be described as *threshold voltage-based*, *surface potential–based*, and *charge-based* as described in Sections 1.2.2.1 through 1.2.2.3.

1.2.2.1 Threshold Voltage–Based Compact MOSFET Modeling

The major development of V_{th}-based compact MOS model is the development of *Berkeley Short Channel IGFET Model*, commonly known as BSIM, in the year 1987 [24]. It incorporated some improved understanding of the SCEs and worked well for devices with channel length of 1 μm and above. However, it also introduced several empirical fitting parameters just to enhance the scalability of the model. Even then, the model scalability was not totally satisfactory. Also, circuit designers did not like the use of many fitting parameters, which do not have any physical meaning.

In order to address the shortcomings of the first generation of BSIM or BSIM1, BSIM2 was introduced in 1990 [40]. BSIM2 improved upon BSIM1 in several aspects such as model continuity, output conductance, and subthreshold current [40]. However, the model still could not use one set of parameters for wide range of device sizes. Users typically need to generate a few or many sets of model parameters, each covering a limited range of device geometries in order to obtain good accuracy over the full range of devices used in circuits. This makes the parameter extraction difficult. Also, it is difficult to use these parameters to perform statistical modeling or extrapolation of the model parameters from the present technology to a future one.

In early 1990s, the proprietary compact model, HSPICE Level 28, was released from Meta-Software to address the shortcomings of BSIM1 [41,42]; where 'H' in HSPICE abbreviates the initial of the family name, "Hailey' of the developers of the industrial SPICE circuit CAD and founders of the company Meta-Software. The widespread use of Meta-Software's circuit CAD tool, HSPICE, served as the vehicle for the Level 28 model, helping Level 28 to become the most widely used MOSFET model in the semiconductor industry. The HSPICE Level 28 model is based on BSIM, without many of BSIM's intrinsic shortcomings; it also has accurate capabilities for modeling both the analog and digital circuits in contrast to BSIM that has been mainly developed for modeling digital circuits.

In 1994, BSIM3 [43] was developed to account for the shortcomings of BSIM2. The device theory has been developed over a number of years [43–46]. The model explicitly takes into account the effects of many device sizes and process variables for good model scalability and predictability. The short channel and narrow width effects as well as high field effects are well modeled. The first released version of BSIM3, BSIM3v2 [43], offered better model accuracy and scalability than the previous BSIM models but it still suffers from discontinuity problems such as negative conductance and glitches in the g_m/I_{ds} versus V_g plot at the boundary between weak inversion and strong inversion; where g_m is the device transconductance. In the meantime, the need for a good open MOSFET model had been widely recognized by the semiconductor companies. To eliminate all the kinks and glitches in BSIM3v2, BSIM3v3 with a single-equation approach along with the enhanced modeling of small size and other physical effects [44–47] was developed. The BSIM3v3.0 model has been extensively verified and selected as the first industry standard compact MOSFET model in 1996 by Compact Modeling Council (CMC) [48]. The convergence performance of BSIM3v3.0 was enhanced in BSIM3v3.1 [45]. Version BSIM3v3.2 [47] introduced a new charge/capacitance model that accounts for the QM effect, and improves V_{th} model, substrate current model, NQS model, and others and was released in 1998 and 2005 [49–51].

During 1990s, Philips Laboratories started developing MOS Model 9 [52,53] and released the model in 1994 [54], making it widely available in mainstream circuit CAD tools. The basic features of MOS 9 include very clean and simple model equations, use of well-behaved hyperbolic expressions as smoothing functions for good behavior in circuit simulation, and less number of model parameters. The smoothing functions in MOS 9 serve continuous and smooth equations across the various transition points (such as V_{dsat}) of MOSFET operation and allow the realization of a single-model equation (e.g., I_{ds} equation) valid in all regions of device operation. Finally, MOS 9 includes some of the features of HSPICE Level 28, thus accommodating proper model binning. Unlike BSIM3, MOS 9 retains the existing approach in describing the geometry dependence of the model characteristics. While the basic method of the existing modeling know-how is used, the method is extensively modified to improve the circuit simulation results.

In the meanwhile, BSIM has been continuously updated and extended to accurately model the physical effects observed in sub-100 nm regime. In 2000, BSIM4, version BSIM4.1.0, was released [55]. BSIM4 offers several improvements over BSIM3, including the traditional *I–V* modeling of intrinsic transistor, the transistor's noise modeling, and the incorporation of extrinsic parasitics. Some of the salient features of BSIM4 are an accurate model of the intrinsic input resistance for RF, high-frequency analog and high-speed digital applications, flexible substrate resistance network for RF modeling, an accurate channel thermal noise model along with a noise partition model for the induced gate noise, an NQS model consistent with the gate resistance-based RF model, an accurate gate direct tunneling model, a geometry-dependent parasitics model for various source-drain connections and multifinger devices, improved model for steep vertical retrograde doping profiles, better model for halo-implanted devices in V_{th}, bulk charge effect model, and output resistance, asymmetrical and bias-dependent source-drain resistance, QM charge-layer model for both *I–V* and *C–V*, gate-induced drain/source leakage (GIDL/GISL) current model, and improved unified $1/f$ noise model [55–57].

1.2.2.2 Surface Potential–Based Compact MOSFET Modeling

In the surface potential–based modeling approach [23,37], ϕ_s is solved at the two ends of the MOS channel. The terminal charges, currents, and derivatives are then calculated from ϕ_s. During 1980s, a considerable progress has been made to solve ϕ_s efficiently from the implicit ϕ_s equation. In 1985, Bagheri and Tsividis reported an efficient algorithm [58] to solve these implicit ϕ_s equations using Schroder series method [59,60], which is based on Taylor series expansion of the inverse function, provided a good initial guess such as the *zero-order* relationship [61] is used. It is reported that at most only two iterations are required to achieve an excellent estimation of ϕ_{s0} or ϕ_{sL} in all operating regions.

In 1994, Arora et al. reported an efficient ϕ_s-based MOSFET model referred to as the "PCIM" for in-house circuit simulation of Digital Equipment Corporation's (DEC) Alpha chip [62]. Based on the source-side-only surface potential proposed by Park [63], Rios et al. in 1995 reported a model that is shown to be practical and efficient and used it in DEC's Alpha chip design from 1996, featuring automatic and physical transitions between partially and fully depleted modes of Silicon-on-Insulator (SOI) operations [64,65]. The source-side-only solution was used to offer a good compromise between the accuracy and simplicity, and the solution speed required for practical applications. This approach was shown to avoid solving for ϕ_s on the drain side, while providing a simple and self-consistent treatment of carrier velocity saturation. In addition, the appropriate treatment of the body charge linearization and the effective drain bias was used to maintain source-drain symmetry. The solution method preserves source-drain symmetry and produces the correct drain current behavior near drain voltage, $V_{ds} = 0$. It was reported that in the source-side-only approach, simple, explicit, and self-consistent V_{dsat}

solutions are possible by equating the saturation drain current to the model drain current equation, at $V_{ds} = V_{dsat}$. The velocity–field relation requires special treatment to be able to include the effect of longitudinal field-dependent mobility in the integration of the continuity equation. A good approximation was proposed by Arora et al. [62]. The small geometry effect and different physical effects including QM and polysilicon depletion effects are implemented in the CAD-oriented analytical MOSFET model [61]. QMEs on the inversion charge density can be handled in a physical manner by a bandgap-widening approach [65].

The development of ϕ_s-based *Hiroshima University STARC IGFET Model*, referred to as the HiSIM, has been started in the early 1990s based on the drift-diffusion concept and proved its feasibility for real applications [66–68]. Since 1993, the model has been successfully applied in the development of dynamic random-access memory (DRAM), subthreshold region ICs, and IC-card products at Siemens. In HiSIM, the surface potentials are obtained by solving the Poisson's equation iteratively both at the source side and at the drain side with an accuracy of 10 pV, and simulation speed is comparable to industry standard V_{th}*-based* models [66]. The reported accuracy is absolutely necessary for maintaining sufficient accurate solutions for transcapacitance values and achieving stable circuit simulation [69]. The salient features of HiSIM include accurate modeling of small geometry effects, polydepletion effects, and QM effects in MOSFETs. This is accomplished by modifying the generalized expression for ϕ_s to include a shift in V_{th} due to the above-referred physical effects. The HiSIM modeling approach automatically preserves scalability of model parameters, and thus, one model parameter set for all device dimensions is used. Since a complete ϕ_s-based model automatically preserves the overall model consistency through ϕ_s, the number of model parameters can be drastically reduced in comparison to the conventional V_{th}-based models [68]. This parameter reduction comes without any loss in the reproduction accuracy of measurement data (e.g., *I–V* characteristics). Moreover, it has been reported that the nonlinear phenomena such as harmonic distortions are accurately calculated automatically [69]. All higher-order phenomena observed such as noise have been shown to be determined by the potential gradient along the channel [69], which again highlights the strength of the concept of ϕ_s-based modeling. Investigations of the high-frequency small-signal behavior with HiSIM concluded that the NQS effect is not as strong as previously believed [70,71]. Three members of the HiSIM family have been selected as the industry standards by CMC [48]. HiSIM-HV (1st standard version released in January 2009) is the high-voltage MOS device model standard, HiSIM2 (1st standard version released in April 2011) is the second-generation MOSFET model standard, and HiSIM-SOI (1st standard version released in July 2012) is the surface-potential SOI-MOSFET model standard.

At Philips Semiconductors, the development of MOS model 11 or MM11 started in 1994, primarily aimed at simple and accurate digital, analog, and RF

modeling [72] of advanced ICs using analytical solution of surface potential. The implicit ϕ_s equation is modified to include polysilicon depletion effect by including a potential across the depletion layer due to polysilicon depletion and an empirical parameter to account for SCEs. In order to obtain efficient expressions for model outputs, several approximations were made, mainly based on the linearization of the inversion charge as a function of ϕ_s. In MM11, a linearization is performed around the average of source and drain potentials given by $\bar{\phi}_s = 1/2\left(\phi_{s0} + \phi_{sL}\right)$ [72]. This linearization technique was shown to yield simpler and accurate expressions for ϕ_s keeping model symmetry with respect to source-drain interchange. This linearization approach offers an easy implementation of well-known physical phenomena such as thermal noise [73], induced gate noise [73], and gate leakage [74] in ϕ_s-based models.

In MM11, an accurate description of mobility effects and conductance effects has been added with a special emphasis on distortion modeling. For an accurate description of distortion, MM11 model is shown to accurately describe the drain current and its higher-order derivatives (up to at least the 3rd order). Thus, MM11 models reported contain improved expressions for mobility reduction [75], velocity saturation, and various conductance effects [76]. The distortion modeling of MM11 has been rigorously tested on various MOSFET technologies [77], and is shown to offer an accurate description of modern CMOS technologies. MM11 model is shown to preserve the source-drain interchange symmetry in model expressions [75,78] and thus eliminates the discontinuities in the high-order derivatives of channel current at $V_{ds} = 0$ [79]. MM11 incorporates an accurate description of all-important physical effects, such as polydepletion [80], the effect of pocket implants [81], gate tunneling current [66,80], bias-dependent overlap capacitances [80,82], GIDL, and noise [68,83] and therefore offers an accurate description of advanced MOSFETs in circuit operation.

In the early 1990s, the development of ϕ_s–based model, called *SP model*, started at the Pennsylvania State University by the research group led by Gildenblat. The modeling algorithm has been developed over the years [84–90]. In SP, SCE is modeled using the reported [91] bias and geometry-dependent lateral gradient factor while the geometry-dependent technique was used in HiSIM [68]. To overcome the inherent complexities of ϕ_s-based compact model, especially the expressions for the intrinsic charges [38,92,93], various approximations were developed based, primarily, on the linearization of the inversion charge as a function of ϕ_s. It is observed that this linearization technique [79] is a critical step to preserving the Gummel symmetry test and to avoid difficulties in the simulation of passive mixers and related circuits [94]. The symmetric linearization method developed in SP [85,87,93] preserves the Gummel symmetry and produces expressions for both the drain current and the terminal charges that are as simple as those in V_{th}-based or Q_i-based models and are numerically indistinguishable from the original charge-sheet model equations [85,94].

It has been reported that the symmetric linearization approach is not particularly sensitive to the details of the velocity saturation model, which enabled the merger of the best features of the SP and MM11 models to create PSP model. In addition to charge linearization relative to the source causing violation of the Gummel symmetry test, the singular nature of the popular velocity saturation model [79,94] is a critical problem. The problem can be solved using different techniques such as adopting a V_{ds}-dependent critical field [38,62,72]. When combined with the symmetric linearization method, this technique automatically solves the singularity issue [85,94]. Some of the specific features of SP include its unique symmetric linearization method, completely noniterative formulation, nonregional description from accumulation to strong inversion, inclusion of all relevant short-channel and thin-oxide effects, bias-dependent effective doping to deal with *halo* effects, physical description of the overlap regions and of the *inner-fringing* effects, and the comprehensive and accurate NQS model based on the spline collocation method [93]. The latter has been recently extended to include the accumulation region [92] and the small-geometry effects [95]. Finally, it has been reported [96,97] that when combined with the general one-flux theory of the nonabsorbing barrier, SP model is capable of reproducing the quasi-ballistic effects using the one-flux method [98].

The new ϕ_s–based PSP model is obtained by merging and developing the best features of SP (developed at the Pennsylvania State University) and MM11 (developed at Philips) models. The first version of the compact MOS model PSP, Level 100, has been released to the public domain in April 2005. In December 2005, CMC elected PSP as the new industrial standard model for compact MOSFET modeling [48].

1.2.2.3 Charge-Based Compact MOSFET Modeling

During the late 1980s, the charge-based compact models emerged as a viable alternative to widely used V_{th}-based compact models due the increasing complexities of V_{th}-based modeling for scaled MOSFET devices and computationally demanding solution techniques for ϕ_s-based modeling. In 1987, Maher and Mead reported a drain current expression in terms of the inversion charge density (Q_i) at the source and the drain ends [99]. Subsequently, a unified charge control model (UCCM) relating charge densities in terms of terminal voltages was reported in the early 1990s [100,101]. In 1995, Cunha et al. derived expressions for the total charges and small signal parameters as a function of the source and drain channel charge densities [102]. In 2001, Gummel et al. derived a charge equation and reported a charge-based model, referred to as USIM [103]. In 2003, He et al. reported an alternative derivation of charge [104] using gradual channel [26] and charge-sheet [23] approximations and linearization of the bulk and inversion charges with respect to the

surface potential at a fixed gate bias. Since there is no Q_i in the accumulation region, different approaches used include an equation for the accumulation charge similar to that for Q_i or accumulation surface potential.

In charge-based models, an implicit function is evaluated to find the charge density for each set of biasing voltages in SPICE iterations similar to ϕ_s calculation. Note that the current is an exponential function of ϕ_s whereas a linear or quadratic function of Q_i. Therefore, the accuracy of calculation of the Q_i is not as high as that of ϕ_s calculation. Some of the widely referred charge-based compact MOSFET models include ACM [102], EKV [16], and BSIM6 [4] as described below.

In 1995, Cunha et al. reported a charge-based compact model, called the *advanced compact MOSFET* or *ACM model* [102]. The basic formulation of the ACM model is based on the charge-sheet model [23], inversion charge versus current relationship [99], UCCM [100,101], and symmetrical MOSFET model [105]. Explicit expressions for the current, charges, transconductances, and the 16 capacitive coefficients are shown to be valid in the weak, moderate, and strong inversion regions. In 1997, the ACM model was implemented in a circuit simulator [106] and emerged out of the necessity of modeling MOS capacitor for analog design in digital CMOS technology. In order to model the weak nonlinearities of an MOS capacitor in the accumulation and moderate as well as strong inversion regimes, Behr et al. reported an improved capacitive model of the MOSFET gate in 1992 [107]. A link between the charge model by Cunha et al. [102] and the current-based model of Enz et al. [16] was established by Galup-Montoro et al. [105] and Cunha et al. [108]. The models for DC, AC, and NQS behaviors were developed [105,106]. In 1999, UCCM [100,101] was revisited [109,110] to enhance the basic ACM model [102].

The ACM model has been reported to have a hierarchical structure facilitating the inclusion of different physical phenomena into the model [111]. Because of its very simple expression for the derivative of the channel charge density, ACM has been reported to offer simple explicit expressions for all intrinsic capacitive coefficients even when SCEs are taken into account [111]. The parameters of the ACM can be easily extracted [108,110]. Recently, ACM has been reported to include unified $1/f$ noise and mismatch models [112,113].

In 1995, Enz et al. reported an analytical compact MOSFET model, referred to as the EKV model, by referencing all the terminal voltages to the substrate [16]. The primary objective of the EKV model was low-power analog IC CAD using an analytical model that is valid in all modes of device operation with accurate modeling of weak inversion regime [114,115]. The model uses the linearization of Q_i with respect to the channel voltage to derive I_{ds} based on the continuous g_m/I_{ds} characteristics. In 2003, a rigorous derivation of the charge-based EKV model along with the detailed technique of Q_i linearization was reported using the existing charge-based models [99,103,116,117].

The bulk voltage referencing makes the EKV model symmetric [118–120] and preserves the symmetry property with reference to effects such as velocity saturation and nonuniform doping in the longitudinal direction [121]. The EKV model uses normalized Q_i at the source and drain ends to determine all the important MOSFET variables including the current [118,122], the terminal charges [123], the transcapacitances [123–125], the admittances, the transadmittances, [125], and the thermal noise, including the induced-gate noise [126,127].

It is shown that in the charge-based EKV model, Q_i linearization offers a direct, simple relation between the surface potential ϕ_s and Q_i [118,122,128]. The EKV model has been evolved into a full featured scalable compact MOS model that includes all the major effects that have to be accounted for in deep submicron CMOS technologies [129–131]. The model has also been extended to double-gate device architectures using the EKV charge-based approach [132].

In 2003, He et al. reported the charge-based BSIM5 model that uses a single set of equations to calculate terminal charges throughout all the bias regions [104,133]. The BSIM5 Q_i equation is derived directly from the solution of Poisson's equation in terms of ϕ_s in contrast to the conventional charge-based models [16,102] to obtain the final explicit function relating Q_i with MOS terminal voltages. The core BSIM5 model is derived assuming gradual channel and constant quasi-Fermi level to the channel current, I_{ds} in terms of Q_i at the source and drain ends. The I_{ds} equation includes the diffusion and drift components in a very simplified form. The model is reported to offer symmetry, continuity, scalability, and computational efficiency with a minimal number of parameters. It can easily incorporate short-channel, nonuniform doping, and numerous other physical effects such as polydepletion, velocity saturation, and velocity overshoot to accurately model subtle details of the device behaviors including current saturation and QM effect. It is also reported that BSIM5 core model can be easily extended to model nonclassical devices such as ultrathin body SOI and multigate devices including FinFETs [134].

In late 2010, the BSIM group started the development of BSIM6 core model [4]. The basic objective of BSIM6 development is to solve the symmetry issue of BSIM4 while maintaining BSIM4's accuracy, speed, and user support. The core BSIM6 has been derived using the reported charge-based approach [99,128,131,133]. The main features of BSIM6 include: smooth and continuous behaviors of *I–V* and *C–V* and their derivatives; continuity around $V_{ds} = 0$ and symmetry issue; excellent scalability with geometry, bias, and temperature; robust and physical behavior; excellent analog and RF modeling capability; and maintaining BSIM4 user experience [135]. In May 2013, BSIM6 has been selected and released as the industry-standard compact model for the existing as well as advanced planar CMOS technology nodes [48]. The model has been coded in Verilog-A and implemented in major EDA environment [136].

1.3 Motivation for Compact Modeling

The major motivation for the use of compact model for circuit CAD in the semiconductor industry is the cost-effective and efficient design optimization of IC products [137] in EDA environment. The use of compact models in circuit CAD allows optimization of circuit performance for robust IC chip design. This optimization is a complex task due to the increasing complexities of the scaled MOSFET devices and technology. The continuous scaling of CMOS devices to sub-100 nm regime has resulted in higher device density, faster circuit speed, and lower power dissipation. Many new physical phenomena such as SCE and reverse SCE (RSCE), channel length modulation, drain-induced barrier lowering, remote surface roughness scattering, mobility degradation, impact ionization, band-to-band tunneling, velocity overshoot, self-heating, channel quantization, polysilicon depletion, RF behaviors, NQS effects, and discrete dopants become significant as the device dimension approaches its physical limit [51,55]. Thus, intuitive analysis of the performance of nanoscale VLSI circuits using first principle is no longer possible whereas trial-and-error experimentations using breadboarding prototype [27] to build and characterize advanced IC chips are time consuming and expensive. In addition, advanced VLSI circuits with scaled devices are susceptible to process variability, causing device and circuit performance variability [5]. As a result, the statistical analysis of circuits is critical to develop advanced VLSI chips. Therefore, the compact models are the desirable alternative for cost-effective and efficient design of robust VLSI circuits, analysis of statistical device performance, analysis of yield, and so on.

Again, by the introduction of the SPICE program from Berkeley in 1975, the circuit simulator became a useful design tool, essentially replacing the breadboarding of prototypes [27]. However, for accurate circuit analysis, compact device models are required. Thus, the widespread use of circuit simulation also motivated the early development and use of compact model for IC device analysis. For today's circuit design, the major motivations for compact modeling include:

1. Circumventing the inadequate conventional manual techniques for design and analysis of today's complex VLSI circuits consisting of billions of nanoscale devices
2. Designing an IC chip under the worst-case conditions so that manufacturing tolerances can be incorporated into the design, thus ensuring the target production yield of the chip
3. Performing statistical analysis to optimize circuits for process variability–induced circuit performance variability, and also ensuring the target production yield of the chip

4. Design-for-reliability, enabling designers to predict and optimize circuit performance
5. Improving design efficiency using compact models instead of measured data from billions of transistors with different dimensions operating under different voltages that are used in an IC chip

1.4 Compact Model Usage

Compact models are an integral part of circuit analysis in EDA environment. Typically, the analytical equations of the target compact model (e.g., BSIM4) are fitted to the device characteristics of an IC technology obtained under different biasing conditions and extract device model parameters. These model parameters are used to generate a technology-specific device model library. Similarly, compact model parameters for passive elements of a circuit are extracted from the respective model formulations. Thus, a model library includes compact models for active and passive elements describing the behavior of these elements in VLSI circuits. This model library is used as the input file along with the input circuit description, called the *netlist*, for circuit simulation using a circuit CAD tool [27] as shown in Figure 1.2. A netlist describes the detailed description of a circuit performance under the target biasing conditions.

Figure 1.2 shows a circuit netlist and compact model library as the input to circuit CAD and the output is the simulation results including circuit speed (delays), logic levels, circuit performance variability, and SRAM yield.

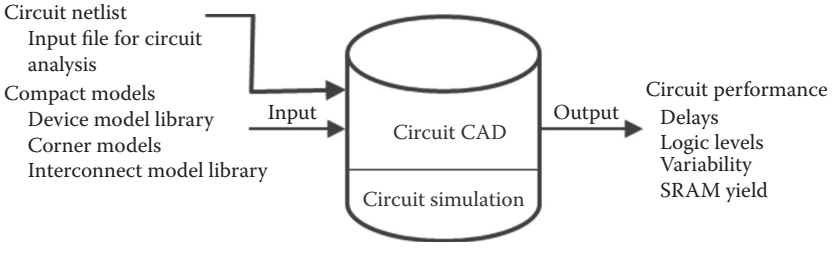

FIGURE 1.2
Usage of compact models in a circuit CAD: compact models describing the performance of circuit elements are used as the input to circuit CAD along with the description of the VLSI circuit for computer analysis of circuit performance; circuit CAD is a circuit simulation tool for computer analysis of VLSI circuits in EDA environment.

1.5 Compact Model Standardization

From the brief history of compact device models in Section 1.2, we find that a large number of compact MOSFET models have been developed over the past 40 years and are continued to date. Therefore, it is extremely difficult to generate, maintain, and support a large number of model libraries for a large number of process technologies for circuit CAD by device engineers of a manufacturing company. In order to improve the efficiency of compact modeling for circuit CAD, model developers and users have made a joint effort to establish a standard compact model for each IC device with robustness, accuracy, scalability, and computational efficiency to meet the needs of digital, analog, and mixed analog/digital designs. A standard model common to all or most semiconductor manufacturers and circuit CAD tools is desirable to facilitate intercompany collaborations.

With the objective of compact model standardization, an independent Compact Model Council, CMC was founded in 1996, consisting of many leading companies in the semiconductor industry. The charter of CMC is to promote the international, nonexclusive standardization of compact model formulations and the model interfaces. The CMC standardizes compact models for all major technologies to enhance the design efficiency, performs extensive model testing for model validation, and ensures robustness and accuracy of compact models for the latest technologies to shorten leading-edge design development cycle time. In 2013, CMC has become a part of an EDA standardization forum, Si2, to continue offering compact model standardization.

1.6 Summary

This chapter presents an overview of compact modeling for circuit CAD and the constituents of compact models to mathematically describe the real device effects. A brief history of compact MOSFET models for circuit simulation from the first Schimann-Hodges in 1970s to the recent surface potential–based and inversion charge–based models is presented. It is found that the early compact MOS models consist of physics-based analytical expressions to simulate the basic characteristics of devices in digital circuits. These models were continuously updated using empirical equations containing empirical fitting parameters to facilitate efficient circuit simulation. During 1980s physics-based compact MOS models with well-behaved mathematical smoothing functions were introduced, which describe the characteristics of scaled devices in all regions of circuit operation. With

the increase in the complexities of MOS devices and technologies, compact MOS models based on surface potential and inversion charge started to emerge, especially to fulfil the increasing demands for analog and digital applications. These physics-based emerging models promise to simulate nano-MOSFET device characteristics in both digital and analog ICs. The accuracy, predictability, and longevity of these emerging models to meet the design challenges of MOS ICs down to 10 nm regimes are still to be seen. Finally, the motivation for compact modeling, the usage of compact models, and model standardization are briefly discussed.

Exercises

1.1 Double gate and multiple gate thin-body FETs like FinFETs and UTB-SOI FETs have emerged as the alternative devices to planar MOSFETs for advanced VLSI circuits. Write a brief history of the compact modeling of multiple gate FETs.

1.2 Write a brief history of compact modeling of the emerging devices including tunnel FETs as the potential alternative to next generation devices for VLSI circuits.