4

Large Geometry MOSFET Compact Models

4.1 Introduction

In the two-terminal MOS (metal-oxide-semiconductor) capacitor system in Chapter 3, we have discussed that an inversion condition can be reached by a certain applied gate bias to form a thin layer of minority carrier concentration (e.g., electron) in the majority carrier (e.g., *p*-type) silicon surface at the silicon/SiO_2 interface. Under this inversion condition, the thermally generated minority carriers diffuse to the surface to form the inversion layer in the majority carrier substrate. However, it is difficult to sustain this minority carrier inversion layer in a majority carrier substrate from thermal generation and subsequent diffusion of these carriers to the surface without a steady source of carrier supply. Therefore, a heavily doped minority carrier region (e.g., *n*+ region in a *p*-type substrate), called the *source* (s), is added to the MOS structure as a terminal for the steady supply of minority carriers at the inversion condition. And, a complete MOSFET (metal-oxide-semiconductor field-effect transistor) structure is formed by adding one more terminal, called the *drain* (d), with a heavily doped region with the doping-type same as the source region. These source and drain terminals contact the two opposite ends of the inversion layer so that a potential difference can be applied across this layer and cause a current flow in the MOSFET structure. In this chapter, we will develop the basic mathematical models of this current flow from the source to drain of MOSFET devices, referred to as the *drain current model*.

Since the conception of MOSFETs in 1920s [1], there has been a continuous research and development effort on MOSFET device, technology, and modeling [2–5]. As stated in Chapter 1, the basic theory of MOSFETs has been developed in 1960s. In 1970s, complementary MOS (CMOS) technology with MOSFET devices became the pervasive technology of mainstream VLSI (very-large-scale-integrated) circuits. In the last five decades, there has been a relentless pursuit of developing MOSFET compact models that accurately simulate the experimental behavior of MOSFET devices in VLSI circuits. In this chapter, we will present the basic MOSFET drain current models for large geometry devices to lay the foundation for the understanding of

advanced industry standard models for circuit computer-aided design (CAD). Our objective is to determine the drain current for any combination of DC voltages. First of all, we will present a brief overview of the basic MOSFET structure as used in VLSI technology, its features and behavior under operating biases, and the basic theory of MOSFET device operation and characteristics. One of the most important physical parameters of MOSFET device operation is the threshold voltage, V_{th}, defined as the gate voltage at which the device starts to turn on. In this chapter, we will develop the basic theory of V_{th} modeling for long channel devices. Throughout this chapter we will assume that the channel is sufficiently *long* and *wide*, so that the edge effects are negligibly small. Unless stated otherwise, we will also assume that the substrate is uniformly doped *p*-type silicon. We will introduce the relevant basic drain current models in a systematic way, deriving them from an important model and relating them to the source and to each other. Before, describing large geometry model, we first present a brief overview of MOSFET device architecture for better appreciation of MOSFET compact models.

4.2 Overview of MOSFET Devices

An ideal MOSFET device structure is shown in Figure 4.1 and a 2D (two-dimensional) cross section is shown in Figure 4.2. The structure includes a semiconductor substrate such as silicon on which a thin insulating layer such as SiO_2 of thickness T_{ox} is grown. A conducting layer (a metal or degenerately doped polycrystalline silicon) called gate electrode is deposited on the top of the gate oxide. Two heavily doped regions of depth X_j, called the source and drain, are formed in the substrate on either side of the gate. The source and drain regions overlap with the gate at its two ends. The source-to-drain regions are equivalent to two back-to-back *pn*-junctions. This region between the source and drain near the silicon surface is called the *channel region*. Thus, in essence, a MOSFET is essentially an MOS capacitor with two back-to-bask *pn*-junctions at the two ends of the gate. In advanced VLSI circuits, NMOS (*p*-type body with *n*+ source-drain) and PMOS (*n*-type body with *p*+ source-drain) are fabricated together using shallow trench isolation (STI) and is called the CMOS transistor. Thus, the STI shown in Figure 4.2 is used to isolate various devices fabricated on the same substrate. For device operation, a MOSFET is a four-terminal device with *gate g*, *source s*, *drain d*, and *substrate or body b*. The device is symmetrical and cannot be distinguished without the applied bias. The body terminal allows to modulating the inversion layer from the gate as well as body to offer more flexibility of devices at circuit operation.

As shown in Figure 4.1, a MOSFET device is characterized by channel length *L*, channel width *W*, gate oxide with thickness T_{ox}, substrate doping N_b, and source-drain with junction depth X_j. In advanced VLSI circuits, NMOS (*p*-type body with *n*+ source-drain) and PMOS (*n*-type body with *p*+ source-drain) are used together and is called the complementary MOS transistor.

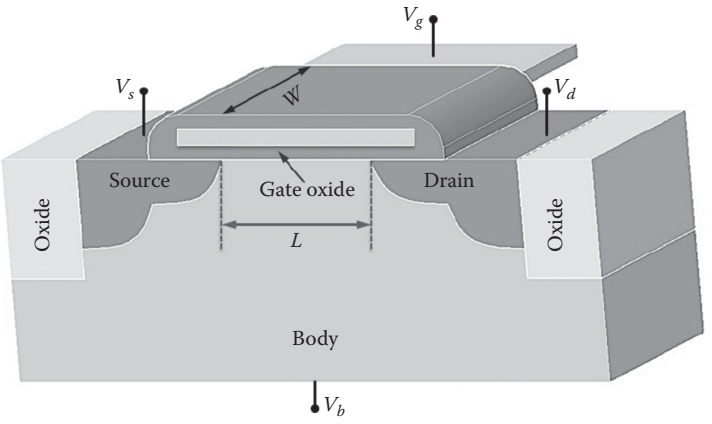

FIGURE 4.1
An ideal structure of a four-terminal MOSFET device; here V_g, V_s, V_d, and V_b are the gate, source, drain, and body terminals, respectively; and W and L are the channel width and channel length of the device, respectively.

4.2.1 Basic Features of MOSFET Devices

A 2D cross section of an advanced CMOSFET (CMOS field-effect transistor) structure along with its basic technology parameters is shown in Figure 4.2 [6]. It is observed from Figure 4.2 that the basic device engineering includes: (1) gate engineering to integrate dual-polysilicon (degenerately doped *n*+ and *p*+) gates or work function engineering for metal gate, (2) channel engineering with *p*-type and *n*-type well implants as well as threshold-voltage adjust implants

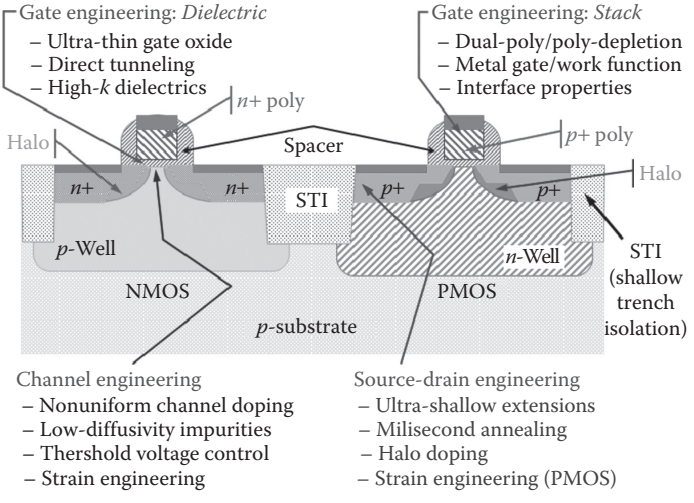

FIGURE 4.2
A typical 2D-cross section of an ideal advanced CMOS device showing major technology elements.

with impurities same as the well type, (3) halo implants with impurities same as the well type, and (4) source-drain (S/D) engineering to implant S/D with impurities opposite to the well-type. The channel engineering with V_{th} adjust implant produces vertically nonuniform channel doping profile and S/D engineering with halo implants produces laterally nonuniform channel doping profile in advanced bulk MOSFET devices [7–11].

A MOSFET structure shown in Figures 4.1 and 4.2 can be characterized by different circuit elements and current flow between source-drain terminals as shown in Figure 4.3. Figure 4.3a shows that a MOSFET structure includes parasitic source, drain, and gate resistances R_s, R_d, and R_g, respectively; and parasitic *pn*-junctions from body to source and from body to drain [12]. Figure 4.3b shows the small signal capacitances associated with a MOSFET structure. The capacitances include intrinsic source, drain, and body capacitances C_{GS}, C_{GD}, and C_{GB}, respectively, with reference to source and the extrinsic gate overlap capacitances C_{GSO}, C_{GDO}, and C_{GBO} with source, drain, and body, respectively, with reference to the gate and the junction capacitances C_{jS} and C_{jD} due to body to source and body to drain *pn*-junctions, respectively, as shown in Figure 4.3b [13].

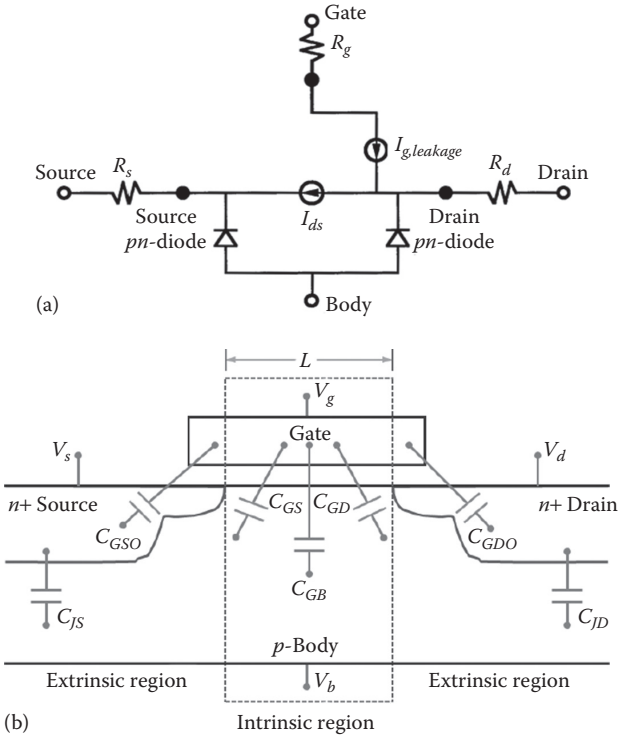

FIGURE 4.3
Basic features of MOSFETs: (a) basic circuit elements and current flows and (b) intrinsic and extrinsic parasitic capacitance elements.

4.2.2 MOSFET Device Operation

A MOSFET device has three modes of operation such as *accumulation*, *depletion*, and *inversion* similar to an MOS capacitor system. Therefore, the theory developed for an MOS capacitor system can be directly extended to MOSFETs by considering the channel potential due to the lateral electric field from the source to drain terminals of the structure shown in Figure 4.1.

In conventional MOSFET device operation, the source is used as the reference terminal with bias $V_s = 0$ and a drain voltage V_{ds} with reference to the source is applied to the drain so that the S/D *pn*-junctions are reverse biased. Under this biasing condition, the body or substrate current, $I_{bs} = 0$, and the gate current, $I_{gs} = 0$. The gate bias, V_{gs}, controls the surface carrier densities. A certain value of V_{gs}, referred to as the threshold voltage (V_{th}), is required to create the channel *inversion layer*. The parameter, V_{th} is determined by the properties of the structure. Thus, with reference to source potential,

- For $V_{gs} < V_{th}$, the MOSFET structure consists of two back-to-back *pn*-junctions and only leakage currents (~I_o of S/D *pn*-junctions) flow from source to drain of the device, that is, $I_{ds} \sim 0$;
- For $V_{gs} > V_{th}$, an inversion layer exists, that is, a conducting channel exists from the drain to source of the device and a drain current I_{ds} will flow.

The body or bulk terminal allows modulating the inversion layer from the bottom by body bias, V_{bs}, as well as from the top by V_{gs} to offer more flexibility of devices at circuit operation. In normal MOSFET operation, V_{bs} is applied to reverse bias the source-drain *pn*-junctions.

4.3 MOSFET Threshold Voltage Model

All MOS capacitor equations derived in Chapter 3 are valid for large L and large W MOSFETs with proper consideration of the lateral electric field, E_y, due to the applied drain bias, V_{ds}, as shown in Figure 4.4.

Let us consider the source potential $V_s = 0$ as the reference voltage for MOSFETs. Due to the applied V_{ds}, the surface potential, ϕ_s, is a function of location, y, along the channel such that $\phi_s = \phi_s(y)$. Therefore, a channel potential, $V_{ch}(y)$, exists along the channel from the source to drain such that

$$V_{ch}(y) = \begin{cases} V_{sb}; & \text{at } y = 0 \\ V_{sb} + V_{ds}; & \text{at } y = L \end{cases} \tag{4.1}$$

Similar to an MOS capacitor, a MOSFET V_{th} model is obtained by solving Poisson's equation relating the charge density, ρ, to the electrostatic potential ϕ (or, electric field E) given by

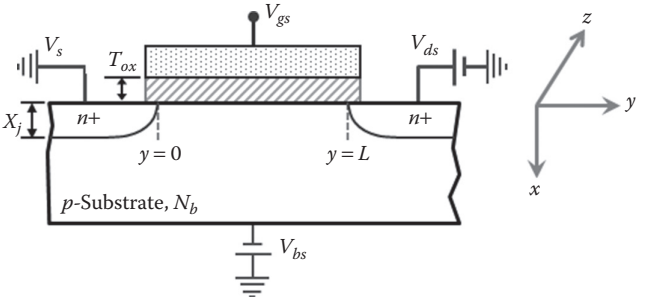

FIGURE 4.4
Schematic 2D cross section of an *n*-channel MOSFET showing the biasing conditions and the coordinate system; *x*, *y*, and *z* represent the distances along the depth, length, and width of the device, respectively.

$$\nabla^2\phi = -\frac{\rho}{K_{si}\varepsilon_0} \tag{4.2}$$

Generally, a MOSFET is a 3D (three-dimensional) problem; however, for all practical purposes (except for very small *W* and *L*), we can treat the system as a 2D problem in the *x* and *y* directions only. We can further convert the 2D problem to 1D (one-dimensional) by a set of simplifying assumptions. First of all, we assume that the variation of the electrical field E_y in the *y* direction along the channel is much less than the corresponding variation of the electrical field E_x in the *x* direction down to the substrate. Then we have

$$\frac{\partial E_y}{\partial y} << \frac{\partial E_x}{\partial x}; \quad \therefore \frac{\partial^2\phi}{\partial y^2} << \frac{\partial^2\phi}{\partial x^2} \tag{4.3}$$

Equation 4.3 is referred to as the *gradual channel approximation* (GCA) [2]. Therefore, like an MOS capacitor, we solve for ϕ in the *x* direction along the depth of the channel only to obtain the total charge, Q_s, in the semiconductor. For MOSFETs in *inversion* ($\phi_B < \phi_s < 2\phi_B$), the total charge $Q_s = Q_s(y)$ due to the channel potential $V_{ch}(y)$ can be derived from the MOS capacitor theory (Equation 3.52). In Equation 3.52, we observe that for $\phi_s > 0$, $\exp(-\phi_s/v_{kT})$ is negligibly small, the term "–1" is negligibly small since $\exp(\phi_s/v_{kT}) >> -1$ in strong inversion, and the term $(-\phi_s/v_{kT})$ is negligibly small in weak inversion. Therefore, from Equation 3.52, $Q_s(y)$ for MOSFETs at inversion can be shown as

$$\begin{aligned} Q_s(y) &= -\sqrt{2K_{si}\varepsilon_0 qN_b}\left[\phi_s(y) + v_{kT}\frac{n_i^2}{N_b^2}\left(e^{(\phi_s(y)-V_{ch}(y))/v_{kT}}\right)\right]^{1/2} \\ &= -\sqrt{2K_{si}\varepsilon_0 qN_b}\left[\phi_s(y) + v_{kT}\left(e^{(\phi_s(y)-2\phi_B-V_{ch}(y))/v_{kT}}\right)\right]^{1/2} \\ &= -\sqrt{2K_{si}\varepsilon_0 qN_b}\, f\left(\phi_s(y), \phi_B, V_{ch}(y)\right) \end{aligned} \tag{4.4}$$

where we have used $n_i^2/N_b^2 = \exp\left(-2\phi_B/v_{kT}\right)$ from Equation 3.41, and defined

$$f\left(\phi_s(y), \phi_B, V_{ch}(y)\right) \equiv \left[\phi_s(y) + v_{kT}\left(e^{\left(\phi_s(y)-2\phi_B-V_{ch}(y)\right)/v_{kT}}\right)\right]^{1/2} \tag{4.5}$$

Now, from Equation 3.23, the gate voltage V_{gb} with reference to bulk can be represented as

$$V_{gb} = V_{fb} + \phi_s(y) - \frac{Q_s(y)}{C_{ox}} \tag{4.6}$$

Substituting for $Q_s(y)$ from Equation 4.4 to Equation 4.6, we can show

$$V_{gb} = V_{fb} + \phi_s(y) + \frac{\sqrt{2K_{si}\varepsilon_0 q N_b}}{C_{ox}}\left[\phi_s(y) + v_{kT}e^{\left(\left(\phi_s(y)-2\phi_B-V_{ch}(y)\right)/v_{kT}\right.}\right]^{1/2} \tag{4.7}$$

Conventionally, *strong inversion* is defined at $\phi_s = 2\phi_B$. Therefore, assuming $V_{ds} \cong 0$, we get from Equation 4.1, $V_{ch}(y) \cong V_{sb}$. Then the surface potential, $\phi_s(y)$, at strong inversion due to V_{sb} is a constant along the channel and is given by

$$\phi_s(y) = \phi_s = 2\phi_B + V_{sb} \tag{4.8}$$

Thus, under the condition $V_{ds} \cong 0$, substituting for $\phi_s(y)$ from Equation 4.8 and $V_{ch}(y) = V_{sb}$ in Equation 4.4, we get:

$$\begin{aligned} Q_s(y) &= -\sqrt{2K_{si}\varepsilon_0 q N_b}\left[\left(2\phi_B + V_{sb}\right) + v_{kT}\left(e^{\left((2\phi_B+V_{sb})-2\phi_B-V_{sb}\right)/v_{kT}}\right)\right]^{1/2} \\ &\cong -\sqrt{2K_{si}\varepsilon_0 q N_b\left(2\phi_B + V_{sb}\right)} \end{aligned} \tag{4.9}$$

Now, substituting for $Q_s(y)$ from Equation 4.9 to Equation 4.6, we get

$$\begin{aligned} V_{th} = V_{gb} &= V_{fb} + 2\phi_B + \frac{\sqrt{2K_{si}\varepsilon_0 q N_b}}{C_{ox}}\sqrt{\left(2\phi_B + V_{sb}\right)} \\ &= V_{fb} + 2\phi_B + \gamma\sqrt{\left(2\phi_B + V_{sb}\right)} \end{aligned} \tag{4.10}$$

where the parameter γ strongly depends on channel doping concentration and called the *body factor* given by

$$\gamma = \frac{\sqrt{2K_{si}\varepsilon_0 q N_b}}{C_{ox}} \tag{4.11}$$

Thus, from Equation 4.10, the threshold voltage for long channel devices is given by

$$V_{th} = V_{fb} + 2\phi_B + \gamma\sqrt{\left(2\phi_B + V_{sb}\right)} \tag{4.12}$$

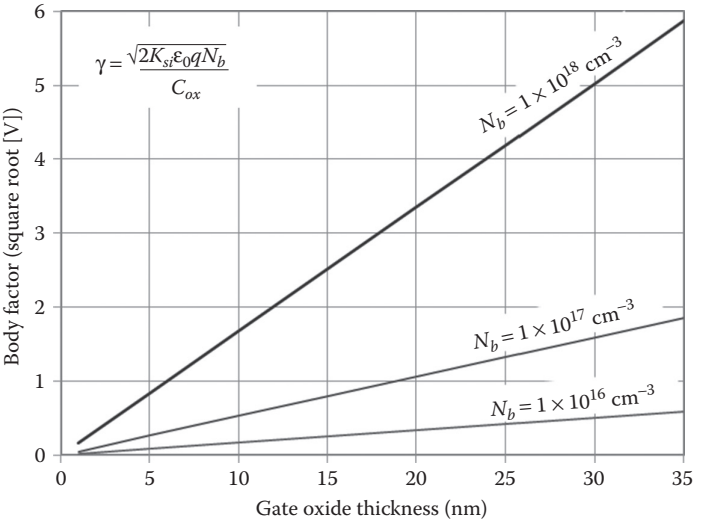

FIGURE 4.5
Effect of gate oxide thickness T_{ox} and channel concentration N_b on body coefficient of long channel MOSFETs.

where from Equation 3.15, $V_{fb} = \phi_{ms} - Q_o/C_{ox}$. Now, if the body bias $V_{bs} = V_{sb} = 0$, then from Equation 4.12, the threshold voltage without body bias is given by

$$V_{th0} = V_{fb} + 2\phi_B + \gamma\sqrt{2\phi_B} \tag{4.13}$$

Combining Equations 4.12 and 4.13, we get the expression for threshold voltage at any biasing condition as

$$V_{th} = V_{th0} + \gamma\left(\sqrt{(2\phi_B + V_{sb})} - \sqrt{2\phi_B}\right) \tag{4.14}$$

Equation 4.14 is the general expression for V_{th} of MOSFETs in inversion condition. The body effect parameter γ depends on the gate oxide thickness and channel doping concentration. Figure 4.5 shows the effect of T_{ox} and N_b on γ.

4.4 MOSFET Drain Current Model

In order to obtain the device characteristics of MOSFETs, let us consider an *n*-channel MOSFET (nMOSFET) device with uniformly doped substrate concentration N_b (cm^{-3}), the structure and dimensions of which are shown in Figure 4.6. For the sake of simplicity we will assume this to be a large

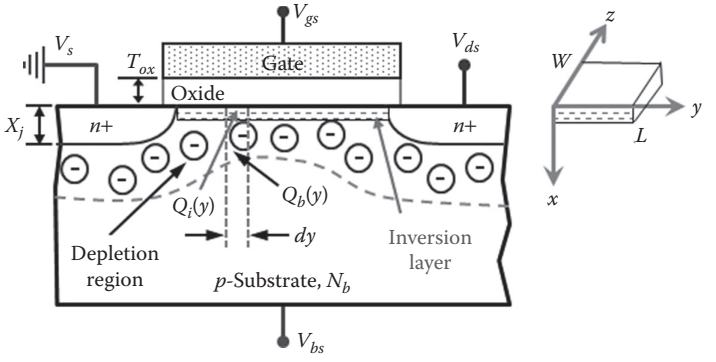

FIGURE 4.6
Schematic of an *n*MOSFET device showing different biases and reference direction; *x*, *y*, and *z* distance into the silicon, along the channel, and along the channel width of the device, respectively.

geometry device so that the short channel and narrow width effects can be neglected. We will develop a generalized large geometry MOSFET drain current model using several simplifying assumptions.

4.4.1 Drain Current Formulation

In general, the static and dynamic characteristics of a semiconductor device under the influence of external fields can be described by the following three sets of coupled differential equations

1. The Poisson's equation for electrostatic potential ϕ is described in Equation 4.2 and is given by

$$\nabla^2\phi = -\frac{\rho}{K_{si}\varepsilon_0} \tag{4.15}$$

   where:
   ρ is the charge density
   K_{si} is the dielectric constant of silicon
   ε_0 is the permittivity of free space
2. The *current density* equations for electron current density (J_n) and hole current density (J_p),

$$\begin{aligned} J_n &= q\mu_n nE + qD_n\nabla n \quad \text{(electrons)} \\ J_p &= q\mu_p pE - qD_p\nabla p \quad \text{(holes)} \end{aligned} \tag{4.16}$$

   Equation 4.16 under nonequilibrium condition is represented by

$$\begin{aligned} J_n &= -qn\mu_n\nabla\phi_n \quad \text{(electrons)} \\ J_p &= -qp\mu_p\nabla\phi_p \quad \text{(holes)} \end{aligned} \tag{4.17}$$

where:

n and p represent the electron and hole concentrations, respectively
q is the electronic charge
E is the electric field
ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials, respectively, in nonequilibrium condition
μ_n and μ_p are the electron and hole mobilities, respectively.

The total current density (J) flowing through the device is given by $J = J_n + J_p$.

3. The *current continuity* equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n - R_n + G_n \quad \text{(electrons)}$$
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot J_n - R_p + G_p \quad \text{(holes)} \tag{4.18}$$

In Equation 4.18, G_n and G_p are the generation rates for electrons and holes, respectively, whereas R_n and R_p represent the recombination rates for electrons and holes, respectively.

As pointed out in Section 4.3, modeling of a MOSFET device is a 3D problem; however, for all practical purposes (except for small geometry devices), we can treat a MOSFET device as a 2D problem in the x and y directions only (Figure 4.6). Even as a 2D problem, the mathematical expressions are fairly complex and can only be solved exactly using numerical techniques used in 2D/3D device simulators including MEDICI [14], MINIMOS [15], Sentaurus Device [16], and ATLAS [17]. However, in order to obtain simplified analytical solutions for circuit CAD, we make a number of valid simplifying assumptions to develop compact device equations that accurately describe the behavior of semiconductor devices in circuit operation.

Now, we make a number of valid simplifying assumptions to develop a generalized expression for drain current, I_{ds}, of large geometry MOSFETs on a uniformly doped substrate as described below:

Assumption 1: We assume that the variation of the electric field E_y in the y direction (along the channel) is much less than the corresponding variation of the electric field E_x in the x direction into the substrate. Thus, as discussed in Section 4.3, here again, we assume GCA [2] so that we need to solve only 1D Poisson's equation described in Equation 2.58, which is given by

$$\frac{d^2\phi}{dx^2} = -\frac{\rho(x)}{K_{si}\varepsilon_0} \tag{4.19}$$

2D numerical analysis shows that the GCA is valid for most of the channel length except near the drain end of the channel region. Near the drain end of the channel, the longitudinal electric field E_y is comparable to the transverse electric field E_x even for long channel devices and GCA breaks down. In spite of its failure near the drain end, the GCA is used as it reduces the system to a 1D current flow problem. The fact that we have to solve only a 1D Poisson's equation means that the charge expressions developed in Chapter 3 for an MOS capacitor system could be used for an MOS transistor, with the modification that charge and potential will now be position dependent in the y direction.

Assumption 2: Assume that only minority carriers contribute to I_{ds}; for example, for an nMOSFET device, the hole current can be neglected. In nMOSFETs, the majority carrier holes are created by impact ionization and become important in describing the device characteristics in the avalanche or breakdown regime. However, in the normal operation range of MOSFET devices, the drain current does not include breakdown regime, and therefore, the assumption that the current in MOSFETs is due to the minority carriers is valid under the normal biasing conditions, for example, for nMOSFETs $V_{ds} \geq 0$ and $V_{bs} \leq 0$. Thus, the drain current model needs to consider only the minority carrier current density, J_n, for nMOSFET devices.

Assumption 3: Assume there are no generation and recombination of carriers, that is, for an nMOSFET device $R_n = 0 = G_n$. Then considering only the static characteristics of the device, the continuity equation 4.18 becomes

$$\nabla \cdot J_n = 0 \tag{4.20}$$

This implies that the total drain current I_{ds} is a constant at any point along the channel of the device.

Assumption 4: Assume that the current flows in the y direction along the channel only, that is, $d\phi_n/dx = 0$. Thus, the electron quasi-Fermi potential, ϕ_n, is a constant in the x direction. Then from Equation 4.17, the electron current density is given by

$$J_n(x,y) = -qn(x,y)\mu_n(x,y)\frac{\partial \phi_n}{\partial y} \tag{4.21}$$

Since the cross-sectional area of the channel in which the current flows is the channel width, W, times the channel length, L, integrating Equation 4.21 across the depth x and width z, we get I_{ds} at any point y in the channel as

$$I_{ds}(y) = -W\int_0^{\infty}\left[qn(x,y)\mu_n(x,y)\frac{\partial\phi_n}{\partial y}\right]dx = \text{constant} \tag{4.22}$$

where μ_n in Equation 4.22 is the channel electron surface mobility for nMOSFETs, often referred to as the surface mobility μ_s in order to distinguish it from the bulk mobility deep into the substrate described in Section 2.2.5.1. In the rest of the discussion, we will replace μ_n by μ_s to emphasize that the inversion layer mobility we deal with for MOSFET devices is the surface mobility.

In MOSFET devices, the application of source and drain voltages relative to the substrate results in a lowering of the quasi-Fermi level F_n (or potential ϕ_n) at the source end of the device by an amount qV_{sb}, and the drain end of the device by an amount $q(V_{sb} + V_{ds})$, relative to equilibrium Fermi level E_f in the substrate. It is this difference in ϕ_n between the source and drain that drives the electrons down the channel. Now, the channel potential $V_{ch}(y)$ at any point y in the channel in Figure 4.7 is given by

$$V_{ch}(y) = \phi_n(y) - \phi_n\big|_{\text{source}} \tag{4.23}$$

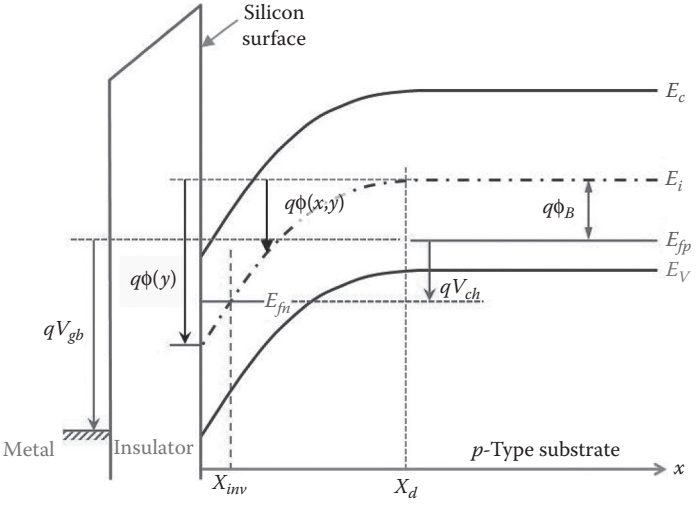

FIGURE 4.7
Energy band diagram of an nMOSFET device shown in Figure 4.6; E_c, E_v, and E_i represent the bottom of the conduction band, top of the valence band, and intrinsic band, respectively, of the p-type substrate; E_{fn} and E_{fp} are the quasi-Fermi level of electrons and holes, respectively; qV_{ch} is the channel potential due to the difference in $E_{fn} - E_{fp}$ caused by the difference in source and drain potentials.

At the source end of the channel, $V_{ch}(0) = 0$, and at the drain-end of the channel, $V_{ch}(L) = (V_{sb} + V_{ds})$. Thus, compared to the case of an MOS capacitor, the quasi-Fermi potential is lowered by an amount $V_{ch}(y)$ at the surface region of a MOSFET device. As a result, the surface electron concentration (n_s) is lowered by a factor $\exp(-V_{ch}(y)/v_{kT})$. Then following the derivation of minority carrier density expression (Equation 3.42) for an MOS capacitor, we can write the minority carrier surface electron concentration at any point y in a MOSFET device as

$$n(y) = N_b \exp\left[\frac{\phi(y) - 2\phi_B - V_{ch}(y)}{v_{kT}}\right] \tag{4.24}$$

where the parameters have their usual meanings as defined in Section 3.4.1. The minority carrier concentration changes due to the applied bias; however, the majority carrier hole concentration does not change with bias, and therefore, following MOS capacitor Equation 3.39, we can write for the majority carrier concentration in MOSFETs as $p = N_b \exp[(-\phi(y)/v_{kT}]$.

Then using Equation 4.23, Equation 4.22 can be written as:

$$I_{ds}(y) = -W\frac{dV_{ch}(y)}{dy}\int_0^{\infty} qn(x,y)\mu_s(x,y)dx \tag{4.25}$$

Assumption 5: For the simplicity of long channel I_{ds} calculation, we assume μ_s = constant at some average gate and drain electric field; however, μ_s depends on both E_x and E_y, as we will discuss in Chapter 5. With this assumption, we can write Equation 4.25 as:

$$I_{ds}(y) = -W\mu_s\frac{dV_{ch}(y)}{dy}\int_0^{\infty} qn(x,y)dx \tag{4.26}$$

Now, we define Q_i as the mobile minority carrier charge density, that is

$$Q_i(y) = -q\int_0^{\infty} n(x,y)dx \tag{4.27}$$

Using Equation 4.27 in Equation 4.26, we get the general expression for $I_{ds}(y)$ as

$$I_{ds}(y)dy = W\mu_s Q_i(y)dV_{ch}(y) \tag{4.28}$$

Again, assuming GCA is valid along the entire length of the channel, we get after integrating Equation 4.28 along the channel length from $y = 0$ to $y = L$

$$I_{ds} = \mu_s \left(\frac{W}{L} \right) \int_{V_{sb}}^{V_{sb}+V_{ds}} Q_i(y) dV_{ch} \tag{4.29}$$

Equation 4.29 is the general expression for I_{ds} flowing through a MOSFET device. In order to calculate I_{ds}, we need to calculate the mobile inversion charge density $Q_i(y)$ in the channel region. A number of I_{ds} models have been developed depending on different approaches to compute $Q_i(y)$. We will discuss some of the early generation of compact models in the following section to appreciate the rigor of the advanced industry standard compact models.

4.4.2 Pao-Sah Model

In this model, $Q_i(y)$ is calculated numerically by integrating the electron concentration in the x direction. In order to evaluate $Q_i(y)$, let us change the variable of integration in Equation 4.27 from x to ϕ and integrate from $\phi(x = 0) = \phi_s$ to $\phi(x = \infty) = \phi_B$ so that

$$Q_i(y) = -q \int_0^{\infty} n(x, y) dx = -q \int_{\phi_s}^{\phi_B} n\left(\phi, V_{ch}(y)\right) \frac{dx}{d\phi} d\phi \tag{4.30}$$

where:

ϕ_s is the surface potential (at $x = 0$) and is position dependent due the applied voltage between the source and drain

Since the inversion layer is formed when the minority carrier concentration exceeds the majority carrier concentration, that is, $\phi \geq \phi_B$, the upper limit of integration is ϕ_B where the inversion layer ends. In Equation 4.30, $(d\phi/dx)^{-1} = -1/E_x$, where E_x is the vertical electric field along the depth of the channel. In order to obtain $Q_i(y)$ from Equation 4.30, we need to determine the electron concentration along the channel $n\left(\phi, V_{ch}(y)\right)$ and the variation of potential representing the inverse of the vertical electric field $(d\phi/dx)^{-1} = -1/E_x$ along the depth of the channel.

Derivation of $n(\phi, V_{ch}(y))$: As pointed out earlier, we can use MOS capacitor equation with appropriate modification to include the channel potential $V_{ch}(y)$ to account for the applied drain bias in MOSFETs. Therefore, considering the channel potential, $V_{ch}(y)$, due to the applied V_{ds} in Equation 3.42, we can write the expression for the inversion carrier at a point y along the channel as

$$n(y) = N_b e^{\left(\phi(y) - 2\phi_B - V_{ch}(y)\right)/v_{kT}} \equiv n\left(\phi, V_{ch}(y)\right) \tag{4.31}$$

Derivation of $(d\phi/dx)^{-1}$: From Gauss's law given in Equation 2.61, the total induced charge in the p-type semiconductor of an nMOSFET device is given by

$$Q_s = -\varepsilon_0 K_{si} E_s = \varepsilon_0 K_{si}\left(\frac{d\phi}{dx}\right)$$
$$\therefore \left(\frac{d\phi}{dx}\right) = \frac{Q_s}{\varepsilon_0 K_{si}} \tag{4.32}$$

where we have used $E_s = -\left(d\phi/dx\right)$ in Equation 4.32. Again, repeating Equation 4.4 for $Q_s(y)$ of an nMOSFET device, we get

$$Q_s(y) = -\sqrt{2K_{si}\varepsilon_0 q N_b}\, f\left(\phi_s(y), \phi_B, V_{ch}(y)\right) \tag{4.33}$$

Combining Equations 4.32 and 4.33, we get

$$\frac{d\phi}{dx} = -\sqrt{\frac{2qN_b}{K_{si}\varepsilon_0}}\, f\left(\phi_s, \phi_B, V_{ch}(y)\right) \tag{4.34}$$

Now, substituting for $n(\phi, V_{ch}(y))$ and $(d\phi/\mathrm{dx})^{-1}$ from Equations 4.31 and 4.34, respectively, into Equation 4.30, we can show

$$Q_i(y) = \sqrt{\frac{K_{si}\varepsilon_0 N_b q}{2}} \int_{\phi_s}^{\phi_B} \frac{e^{[\phi(y)-2\phi_B - V_{ch}(y)]/v_{kT}}}{f\left(\phi_s, \phi_B, V_{ch}(y)\right)} d\phi \tag{4.35}$$

Equation 4.35 is the generalized expression for the inversion charge $Q_i(y)$ in a MOSFET device. Then substituting for $Q_i(y)$ from Equation 4.35 to Equation 4.29, we get the expression for the drain current as

$$I_{ds} = \mu_s \frac{W}{2L} C_{ox}\gamma \int_{V_{sb}}^{V_{sb}+V_{ds}} \int_{\phi_s}^{\phi_B} \frac{e^{[\phi(y)-2\phi_B - V_{ch}(y)]/v_{kT}}}{f\left(\phi_s, \phi_B, V_{ch}(y)\right)} d\phi dV_{ch} \tag{4.36}$$

In Equation 4.36, we have used $\gamma = \sqrt{2qK_{si}\varepsilon_0 N_b}\,/C_{ox}$ and γ is defined in Equation 4.11 as the body effect coefficient. Equation 4.36 was fist derived by Pao and Sah [2] and is called the *Pao-Sah* or *double integral* model for MOSFET devices. Equation 4.36 can only be solved numerically using ϕ_s from Equation 4.7 given by

$$V_{gb} = V_{fb} + \phi_s(y) + \gamma\left[\phi_s(y) + v_{kT} e^{\left[(\phi_s(y)-2\phi_B - V_{ch}(y)\right]/v_{kT}}\right]^{1/2} \tag{4.37}$$

As we can see Equation 4.37 is an implicit equation in ϕ_s and must be solved for a given bias condition using an iterative procedure. The Pao-Sah model given by Equation 4.36 provides a unified description of both the drift and diffusion components of I_{ds} and is valid in all regions of a MOSFET device operation. However, due to long computation time to generate *I–V* characteristics by solving double numerical integration along with the iterative solution of ϕ_s at each bias point, the model is too complex and unsuitable for

circuit CAD. Therefore, various simplifications of Pao-Sah model have been used to develop computationally efficient compact models suitable for circuit analysis [3–5,12–22]. Pao-Sah model is used to benchmark the accuracy of other simplified models.

4.4.3 Charge-Sheet Model

In order to derive an accurate and simplified I_{ds} model from the generalized Equation 4.29, let us assume that the inversion layer is a sheet of charge without any finite thickness. Then assuming that the depletion approximation is valid, we can show from Equation 3.64 that the induced depletion charge in terms of the body factor γ is given by

$$Q_b(y) = -\gamma C_{ox}\sqrt{\phi_s(y)} \tag{4.38}$$

Again, from Equation 4.6, the expression for the total charge in the semiconductor is given by

$$Q_s(y) = -C_{ox}\left[V_{gb} - V_{fb} - \phi_s(y)\right] \tag{4.39}$$

We know that $Q_i(y) = Q_s(y) - Q_b(y)$; therefore, from Equations 4.38 and 4.39, the expression for the sheet of inversion charge with zero thickness is given by

$$Q_i(y) = -C_{ox}\left[V_{gb} - V_{fb} - \phi_s(y) - \gamma\sqrt{\phi_s(y)}\right] \tag{4.40}$$

Rearranging Equation 4.28, using Equations 4.38 and 4.40, Brews [5] showed that the total drain current can be expressed as

$$\begin{aligned} I_{ds}(y) &= -\mu_s W\left[Q_i(y)\frac{d\phi_s}{dy} - v_{kT}\frac{dQ_i(y)}{dy}\right] \\ &= I_{ds1}(y) + I_{ds2}(y) \end{aligned} \tag{4.41}$$

where I_{ds1} and I_{ds2} are given by

$$\begin{aligned} I_{ds1}(y) &= -\mu_s W Q_i(y)\frac{d\phi_s}{dy} \\ I_{ds2}(y) &= \mu_s W v_{kT}\frac{dQ_i}{dy} \end{aligned} \tag{4.42}$$

We know that under the lateral electric field $E(y)$ from the source to drain along the channel, the electrons move with a drift velocity v_d and the drain current due to drift of electrons is given by

$$I_{ds}(\text{drift}) = W\left(J_{\text{drift}}\right) = W\left(nqv_d\right) = WQ_i\mu_s E(y) = -WQ_i\mu_s\frac{d\phi_s}{dy} = I_{ds1} \tag{4.43}$$

where n is the inversion layer electron concentration for nMOSFETs, q is the electronic charge so that $Q_i = nq$ and $v_d = \mu_s E(y) = -\mu_s(d\phi_s/dy)$.

Again, if the electron transport is due to the concentration gradient (dn/dy) along the channel, then from Fick's first law of diffusion (Equation 2.39), the electron diffusion current along the channel is given by

$$I_{ds}\left(\text{diffusion}\right)=W\left(J_{\text{diffusion}}\right)=W\left(qD_n\frac{dn}{dy}\right)=qW\left(v_{kT}\mu_s\right)\frac{dn}{dy}=W\mu_s v_{kT}\frac{dQ_i}{dy}=I_{ds2} \tag{4.44}$$

where we have used Einstein's relation $D_n/\mu_s = kT/q = v_{kT}$. Thus, we find that the total drain current in a MOSFET device is the sum of the drift and diffusion components I_{ds1} and I_{ds2} as given by Equations 4.43 and 4.44, respectively. In general, I_{ds1} and I_{ds2} are coupled differential equations and cannot be integrated separately. However, for simplicity of compact device modeling, we solve each component separately under the appropriate boundary conditions and add them together to obtain the expression for the total drain current I_{ds}.

4.4.3.1 Drift Component of Drain Current

Substituting for Q_i from Equation 4.40 to Equation 4.43, we get for the drift component of the drain current as

$$I_{ds1}(y) = \mu_s WC_{ox}\left[V_{gb} - V_{fb} - \phi_s(y) - \gamma\sqrt{\phi_s(y)}\right]\frac{d\phi_s(y)}{dy} \tag{4.45}$$

In order to solve Equation 4.45, we use the boundary condition

$$\phi_s(y) = \begin{cases} \phi_{s0} & \text{at } y = 0 \\ \phi_{sL} & \text{at } y = L \end{cases} \tag{4.46}$$

where:

ϕ_{s0} and ϕ_{sL} represent the surface potential at the source end and at the drain end of the channel, respectively, as shown in Figure 4.8

Therefore, using the boundary condition from Equation 4.46, we get from Equation 4.45

$$\int_0^L I_{ds1}(y)dy = \mu_s WC_{ox}\int_{\phi_{s0}}^{\phi_{sL}}\left[V_{gb} - V_{fb} - \phi_s(y) - \gamma\sqrt{\phi_s(y)}\right]d\phi_s(y) \tag{4.47}$$

After integration and simplification, we get the drift component of the drain current in MOSFETs as

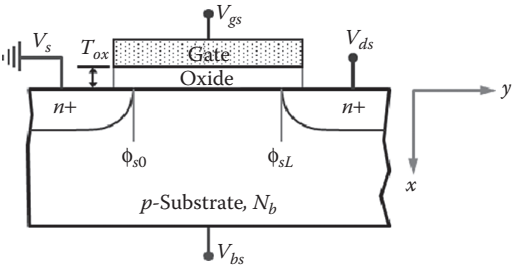

FIGURE 4.8
MOSFET device structure showing the boundary conditions to solve current equations for the drift and diffusion components of the drain currents; ϕ_{s0} and ϕ_{sL} are the surface potentials at the source end ($y = 0$) and drain end ($y = L$) of the channel, respectively.

$$I_{ds1} = \mu_s C_{ox} \frac{W}{L}\left[\left(V_{gb} - V_{fb}\right)\left(\phi_{sL} - \phi_{s0}\right) - \frac{1}{2}\left(\phi_{sL}^2 - \phi_{s0}^2\right) - \frac{2}{3}\gamma\left(\phi_{sL}^{3/2} - \phi_{s0}^{3/2}\right)\right] \tag{4.48}$$

where, ϕ_{s0} and ϕ_{sL} are the surface potentials as shown in Figure 4.8 and are computed iteratively for each bias point from the surface potential Equation 4.37.

4.4.3.2 Diffusion Component of Drain Current

From Equation 4.44, we get for the *diffusion* component of the drain current using the boundary condition from Equation 4.46 as

$$\int_0^L I_{ds2}\,dy = \mu_s W v_{kT} \int_{\phi_{s0}}^{\phi_{sL}} dQ_i \tag{4.49}$$

Substituting for Q_i from Equation 4.40 in Equation 4.49, we can show

$$\int_0^L I_{ds2}\,dy = \mu_s C_{ox} W v_{kT} \int_{\phi_{s0}}^{\phi_{sL}} \left(d\phi_s + \frac{\gamma}{2}\frac{d\phi_s}{\sqrt{\phi_s}}\right) \tag{4.50}$$

Therefore, after integration and simplification, we get for diffusion component of drain current as

$$I_{ds2} = \mu_s C_{ox} \frac{W}{L} v_{kT}\left[\left(\phi_{sL} - \phi_{s0}\right) + \gamma\left(\phi_{sL}^{1/2} - \phi_{s0}^{1/2}\right)\right] \tag{4.51}$$

In order to solve I_{ds1} and I_{ds2} from Equations 4.50 and 4.51, respectively, we obtain ϕ_{s0} at $y = 0$ at the source end and ϕ_{sL} at $y = L$ at the drain end of the MOSFET channel from Equation 4.37. The total current is obtained by adding Equations 4.48 and 4.51. The values of ϕ_{s0} and ϕ_{sL} required to calculate I_{ds} are obtained numerically by solving the implicit Equation 4.37 under the boundary conditions

$$\phi_s(y) = \begin{cases} \phi_{s0} & \text{at } y = 0 \\ \phi_{sL} & \text{at } y = L \end{cases}$$

and (4.52)

$$V_{ch}(y) = \begin{cases} V_{sb} & \text{at } y = 0 \\ V_{sb} + V_{ds} & \text{at } y = L \end{cases}$$

Using the boundary conditions (Equation 4.52) in Equation 4.37, we can show that the implicit equations for ϕ_{s0} and ϕ_{sL} are given by

$$\phi_{s0} = V_{gb} - V_{fb} - \gamma\sqrt{\phi_{s0} + v_{kT}e^{(\phi_{s0} - 2\phi_B - V_{sb})/v_{kT}}} \tag{4.53}$$

$$\phi_{sL} = V_{gb} - V_{fb} - \gamma\sqrt{\phi_{sL} + v_{kT}e^{[\phi_{sL} - 2\phi_B - (V_{sb} + V_{ds})]/v_{kT}}} \tag{4.54}$$

From Equations 4.48 and 4.51, we find that both the drift and diffusion components of I_{ds} depend on $(\phi_{sL} - \phi_{s0})$. In weak inversion, $\phi_{s0} \approx \phi_{sL,}$ so that even small errors in the values of ϕ_{s0} and ϕ_{sL} can lead to a large error in I_{ds2}. Therefore, an accurate solution is required for the surface potential, particularly for weak inversion conditions. In reality, the accuracy of calculation for ϕ_s must be ~1×10^{-12} V. The implicit Equation 4.37 can be solved iteratively as well as by using Taylor series expansion [23] to obtain ϕ_{s0} and ϕ_{sL} at each biasing condition.

Figure 4.9 shows the total drain current I_{ds} and its components I_{ds1} and I_{ds2} as function of V_{gb} at $V_{db} = 3$ V and $V_{sb} = 1$ V. Figure 4.9 shows that in strong inversion, $I_{ds} \approx I_{ds1}$, and therefore, the total current is mainly due to the drift of electrons due to V_{ds}. In weak inversion, $I_{ds} \approx I_{ds2}$, and the current is mainly due to diffusion of minority carriers from the source end to the drain. However, there is a region between the weak inversion and the strong inversion, called *moderate inversion*, where both the drift and diffusion components are important. The width of the moderate inversion in terms of voltage is several tenths of a volt [24,25]. It is shown that the lower limit of $\phi_s \equiv \phi_{mL}$ in the moderate inversion is ~$(2\phi_B - v_{kT})$, whereas the upper limit $\phi_s = \phi_{mU} \sim (2\phi_B + 6v_{kT})$. And, the corresponding values for V_{gb} are V_{gbL} and V_{gbU}, respectively, are obtained from Equation 4.37 by solving for $\phi_s = \phi_{mL}$ and ϕ_{mU}, respectively.

The comparison of $I_{ds} - V_{ds}$ characteristics shows that the Brews charge-sheet model predicts I_{ds} within 1% of that calculated using the Pao-Sah model under most operating conditions [13]. Although, the charge-sheet model is simpler compared to the Pao-Sah model, it still requires time-consuming iterations to calculate ϕ_{s0} and ϕ_{sL}. Therefore, it is computationally intensive. Hence, in spite of its advantages, this model has not been widely used in real circuit CAD until the development and release of the Hiroshima University STARC IGFET Model (HiSIM) [26] in 2006. HiSIM basic current equations are based on Brews charge-sheet model.

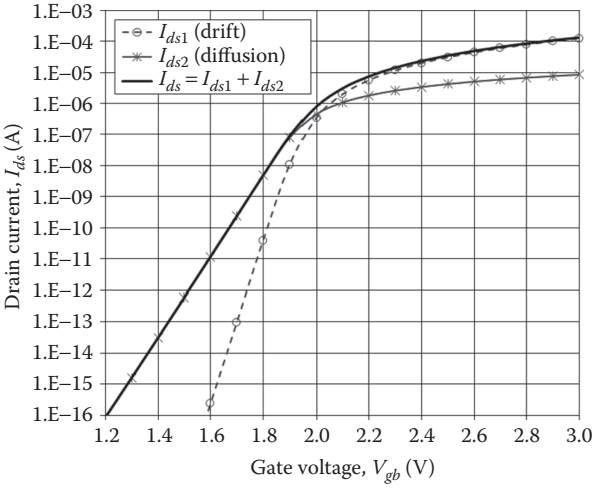

FIGURE 4.9
Drain current as a function of gate voltage obtained by charge sheet model; the plots are obtained for nMOSFET devices with $W/L = 1$ and $T_{ox} = 600$ nm for biasing condition $V_{fb} = -1$ V, $V_{sb} = 1$ V, and $V_{db} = 3$ V.

Though the Pao-Sah and charge-sheet models are complete and most accurately describe MOSFET device characteristics, they are complex and computationally inefficient for circuit CAD. Therefore, simplified analytical compact drain current models have been developed from the generalized drain current (Equation 4.29) based on additional approximations to circumvent solving the implicit Equation 4.37 for calculating ϕ_s. This is achieved by separately modeling each distinct regions of device operation with appropriate boundary conditions. The most commonly used boundary between the *weak* and *strong* inversion regions is the threshold voltage, V_{th}. Based on this approach, we will develop a current equation for *strong inversion* region and the other for *weak inversion* region of device operation to analyze each region independently. Note that the Pao-Sah and charge-sheet models model the entire range of device operation and have completely natural transitions between different regions. The regional models, also known as the *piece-wise* multisectional models, are most commonly used for circuit CAD because of their simplicity and computational efficiency. In the following section, we will develop the first-order piecewise model for large geometry devices and subsequent improvement of the basic models for improved accuracy. In Chapter 5, we will develop more accurate compact industry standard models for short channel VLSI devices for circuit CAD.

4.4.4 Regional Drain Current Model

Equation 4.29 represents the generalized expression for I_{ds} that is derived using five appropriate assumptions to include both the drift and diffusion components of current and is repeated here

$$I_{ds} = \mu_s \left(\frac{W}{L} \right) \int_{V_{sb}}^{V_{sb}+V_{ds}} Q_i(y) dV_{ch} \tag{4.55}$$

In order to derive simplified regional compact MOSFET models for circuit CAD, we will make further simplifying assumptions.

Assumption 6: Let us assume that the diffusion current is negligibly small so that the current flow along the channel in the device is only due to the drift of minority carriers by the applied drain voltage, V_{ds}. This is a fairly good assumption provided the device is in strong inversion; that is, the gate voltage is greater than the threshold voltage ($V_{gs} > V_{th}$ or $\phi_s > 2\phi_B$). If the diffusion current is neglected, then from Equation 4.16 we can write for an nMOSFET device

$$J_n(y) \cong qn(x,y)\mu_s E(y) = -qn(x,y)\mu_s(x,y)\frac{\partial \phi_s(y)}{\partial y} \tag{4.56}$$

where we can safely use $\left(\partial \phi_n / \partial y\right) = \left(\partial \phi_s / \partial y\right)$, that is, the gradients of quasi-Fermi potential and surface potential along the channel are the same in strong inversion. Therefore, for nMOSFET devices at strong inversion, we can write

$$\phi_s(y) = \phi_s(0) + V_{ch}(y) \tag{4.57}$$

where:

$\phi_s(0)$ is the surface potential at $y = 0$ (source end)

For the simplicity of calculation, it is more convenient to express the channel potential in terms of the source potential, V_{sb} and channel voltage $V(y)$ at any point y in the channel due to the applied drain voltage V_{ds} so that

$$V_{ch}(y) = V_{sb} + V(y) \tag{4.58}$$

where $V(y)$ now varies from 0 at $L = 0$ at the source end to V_{ds} at $y = L$ at the drain end of the channel. Then using Equation 4.58, at strong inversion ($\phi_s = 2\phi_B$), Equation 4.57 can be expressed as

$$\phi_s(y) = 2\phi_B + V_{sb} + V(y) \tag{4.59}$$

where $\phi_s(0) = 2\phi_B$ at strong inversion, and $V(y)$ varies from 0 at the source end to V_{ds} at the drain end. Now, substituting Equation 4.59 in 4.56, we get

$$J_n(y) = qn(x,y)\mu_s E(y) = -qn(x,y)\mu_s(x,y)\frac{dV}{dy} \tag{4.60}$$

And, therefore,

$$I_{ds}(y) = -W\frac{dV}{dy}\int_0^{\infty} qn(x,y)\mu_s(x,y)dx \tag{4.61}$$

We know that the minority carrier charge density, Q_i, is given by

$$Q_i(y) = -q\int_0^{\infty} n(x,y)dx \tag{4.62}$$

Then using Equation 4.62 in Equation 4.61, we get the simplified expression for $I_{ds}(y)$ as

$$I_{ds}(y)dy = W\mu_s Q_i(y)dV(y) \tag{4.63}$$

Again we assume that GCA is valid along the entire length of the channel; then integrating Equation 4.63 along the channel length from $y = 0$ to $y = L$ we get

$$I_{ds} = \mu_s\left(\frac{W}{L}\right)\int_0^{V_{ds}} Q_i(y)dV \tag{4.64}$$

Equation 4.64 is the simplified drain current equation for I_{ds} expression to develop compact MOSFET model for circuit CAD in the different regions of device operation. Thus, to calculate I_{ds} in a MOSFET device, we need to calculate Q_i. In the following section, we will derive simple and more useful expression for Q_i using charge balance equation given by Equation 4.40.

4.4.4.1 Core Model

In terms of source as the reference terminal, the expression for inversion charge $Q_i(y)$ in Equation 4.40 can be expressed as

$$Q_i(y) = Q_s(y) - Q_b(y) = -C_{ox}\left[V_{gs} + V_{sb} - V_{fb} - \phi_s(y)\right] - Q_b(y) \tag{4.65}$$

Linear Region Operation: In order to develop the linear region I_{ds} model, we substitute for $\phi_s(y)$ from Equation 4.59 into Equation 4.65 to obtain inversion charge at strong inversion as

$$Q_i(y) = -C_{ox}\left[V_{gs} - V_{fb} - 2\phi_B - V(y)\right] - Q_b(y) \tag{4.66}$$

And, substituting $\phi_s(y)$ from Equation 4.59 into Equation 4.38, we get for the depletion charge

$$Q_b(y) = -\gamma C_{ox}\sqrt{2\phi_B + V_{sb} + V(y)} \tag{4.67}$$

Assumption 7: For a first-order model, we assume that Q_b is a constant along the length of the channel, independent of the applied drain voltage V_{ds} so that $\phi_s(y) = 2\phi_B + V_{sb}$ is a constant along the length of the channel. Therefore, Equation 4.67 can be approximated to

$$Q_b(y) \cong -\gamma C_{ox}\sqrt{2\phi_B + V_{sb}} \tag{4.68}$$

Now, substituting for $Q_b(y)$ from Equation 4.68 into Equation 4.66, we get after simplification

$$Q_i(y) = -C_{ox}\left[V_{gs} - \left(V_{fb} + 2\phi_B + \gamma\sqrt{2\phi_B + V_{sb}}\right) - V(y)\right] \tag{4.69}$$

In Equation 4.12, we have shown that $V_{th} = V_{fb} + 2\phi_B + \gamma\sqrt{(2\phi_B + V_{sb})}$; therefore, we can express Equation 4.69 as

$$Q_i(y) = -C_{ox}\left[V_{gs} - V_{th} - V(y)\right] \tag{4.70}$$

Now, substituting for $Q_i(y)$ from Equation 4.70 in Equation 4.64, we get

$$I_{ds} = \mu_s C_{ox}\left(\frac{W}{L}\right)\int_0^{V_{ds}}\left[V_{gs} - V_{th} - V(y)\right]dV \tag{4.71}$$

After integration of Equation 4.71, we get the first-order drain current model as

$$I_{ds} = \mu_s C_{ox}\left(\frac{W}{L}\right)\left[V_{gs} - V_{th} - \frac{V_{ds}}{2}\right]V_{ds}; \quad V_{gs} > V_{th} \tag{4.72}$$

This current equation was derived by Sah [27] and later used by Shichman and Hodges [28] for modeling MOSFET devices in circuit simulation. This is known as the Simulation Program with Integrated Circuit Emphasis (SPICE) MOS Level 1 model. The factor $\mu_s C_{ox}$ is a model parameter and is referred to as the process transconductance, κ, so that

$$\kappa = \mu_s C_{ox} \tag{4.73}$$

The parameter κ describes the effect of process variation in the drain current. Also, $\kappa(W/L)$ is called the gain factor of a MOSFET device and is defined as

$$\beta = \mu_s C_{ox}\left(\frac{W}{L}\right) \tag{4.74}$$

For small $V_{ds} \leq (V_{gs} - V_{th}) \leq 0.1$ V, Equation 4.72 can be approximated using β from Equation 4.74 as

$$I_{ds} \cong \beta\left[V_{gs} - V_{th}\right]V_{ds}; \quad V_{gs} > V_{th} \tag{4.75}$$

Equation 4.72 shows that I_{ds} varies linearly with V_{ds}. Consequently, this region of MOSFET device performance is called the *linear region* operation. From Equation 4.75, we get

$$\frac{V_{ds}}{I_{ds}} \cong \frac{1}{\beta\left[V_{gs} - V_{th}\right]} = \frac{1}{\beta V_{gst}} \equiv R_{ch} \tag{4.76}$$

where:

R_{ch} is called the channel resistance and is the effective resistance between the source and drain regions of MOSFET channel

Note that R_{ch} varies linearly with $(V_{gs} - V_{th}) \equiv V_{gst}$. V_{gst} is referred to as the *effective gate voltage* or *gate over drive voltage*. Thus, MOSFET devices are sometime referred to as the voltage-controlled variable resistors.

Figure 4.10 shows I_{ds} versus V_{ds} plots for different values of V_{gs} as calculated from Equation 4.72. It is seen from Figure 4.10 that for a given value of V_{gs}, the drain current I_{ds} initially increases with increasing V_{ds}, reaches a peak value and then begins to decrease with further increase in V_{ds}. This decrease in I_{ds} for higher values of V_{ds} is in contrast to the experimental observation, which shows saturation of I_{ds} at its peak value with further increase in V_{ds}. The discrepancy between the measured and computed value of I_{ds} by Equation 4.72 is due to the breakdown of GCA at high V_{ds} beyond

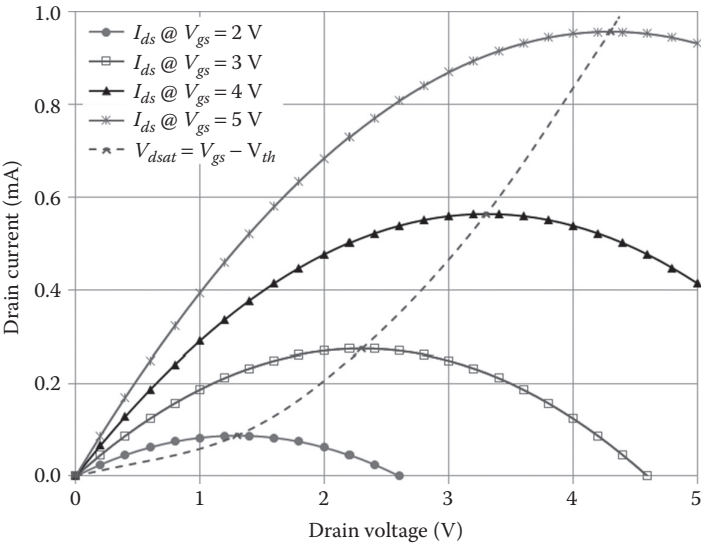

FIGURE 4.10
The current voltage characteristics of an nMOSFET device using Equation 4.72 with $T_{ox} = 20$ nm, $W/L = 1$, $V_{th} = 0.7$ V, and electron mobility = 600 cm^2 V^{-1} sec^{-1}; the dashed line shows the saturation drain voltage, V_{dsat} for each gate voltage.

the peak value of I_{ds}. Now, by differentiating Equation 4.72 with respect to V_{ds} we get

$$\frac{dI_{ds}}{dV_{ds}} = \mu_s C_{ox}\left(\frac{W}{L}\right)\left[V_{gs} - V_{th} - V_{ds}\right] \tag{4.77}$$

We know that at the point of inflexion, that is, at the peak location of $I_{ds} - V_{ds}$ plot, the slope of I_{ds} versus V_{ds} plot, $dI_{ds}/dV_{ds} = 0$. Therefore, equating Equation 4.77 to zero, we get

$$V_{ds} = V_{gs} - V_{th} \tag{4.78}$$

Equation 4.78 shows the condition at which I_{ds} peaks. Now, at this condition, let us find the inversion charge density at the drain end of the channel $Q_i(y = L)$ under the biasing condition of Equation 4.78.

We know that at the drain end of MOSFET channel, $y = L$, $V(y) = V_{ds}$. Then substituting for $V(y) = (V_{gs} - V_{th})$, in Equation 4.70, the channel charge $Q_i(y = L)$ at the drain end of the channel is given by

$$Q_i(y = L) = -C_{ox}\left[V_{gs} - V_{th} - (V_{gs} - V_{th})\right] = 0 \tag{4.79}$$

This value of $Q_i(L) = 0$ implies that at $V_{ds} = V_{gs} - V_{th}$, the channel does not exist at the drain end of the device. And, the maximum value of $V(y)$ will be at the drain end of the channel where $V(y) = V_{ds}$; therefore, when $V_{ds} \geq (V_{gs} - V_{th})$, we find $Q_i = 0$ at the drain end of the channel. In other words, once the peak current is reached, the GCA (assumption 1) fails and Equation 4.72 is no longer valid for $V_{ds} \geq (V_{gs} - V_{th})$. And, therefore, we need to derive a separate expression for drain current in the saturation region for $V_{ds} \geq (V_{gs} - V_{th})$.

Device Saturation: The physical understanding of the mathematical interpretations of Equations 4.78 and 4.79 can be achieved by analysis of device operation under varying V_{ds} for a certain value of $(V_{gs} - V_{th}) > 0$, that is, at strong inversion as shown in Figure 4.11. In deriving I_{ds} Equation 4.72, it is assumed that an inversion layer exists along the channel from the source end to drain end as shown in Figure 4.11a. This is only true for $V_{gs} \geq V_{th}$ with very low value of $V_{ds} < 100$ mV. For a given value of V_{gs}, when $V_{ds} = (V_{gs} - V_{th})$, Equation 4.79 shows that the value of Q_i at the drain end drops to zero. This implies that the channel is *pinched off* at the drain end with $Q_i(L)$ approaching to zero as shown in Figure 4.11b. And, consequently, the magnitude of the vertical electric field E_x approaches to that of the lateral electric field E_y at the pinch-off point.

The drain voltage at which the channel pinch-off occurs at the drain end is called the *pinch-off* or *saturation voltage*, V_{dsat}. The corresponding drain current at V_{dsat} is called the saturation drain current I_{dsat} or device on current I_{on}. From Equations 4.78 and 4.79, the condition for pinch-off ($Q_i = 0$) is $(dI_{ds}/dV_{ds}) = 0$, that is, at pinch-off point the slope of $I_{ds} - V_{ds}$ characteristics

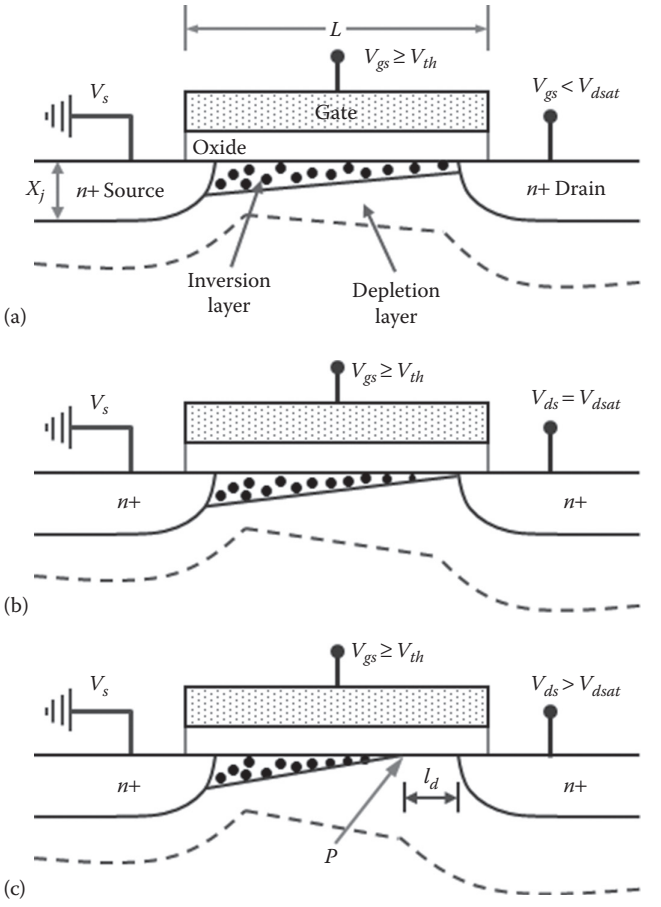

FIGURE 4.11
Schematic diagram of an nMOSFET device at strong inversion showing channel pinch-off as V_{ds} is increased; (a) an inversion layer connects the source and drain, $V_{ds} < V_{dsat}$ and (b) at the onset of saturation, the channel pinches off at the drain end, $V_{ds} = V_{dsat}$, and (c) the pinch-off point P moves toward the source.

becomes zero. At the pinch-off point, $E_x = E_y$, and when $E_y > E_x$, the mobile carriers are pushed off the surface near the drain region creating drain depletion or *pinch-off region* as shown in Figure 4.11c. Then from Equation 4.78, the pinch-off voltage, commonly referred to as the saturation drain voltage, V_{dsat} is given by

$$V_{dsat} = V_{gs} - V_{th} \tag{4.80}$$

Equation 4.80 shows that the pinch-off voltage V_{dsat} equals the effective gate voltage V_{gst} that increases with increasing V_{gs} as shown in Figure 4.10 by the

dash curve. Then substituting for $V_{ds} = V_{dsat}$ from Equation 4.80 in Equation 4.72, we get the drain current I_{dsat} at the pinch-off point as

$$I_{dsat} = \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2; \quad \text{at } V_{ds} = V_{dsat} = V_{gs} - V_{th} \tag{4.81}$$

Thus, the simplified compact model requires two separate expressions for I_{ds} given by Equations 4.72 and 4.81 to model the MOSFET device characteristics in strong inversion region in contrast to Pao-Sah and Brews models described earlier.

Saturation Region Operation: Thus, we find that for a given V_{gs}, as V_{ds} increases the channel charge Q_i decreases near the drain end, and when $V_{ds} = V_{dsat} = (V_{gs} - V_{th})$, the channel is pinched off. For $V_{ds} > V_{dsat}$, the pinched-off region moves away from the drain end of the channel, widening the drain depletion region as shown in Figure 4.11c. Thus, as V_{ds} increases beyond pinch-off, the pinched-off region l_d between the channel pinch-off point P and the $n+$ drain region causes the effective channel length to decrease from L to $(L - l_d)$. Since the channel can support only V_{dsat}, any voltage greater than V_{dsat} is absorbed by the l_d region of the channel. Clearly, l_d is bias-dependent parameter, modulating the effective channel length ($L_{eff} = L - l_d$). This phenomenon is called the *channel length modulation* (CLM). For long channel devices with $L >> l_d$, the drain current I_{ds} remains approximately constant at I_{dsat} for any $V_{ds} > V_{dsat}$. Thus, to a first order, for V_{ds} beyond the pinch-off value, the current $I_{ds} = I_{dsat}$ and is given by Equation 4.81 and is repeated below:

$$I_{dsat} = \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2; \quad V_{ds} > V_{dsat} \tag{4.82}$$

The region of operation of the MOSFETs beyond pinch-off ($V_{ds} > V_{dsat}$) is referred to as the saturation region because I_{ds} ideally does not increase in this region. And, the region below V_{dsat} is called the linear region or triode region. Note that Equation 4.82 predicts that I_{ds} in saturation varies as the square of the effective gate voltage and hence often referred to as the square law model of the MOSFETs. Equations 4.72, 4.80, and 4.82 when plotted together result the output characteristics of a MOSFET device as shown by the continuous lines in Figure 4.12.

Figure 4.12 shows that the calculated value of I_{ds} by Equation 4.82 saturates beyond V_{dsat}. This is because Equation 4.82 is based on the assumption that the current is independent of V_{ds}. In reality, I_{ds} depends on $V_{ds} > V_{dsat}$ due to CLM due to the change in the effective channel length $L_{eff} = L - l_d$. Then using L_{eff} for L in Equation 4.82, we get

$$I_{ds} = \mu_s C_{ox} \frac{W}{2\left(L - l_d\right)}\left(V_{gs} - V_{th}\right)^2; \quad V_{ds} > V_{dsat} \tag{4.83}$$

Equation 4.83 shows that as l_d increases with the increasing $V_{ds} > V_{dsat}$, the drain current increases. We can express Equation 4.83 as

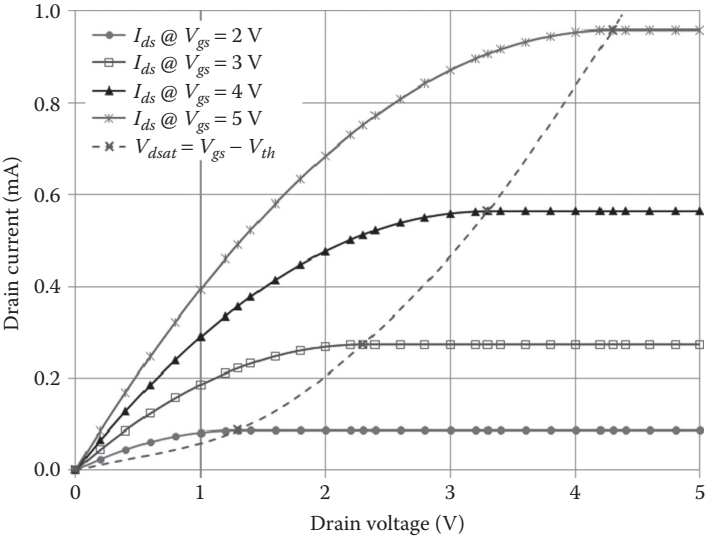

FIGURE 4.12
The current voltage characteristics of an nMOSFET device using Equations 4.72 and 4.82 with T_{ox} = 20 nm, W/L = 1, V_{th} = 0.7 V, and electron mobility = 600 cm^2 V^{-1} sec^{-1}; the dashed line separates the linear and the saturation regions of MOSFET operation.

$$I_{ds} = \mu_s C_{ox} \frac{W}{2L\left[1-\left(l_d/L\right)\right]}\left(V_{gs}-V_{th}\right)^2; \quad V_{ds} > V_{dsat}$$

$$= \mu_s C_{ox} \frac{W}{2L}\left(V_{gs}-V_{th}\right)^2 \cdot \frac{1}{\left[1-\left(l_d/L\right)\right]} \tag{4.84}$$

$$= \frac{\beta}{2}\left(V_{gs}-V_{th}\right)^2 \cdot \left(1-\frac{l_d}{L}\right)^{-1}$$

Using Equation 4.82 in Equation 4.84, we can show for $V_{ds} > V_{dsat}$

$$I_{ds} = I_{dsat}\left(1-\frac{l_d}{L}\right)^{-1} \tag{4.85}$$

In general, $l_d << L$; therefore, by series expansion we get, $\left[1-\left(l_d/L\right)\right]^{-1} \cong 1+\left(l_d/L\right)$. Since l_d increases with the increase of V_{ds}, that is, l_d/L is directly proportional to V_{ds}, we can write $1+\left(l_d/L\right) = 1+\lambda V_{ds}$. Then Equation 4.85 becomes

$$I_{ds} = I_{dsat}\left(1+\lambda V_{ds}\right) \tag{4.86}$$

where:

λ is called the CLM parameter describing the effect of V_{ds} on l_d to model CLM

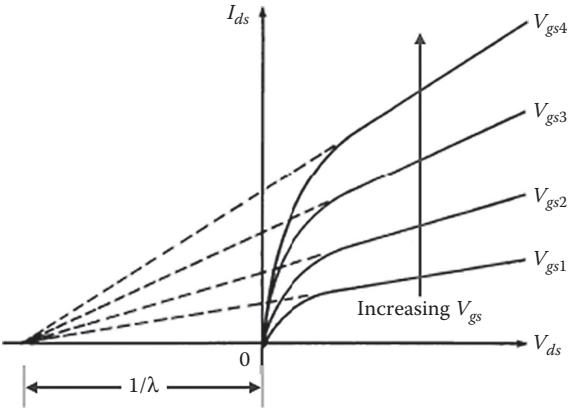

FIGURE 4.13
A typical $I_{ds} - V_{ds}$ characteristics of an nMOSFET device showing the effect of channel length modulation and CLM factor, λ.

We notice from Equation 4.86 that when $V_{ds} = -1/\lambda$, $I_{ds} = 0$. This means that when I_{ds} is extrapolated backward from the saturation region, it will intersect the V_{ds} axis at a value of $-1/\lambda$ as shown in Figure 4.13. However, this is an ideal case and generally the value of λ is obtained by curve fitting the measurement data to Equation 4.86 to minimize the error between the measured data and model.

Equation 4.86 is a first-order approximation for modeling CLM effect in MOSFETs. It provides the basic feature of nonzero slope for the saturated drain current as shown in Figure 4.13. However, the use of Equation 4.86 for calculating I_{ds} in the saturation region results in a discontinuity of the current at $V_{ds} = V_{dsat}$. The SPICE model Level 1 corrects for the discontinuity by multiplying the linear region current by the factor $(1 + \lambda V_{ds})$. Other methods include use of mathematical smoothing functions to make the liner and saturation curve at the transition point at $V_{ds} = V_{dsat}$.

To summarize, we have developed a first-order MOSFET model, which can be described by the following expressions

$$I_{ds} = \begin{cases} 0\,; & \left(V_{gs} - V_{th}\right) < 0 \\ \beta\left(V_{gs} - V_{th} - \dfrac{1}{2}V_{ds}\right)V_{ds}\,; & 0 < \left(V_{gs} - V_{th}\right) \geq V_{ds} \\ \dfrac{\beta}{2}\left(V_{gs} - V_{th}\right)^2\left(1 + \lambda V_{ds}\right); & 0 < \left(V_{gs} - V_{th}\right) \leq V_{ds} \end{cases} \tag{4.87}$$

In Equation 4.87, β depends on κ [Equation 4.73], W, L, and C_{ox} [Equation 4.74] whereas, V_{th} depends on V_{th0}, $2\phi_B$, and γ [Equation 4.14]. Since C_{ox} depends on T_{ox}, the parameter set of SPICE Level 1 model is $\{V_{th0}, \kappa, \gamma, \lambda, 2\phi_B\}$.

SPICE Level 1 model is derived based on the following assumptions:

1. The GCA is valid
2. Majority carrier current can be neglected (e.g., neglected hole current for nMOSFETs)
3. Recombination and generation are neglected
4. Current flows in the y direction (along the length of channel) only
5. Inversion carrier mobility μ_s is a constant in the y direction along the channel
6. Current flow is due to the drift of minority carriers only (diffusion current is neglected)
7. Bulk charge Q_b is constant at any point in the y direction

The parameters of Level 1 MOSFET model for circuit CAD are shown in Table 4.1.

Although Equation 4.87 is derived for an nMOSFET device, the same expressions apply for a p-channel MOSFET (pMOSFET) device once all polarities of voltages and currents are reversed. The accuracy of Level 1 model is very poor even for long channel (10 μm) devices. However, it is very useful for performing basic circuit analysis and developing design equations for circuit performance.

4.4.4.2 Bulk-Charge Model

The level 1 drain current model is useful for hand calculations; however, it is not accurate for circuit CAD because of the inherent simplifying assumptions in deriving the current model. In order to improve the modeling accuracy, first of all, we examine the effect of bulk charge Q_b on I_{ds}. In level 1, we assumed that Q_b is a constant along the length of the channel. This means that the depletion width X_{dm} under the gate is a constant from the source to drain for all biasing conditions of $V_{ds} > 0$. In reality, when $V_{ds} > 0$, X_{dm} will increase as we move from the source toward the drain as shown in Figure 4.14. Consequently, it is more appropriate to consider the variation of bulk charge along the channel due to the applied drain bias from Equation 4.67. Then from Equations 4.66 and 4.67, the inversion charge density $Q_i(y)$ is given by

TABLE 4.1

Model Parameters for MOS Level 1 Compact Model

Device Parameter	Level 1 Model Parameter	Definition
V_{th0}	VTO	Threshold voltage at zero body bias
κ	KP	Transconductance parameter
γ	GAMMA	Body factor
λ	LAMBDA	CLM factor
$2\lvert\phi_B\rvert$	PHI	Bulk potential

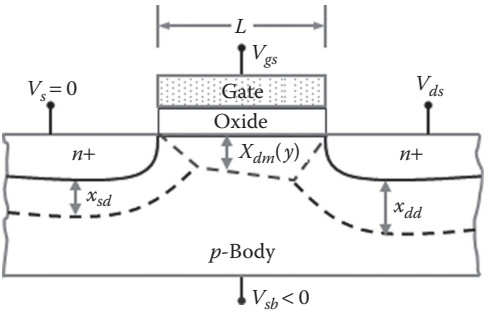

FIGURE 4.14
Depletion region widening at the drain end of the channel of an nMOSFET device due to CLM by applied drain voltage.

$$Q_i(y) = -C_{ox}\left[V_{gs} - V_{fb} - 2\phi_B - V(y) - \gamma\sqrt{2\phi_B + V_{sb} + V(y)}\right] \tag{4.88}$$

Substituting Equation 4.88 in Equation 4.64 and integrating from $V(y) = V_{sb}$ at $y = 0$ to $V(y) = V_{sb} + V_{ds}$ at $y = L$, we get

$$I_{ds} = \mu_s C_{ox}\left(\frac{W}{L}\right)\left\{\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds} - \frac{2}{3}\gamma\left[\left(V_{ds} + 2\phi_B + V_{sb}\right)^{3/2} - \left(2\phi_B + V_{sb}\right)^{3/2}\right]\right\} \tag{4.89}$$

Equation 4.89 accounts for the bulk-charge variation in the depletion region of MOSFETs. The linear region drain current (Equation 4.89) is sometimes referred to as the Ihantola–Moll model [29] and used as SPICE Level 2 MOS model. Comparing Equations 4.72 and 4.89, we find that Equation 4.89 predicts lower current compared to Equation 4.72. This is because the increasing bulk charge Q_b will reduce the inversion charge Q_i for the same bias condition, resulting in a lower drain current. However, Equation 4.89 is more complex compared to Equation 4.72 and time-consuming for circuit CAD.

In order to derive model equation for I_{dsat}, we calculate V_{dsat} by differentiating Equation 4.89 with respect to V_{ds} and equate the resulting expression to zero. This results in the following expression for V_{dsat}

$$V_{dsat} = V_{gs} - V_{fb} - 2\phi_B + \frac{\gamma^2}{2} - \gamma\sqrt{V_{gs} - V_{fb} + V_{sb} + \frac{\gamma^2}{4}} \tag{4.90}$$

Then substituting $V_{ds} = V_{dsat}$ from Equation 4.90 into Equation 4.89, we can compute the saturation region drain current I_{dsat}.

4.4.4.3 Square Root Approximation of Bulk-Charge Model

In order to develop a computationally efficient drain current model considering $Q_b(y)$, we simplify Equation 4.67 by Taylor series expansion and neglect the higher order terms to get

$$\begin{aligned} Q_b(y) &= -C_{ox}\gamma\left[\sqrt{2\phi_B + V_{sb}} + \frac{1}{2}\frac{V(y)}{\sqrt{2\phi_B + V_{sb}}} - \cdots\right] \\ &\cong -C_{ox}\gamma\left[\sqrt{2\phi_B + V_{sb}} + \frac{1}{2\sqrt{2\phi_B + V_{sb}}}V(y)\right] \\ &\cong -C_{ox}\gamma\left[\sqrt{2\phi_B + V_{sb}} + \delta \cdot V(y)\right] \end{aligned} \tag{4.91}$$

Equation 4.91 is called the *square root approximation* of $Q_b(y)$, where δ accounts for the *bulk-charge effect in MOSFETs* and is given by

$$\delta \equiv \frac{1}{2\sqrt{2\phi_B + V_{sb}}} \tag{4.92}$$

It is found that the value of δ obtained by Equation 4.92 is too large for accurate calculation of I_{ds} at low V_{sb} and high V_{ds}. In order to obtain accurate value of δ, several semi-empirical expressions for δ have been proposed as discussed by Arora [13]. It is found that the more appropriate expressions of δ for circuit CAD are the following semi-empirical relations

$$\delta \equiv \frac{1}{2\sqrt{1 + 2\phi_B + V_{sb}}} \tag{4.93}$$

and

$$\delta \equiv \frac{1}{2\sqrt{2\phi_B + V_{sb}}}\left[1 - \frac{1}{a_1 + a_2\left(2\phi_B + V_{sb}\right)}\right] \tag{4.94}$$

where a_1 and a_2 are obtained to minimize the error between the exact function $\sqrt{2\phi_B + V_{sb} + V(y)}$ and its approximation $\left(\sqrt{2\phi_B + V_{sb}} + \delta \cdot V\right)$ within the operating range of V_{sb} and V_{ds}.

With the square root approximation of $Q_b(y)$ from Equation 4.91 in Equation 4.66, we get

$$\begin{aligned} Q_i(y) &= -C_{ox}\left\{V_{gs} - V_{fb} - 2\phi_B - V(y) - \gamma\left[\delta \cdot V(y) + \sqrt{2\phi_B + V_{sb}}\right]\right\} \\ &= -C_{ox}\left[V_{gs} - \left(V_{fb} + 2\phi_B + \gamma\sqrt{2\phi_B + V_{sb}}\right) - (1 + \delta \cdot \gamma)V(y)\right] \\ &= -C_{ox}\left[V_{gs} - V_{th} - \alpha V(y)\right] \end{aligned} \tag{4.95}$$

where we have used Equation 4.12 for V_{th} and α is defined as

$$\alpha = 1 + \delta \cdot \gamma \tag{4.96}$$

α is called the bulk-charge coefficient.

The final expression for $Q_i(y)$ in Equation 4.95 is similar to Equation 4.70 with the difference of the term α, which accounts for the variation of bulk charge along the channel. Using $Q_i(y)$ from Equation 4.95 into Equation 4.64 and after integration and simplification we get the expression for linear current as

$$I_{ds} = \beta\left[V_{gs} - V_{th} - \frac{1}{2}\alpha V_{ds}\right]V_{ds}; \quad V_{gs} > V_{th} \tag{4.97}$$

Comparing Equation 4.97 with Equation 4.89, we see that by approximating the square root term in $Q_b(y)$ we get a much simpler expression for I_{ds}. This current equation is used in most advanced regional drain current models (e.g., BSIM) for circuit CAD [30].

Now, differentiating Equation 4.97 with respect to V_{ds} and equating the resulting expression to zero gives the following simple expression for V_{dsat}

$$V_{dsat} = \frac{V_{gs} - V_{th}}{\alpha} \tag{4.98}$$

Substituting for V_{dsat} from Equation 4.98 into Equation 4.97, we get the drain current model in the saturation region as

$$I_{dsat} = \frac{\beta}{2\alpha}\left(V_{gs} - V_{th}\right)^2; \quad V_{ds} \geq V_{dsat} \tag{4.99}$$

To summarize, we now have a more accurate and compact drain current model that takes into account the bulk-charge variation along the channel region and is represented by the following set of equations

$$I_{ds} = \begin{cases} 0; & \left(V_{gs} - V_{th}\right) < 0 \\ \beta\left(V_{gs} - V_{th} - \dfrac{1}{2}\alpha V_{ds}\right)V_{ds}; & 0 < \left(V_{gs} - V_{th}\right) \geq V_{ds} \\ \dfrac{\beta}{2\alpha}\left(V_{gs} - V_{th}\right)^2; & 0 < \left(V_{gs} - V_{th}\right) \leq V_{ds} \end{cases} \tag{4.100}$$

Equation 4.100 is simple and has been widely used in circuit CAD prior to the introduction of industry standard compact models.

4.4.4.4 Subthreshold Region Drain Current Model

The regional expressions for I_{ds} in Equations 4.87 and 4.100 are derived assuming that the current flow is due to drift only. This resulted in $I_{ds} = 0$ for $V_{gs} < V_{th}$, In reality, this is not true and I_{ds} has a small but finite value for $V_{gs} < V_{th}$ as shown in Figure 4.9, which shows that I_{ds} is of the order of 10 nA for $V_{gs} \approx V_{th}$ and decreases exponentially below V_{th}. This current below V_{th} is called the

subthreshold or *weak inversion* current and occurs when $V_{gs} < V_{th}$ or $\phi_B < \phi_s < 2\phi_B$. Unlike the inversion region where drift current dominates, the subthreshold region conduction is dominated by diffusion current as shown in Figure 4.9. The subthreshold region current is important since this is a major contributor to device leakage current that affects the dynamic circuit performance and determines CMOS standby power. In this region of operation, the assumption $I_{ds} = 0$ in Equations 4.87 and 4.100 (by assumption 6) is not valid.

In the subthreshold region of operation, $Q_i << Q_b$, and therefore, the surface potential ϕ_s (or band bending) is nearly constant from the source to drain end of the device. This means that we can replace $\phi_s(y)$ in the subthreshold region by some constant value, ϕ_{ss}. Then, the bulk charge Q_b in Equation 4.38 can be expressed as

$$Q_b = -C_{ox}\gamma\sqrt{\phi_s(y)} \cong -C_{ox}\gamma\sqrt{\phi_{ss}} \tag{4.101}$$

Again, since $Q_i << Q_b$, we have $Q_s \approx Q_b$, so that Equation 4.6 becomes

$$V_{gb} = V_{fb} + \phi_{ss} - \frac{Q_b}{C_{ox}} \tag{4.102}$$

Substituting for Q_b from Equation 4.101 to Equation 4.93, we get

$$V_{gb} = V_{fb} + \phi_{ss} + \gamma\sqrt{\phi_{ss}}$$

or (4.103)

$$\left(\sqrt{\phi_{ss}}\right)^2 + \gamma\sqrt{\phi_{ss}} - \left(V_{gb} - V_{fb}\right) = 0$$

Solving the quadratic Equation 4.103 we can show

$$\phi_{ss} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gb} - V_{fb}}\right)^2 \tag{4.104}$$

Equation 4.104 shows that ϕ_{ss} is almost linearly dependent on $V_{gb} = V_{gs}$ for $V_{sb} = 0$. It should be emphasized that ϕ_{ss} is a constant in the subthreshold region for long channel devices only. As the channel length becomes shorter, ϕ_{ss} no longer remains constant over the entire channel length.

Since ϕ_{ss} is a constant, $E_y = -d\phi_{ss}/dy = 0$. Therefore, the only current that can flow is the diffusion current as can be seen from Equation 4.16 and is given by

$$J_n(x,y) = qD_n\frac{dn}{dy} = q\left(\mu_s v_{kT}\right)\frac{dn}{dy} \tag{4.105}$$

where from Einstein relation $D_n = \mu_s v_{kT}$. Integrating $J_n(x,y)$ from $x = 0$ at the Si/SiO_2 interface to $x = X_{inv}$ at the end of the inversion layer width, we get for an nMOSFET device of channel length, L, and width, W

$$I_{ds}(y) = W\int_0^{X_{inv}} q\left(\mu_s v_{kT}\right)\frac{dn}{dy} = W\mu_s v_{kT}\frac{d\left(qnX_{inv}\right)}{dy}$$
$$= W\mu_s v_{kT}\frac{dQ_i}{dy} \tag{4.106}$$

where:

$Q_i = qnX_{inv}$ is the inversion charge per unit area at any point y along the channel in the subthreshold region

Now, consider Q_{is} and Q_{id} are the inversion charge densities at $y = 0$ and $y = L$, respectively. Then integrating Equation 4.106 from ($y = 0$, $Q_i(y) = Q_{is}$) to ($y = L$, $Q_i(y) = Q_{id}$), we get

$$I_{ds} = \mu_s\left(\frac{W}{L}\right)v_{kT}\left(Q_{id} - Q_{is}\right) \tag{4.107}$$

Now, in order to calculate the subthreshold current from Equation 4.107, we need to find the inversion charge in the weak inversion regime, $\phi_B < \phi_s < 2\phi_B$. Again, we solve Poisson's equation to calculate Q_s and find an expression for Q_i in the weak inversion following the procedure in Chapter 3 (Equation 3.68). Then for MOSFETs in the weak inversion region, we can show

$$Q_s \cong -\sqrt{2qK_{si}\varepsilon_0 N_b\phi_{ss}}\left[1 + \frac{v_{kT}}{\phi_{ss}}e^{\left[\phi_{ss} - 2\phi_B - V_{ch}(y)\right]/v_{kT}}\right]^{1/2} \tag{4.108}$$

Let us assume that the exponential term in Equation 4.108 is much smaller than ϕ_{ss}. Then using series expansion $\sqrt{1+x} \cong 1 + (x/2)$, we get for the total charge Q_s in the substrate at weak inversion as

$$Q_s \cong -\sqrt{2qK_{si}\varepsilon_0 N_b\phi_{ss}}\left[1 + \frac{v_{kT}}{2\phi_{ss}}e^{\left[\phi_{ss} - 2\phi_B - V_{ch}(y)\right]/v_{kT}}\right]$$
$$= Q_b + \left(-\sqrt{\frac{qK_{si}\varepsilon_0 N_b}{2\phi_{ss}}}v_{kT}e^{\left[\phi_{ss} - 2\phi_B - V_{ch}(y)\right]/v_{kT}}\right) \tag{4.109}$$

where $Q_b = -\sqrt{2qK_{si}\varepsilon_0 N_b\phi_{ss}}$ as shown in Equation 3.64; since, $Q_s = Q_b + Q_i$, from Equation 4.109, the minority carrier charge density at the weak inversion region, $\phi_B < \phi_s < 2\phi_B$, of nMOSFETs is given by

$$Q_i = -\sqrt{\frac{qK_{si}\varepsilon_0 N_b}{2\phi_{ss}}}v_{kT}e^{\left[\phi_{ss} - 2\phi_B - V_{ch}(y)\right]/v_{kT}} \tag{4.110}$$

Again, from Equation 3.62, the width of the depletion region $X_d = \sqrt{2K_{si}\varepsilon_0\phi_{ss}/qN_b}$; then the depletion capacitance C_d ($=K_{si}\varepsilon_0/X_d$) is given by

$$C_d = \sqrt{\frac{qK_{si}\varepsilon_0 N_b}{2\phi_{ss}}} \tag{4.111}$$

Therefore, the charge density in the weak inversion region of nMOSFETs is given by

$$Q_i = -C_d v_{kT} e^{\left[\phi_{ss} - 2\phi_B - V_{ch}(y)\right]/v_{kT}} \tag{4.112}$$

Now, using the appropriate boundary conditions defined earlier

$$V_{ch}(y) = \begin{cases} V_{sb} & \text{at } y = 0 \quad \text{(source end)} \\ V_{sb} + V_{ds} & \text{at } y = L \quad \text{(drain end)} \end{cases}$$

We can write the expressions for the inversion charges from Equation 4.112 as

$$\begin{aligned} Q_{is} &= -C_d v_{kT} e^{\left[\phi_{ss} - 2\phi_B - V_{sb}\right]/v_{kT}} \\ Q_{id} &= -C_d v_{kT} e^{\left[\phi_{ss} - 2\phi_B - V_{sb} - V_{ds}\right]/v_{kT}} \end{aligned} \tag{4.113}$$

Now, substituting for Q_{is} and Q_{id} from Equation 4.113 in Equation 4.107, we get the expression for the subthreshold region current as

$$I_{ds} = \mu_s \left(\frac{W}{L}\right) C_d v_{kT}^2 e^{\left[\phi_{ss} - 2\phi_B - V_{sb}\right]/v_{kT}} \left(1 - e^{-(V_{ds}/v_{kT})}\right) \tag{4.114}$$

Since $\exp(-2\phi_B/v_{kT}) = n_i^2/N_b^2$, Equation 4.114 can also be expressed as

$$I_{ds} = \mu_s \left(\frac{W}{L}\right) C_d \left(v_{kT}\frac{n_i}{N_b}\right)^2 e^{(\phi_{ss} - V_{sb})/v_{kT}} \left(1 - e^{-(V_{ds}/v_{kT})}\right) \tag{4.115}$$

In order to eliminate ϕ_{ss} from Equation 4.115, we expand V_{gs} in a series around the point $\phi_{ss} = 2\phi_B$ (weak inversion corresponding to $\phi_B < \phi_s < 2\phi_B$). We define $V_{th} = V_{gs}$ @ $\phi_{ss} = 2\phi_B$ and $V_{sb} = 0$; therefore, $V_{gb} = V_{gs}$. Then by series expansion of V_{gs} around the point $\phi_{ss} = V_{sb} + 2\phi_B$ at the onset of inversion

$$V_{gs} = V_{gs}\Big|_{\phi_{ss} = V_{sb} + 2\phi_B} + \frac{dV_{gs}}{d\phi_{ss}}\left(\phi_{ss} - 2\phi_B - V_{sb}\right) \tag{4.116}$$

Since $V_{sb} = 0$ at $V_{gs} = V_{th}$, and $\phi_s = 2\phi_B$, by defining $n \equiv dV_{gs}/d\phi_{ss}$, we get from Equation 4.116

$$\begin{aligned} V_{gs} &= V_{th} + n\left(\phi_{ss} - 2\phi_B - V_{sb}\right) \\ \therefore \phi_{ss} - 2\phi_B - V_{sb} &= \frac{V_{gs} - V_{th}}{n} \end{aligned} \tag{4.117}$$

Then from Equation 4.114 we get for subthreshold region drain current model as

$$I_{ds} = \mu_s \left(\frac{W}{L}\right) C_d v_{kT}^2 e^{(V_{gs}-V_{th})/nv_{kT}} \left(1 - e^{-(V_{ds}/v_{kT})}\right) \tag{4.118}$$

where n is the ideality factor that can be determined from Equation 4.103. Using source referencing, we get

$$V_{gs} = V_{fb} + \phi_{ss} + \frac{\sqrt{2qK_{si}\varepsilon_0 N_b \phi_{ss}}}{C_{ox}} \tag{4.119}$$

Then, from Equation 4.119, we can show

$$\frac{dV_{gs}}{d\phi_{ss}} = 1 + \frac{1}{C_{ox}}\sqrt{\frac{qK_{si}\varepsilon_0 N_b}{2\phi_{ss}}} = 1 + \frac{C_d}{C_{ox}} \tag{4.120}$$

where we have used Equation 4.111 for C_d. Thus, we have

$$n = 1 + \frac{C_d}{C_{ox}} \tag{4.121}$$

From Equation 4.121, we get $C_d = (n-1)C_{ox}$. Therefore, we can express the subthreshold region current (Equation 4.118) in terms of C_d as well as C_{ox} as

$$I_{ds} = \begin{cases} \mu_s \left(\frac{W}{L}\right) C_d v_{kT}^2 e^{(V_{gs}-V_{th})/nv_{kT}} \left(1 - e^{-(V_{ds}/v_{kT})}\right) \\ \mu_s \left(\frac{W}{L}\right) (n-1) C_{ox} v_{kT}^2 e^{(V_{gs}-V_{th})/nv_{kT}} \left(1 - e^{-(V_{ds}/v_{kT})}\right) \end{cases} \tag{4.122}$$

From Equation 4.118 we note that in the subthreshold conduction

1. I_{ds} depends on V_{ds} only for small V_{ds}, that is, $V_{ds} \leq 3v_{kT}$, since $\exp(-V_{ds}/v_{kT}) \to 0$ for larger V_{ds}; therefore, for simplicity of device modeling, Equation 4.118 can be approximated to [31]

$$I_{ds} \cong \mu_s \left(\frac{W}{L}\right) C_d v_{kT}^2 e^{(V_{gs}-V_{th})/nv_{kT}} \tag{4.123}$$

2. I_{ds} depends exponentially on V_{gs} but with an *ideality factor* $n > 1$ (Equation 4.121); thus, the slope is poorer than a bipolar junction transistor (BJT) but approaches to that of a BJT in the limit $n \to 1$.
3. N_b and V_{bs} enter in the current model through depletion capacitance, C_d.
4. The subthreshold current (Equation 4.122) is strongly dependent on temperature T because of its dependence on the square of the intrinsic concentration n_i through Equation 4.115 and thermal voltage $v_{kT} = kT/q$.

Subthreshold slope: An important characteristic of the subthreshold region is the gate voltage swing required to reduce the current from its ON value to an acceptable OFF value. This gate voltage is also called the *subthreshold slope S* or *SS* or *S-factor*. It is the inverse of the slope of $I_{ds} - V_{gs}$ characteristics and is defined as the change in the gate voltage V_{gs} required to change the subthreshold current I_{ds} by one decade. Clearly, S is a measure of the turn-off characteristics of a MOSFET device. If we take two points (I_{ds1}, V_{gs1}) and (I_{ds2}, V_{gs2}) in the subthreshold region shown in Figure 4.15, then by definition ($V_{gs2} - V_{gs1}$) required to change (I_{ds2}/I_{ds1}) by one decade or 10 can be expressed as

$$S \equiv \frac{V_{gs2} - V_{gs1}}{\log I_{ds2} - \log I_{ds1}} = \frac{dV_{gs}}{d\left(\log I_{ds}\right)} = 2.3\frac{dV_{gs}}{d\left(\ln I_{ds}\right)} \tag{4.124}$$

where we have used $\left(\ln I_{ds}\right) = 2.3\left(\log I_{ds}\right)$ for the conversion of logarithm base "10" to natural logarithm base "e." In reality, S varies with I_{ds} in the subthreshold region; however, this variation is negligible over one decade of current so that S can be considered as a gate swing per decade of current change. Therefore, from Equation 4.122, we get

$$\ln I_{ds} = \ln\left(\frac{\mu_s W C_d v_{kT}^2}{L}\right) + \frac{V_{gs} - V_{th}}{n v_{kT}} + \ln\left(1 - e^{-(V_{ds}/v_{kT})}\right) \tag{4.125}$$

Then taking the derivative of Equation 4.125, we get

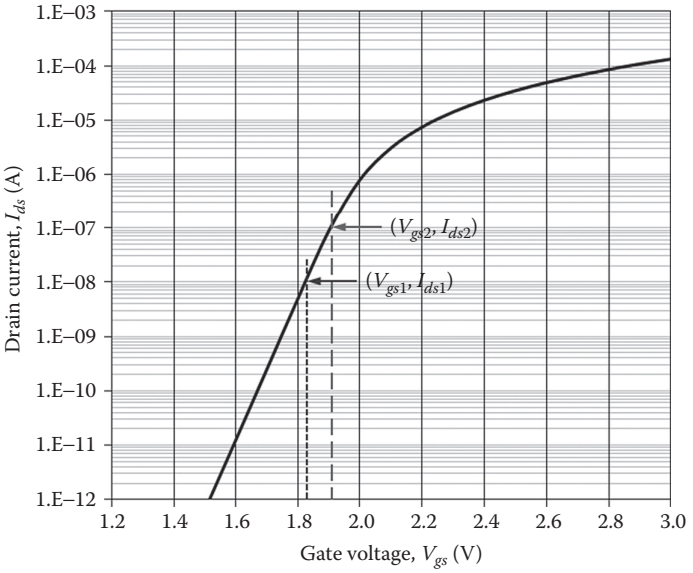

FIGURE 4.15
Log(I_{ds}) versus V_{gs} characteristics of a typical MOSFET device to calculate *S-factor*; the ratio of two data points in the subthreshold current is one decade.

$$d\left(\ln I_{ds}\right) = \frac{dV_{gs}}{nv_{kT}}$$

or (4.126)

$$\frac{dV_{gs}}{d\left(\ln I_{ds}\right)} = nv_{kT}$$

Therefore, combining Equations 4.124 and 4.126, we can show

$$S = 2.3nv_{kT} \tag{4.127}$$

Using Equation 4.121 for the ideality factor n, we get

$$S = 2.3v_{kT}\left(1 + \frac{C_d}{C_{ox}}\right) \tag{4.128}$$

Since at room temperature ($T \sim 300$ K), $v_{kT} \cong 26$ mV, Equation 4.128 shows that the theoretical minimum swing S_{min} is given by

$$S_{\min} = 2.3v_{kT} \cong 60\,\text{mV per decade} \tag{4.129}$$

Thus, the minimum attainable S for any device is approximately 60 mV per decade at room temperature. Since, $1 \le n \le 3$, the typical value of $60 \le S \le 180$ mV per decade at room temperature. If there is a substantial interface trap density, then C_d in Equation 4.121 should be replaced by $(C_d + C_{IT})$. Therefore,

$$S = 2.3v_{kT}\left(1 + \frac{C_d + C_{IT}}{C_{ox}}\right) \tag{4.130}$$

Final notes on subthreshold region conduction:

1. In weak inversion or subthreshold region, MOS devices have exponential characteristics but are less "efficient" than BJTs because $n > 1$.
2. Subthreshold slope S does not scale and is ≈ constant. Therefore, V_{th} cannot be scaled as required by the ideal scaling laws.
3. V_{ds} affects V_{th} as well as subthreshold currents.
4. In order to optimize S, the desirable parameters are:
   a. Thin oxide
   b. Low N_b
   c. High V_{bs}

4.4.4.5 Limitations of Regional Drain Current Model

In the regional drain current models developed in Section 4.4.4 we have assumed that in the subthreshold or weak inversion region I_{ds} is due to

diffusion component only and in the linear and saturation regions (strong inversion) I_{ds} is due to drift component only. This causes a discontinuity in the device characteristics during transition between these weak and strong inversion regions. This discontinuity is a severe drawback of the simplified model for implementation and usage in circuit CAD. To ensure continuity from weak to strong inversion, we consider that at the transition point, the inversion charge at weak and strong inversions are equal, that is, Q_i(weak inversion) = Q_i(strong inversion). Under this condition the gate voltage at the transition point at $V_{gs} = V_{on}$ can be shown to be [32]

$$V_{on} = V_{th} + nv_{kT} \tag{4.131}$$

From Equation 4.131, we find that the upper limit of subthreshold current is V_{on} instead of V_{th}; then replacing V_{th} by V_{on} in Equation 4.118, we can show

$$I_{ds} \cong I_{on} e^{\left(V_{gs}-V_{on}\right)/nv_{kT}} \tag{4.132}$$

where I_{on} is the on current calculated from (4.118) at $V_{gs} = V_{on}$ and is given by

$$I_{on} = \mu_s \left(\frac{W}{L}\right) C_d v_{kT}^2 \left(1 - e^{-\left(V_{ds}/v_{kT}\right)}\right) \tag{4.133}$$

Since in the subthreshold region I_{ds} is nearly independent of V_{ds}, we can safely neglect V_{ds} dependence in Equation 4.132 so that

$$I_{on} = \mu_s \left(\frac{W}{L}\right) C_d v_{kT}^2 \tag{4.134}$$

Thus, for $V_{gs} < V_{on}$, I_{ds} is given by Equation 4.132, whereas for $V_{gs} > V_{on}$, I_{ds} is given by Equation 4.100 with I_{on} from Equation 4.133. Thus, V_{on} acts as a point at which behaviors of strong and weak inversion are pieced together. This is the approach used in SPICE Levels 2 and 3. Combining Equations 4.100 and 4.132 we now have a complete long channel DC MOSFET model for circuit CAD, which is continuous in all regions,

$$I_{ds} = \begin{cases} I_{on} \exp\left(\dfrac{V_{gs} - V_{on}}{nv_{kT}}\right); & \left(V_{gs} - V_{on}\right) < 0 \\ \beta\left(V_{gs} - V_{th} - \dfrac{1}{2}\alpha V_{ds}\right) V_{ds}; & 0 < \left(V_{gs} - V_{th}\right) \geq V_{ds} \\ \dfrac{\beta}{2\alpha}\left(V_{gs} - V_{th}\right)^2; & 0 < \left(V_{gs} - V_{th}\right) \leq V_{ds} \end{cases} \tag{4.135}$$

Although Equation 4.135 results in a continuous transition of device characteristics from weak to strong inversion, there are large errors in the I_{ds} calculations around the transitions region, often called the moderate

inversion region [25]. However, for most of the digital applications this error is not significant due to the low magnitude of the current in this region. There are other approaches reported, which could be used to achieve better simulation results [30]. However, the improvement is not significant.

4.5 Summary

In this chapter we have introduced the four terminal MOSFET devices. The basic features of MOSFETs are described. A number of simplified assumptions are used to derive threshold voltage model for long channel devices. The fundamental Pao-Sah double-integral model and Brews charge-sheet model are derived to characterize MOSFET devices. We have discussed that the Pao-Sah and Brews models are computationally intensive to use for VLSI circuit analysis with billions of transistors in an IC chip. We have used simplified assumptions to derive the first-generation SPICE models for long channel devices. In these basic models, we have discussed how different equations for different regions of device operation are pieced together using smoothing functions.

The advantages of the simplified regional models include easy implementation of physical effects using empirical relations and fast computation time. On the other hand, the disadvantages include assumption of a constant ϕ_s ($=2\phi_B$) in strong inversion, resulting in an inaccurate modeling of moderate inversion, particularly, capacitances; and the model ignores inversion layer thickness and small geometry effects. However, the basic model is widely used for intuitive analysis of device performance.

Exercises

4.1 Pao-Sah model:

a. Complete the mathematical steps to derive Pao-Sah model given by Equation 4.36. Clearly define all parameters and explain.

b. To calculate MOSFET drain current using Pao-Sah model from Equation 4.36, the surface potential is numerically calculated from Equation 4.37. However, Equation 4.37 is derived assuming strong inversion only. Derive an accurate expression similar to Equation 4.37, which is valid in all regions of MOSFET operation.

4.2 For a device with p-type substrate concentration, $N_a = 2.5 \times 10^{16}$ cm^{-3}; gate oxide thickness, $T_{ox} = 100$ A; and $V_{fb} = -0.97$ V, calculate and plot $\ln(Q_i)$ versus V_{gb} in weak inversion.

4.3 Brews charge-sheet model:

a. Carry out the integration to derive the simplified surface potential based MOSFET drain current (Brews) model Equations 4.48 and 4.51.

b. Derive an expression for ϕ_{s0} in terms of the source-to-body bias V_{sb} to calculate I–V characteristics of the drift and diffusion components of I_{ds} for the above model. Clearly define all parameters and explain.

c. Derive an expression for ϕ_{sL} in terms of drain-to-body bias V_{db} to calculate I–V characteristics of the drift and diffusion components of I_{ds} for the above model.

Clearly define all parameters and explain.

4.4 Consider an nMOSFET device with $N_a = 5 \times 10^{17}$ cm^{-3}, $T_{ox} = 6$ nm, $V_{fb} = -1$ V, $\mu = 600$ cm^2 V^{-1}sec^{-1}, $W = L = 2$ μm, biased with $V_{sb} = 1$ V and $V_{db} = 3$ V, while V_{gb} is varied from 0 to 3 V. Use (Brews model) to calculate the following I_{ds} as a function of V_{gb}:

a. Drift component of I_{ds}, $I_{ds,drift}$

b. Diffusion component of I_{ds}, $I_{ds,diff}$

c. Total current I_{ds}

d. Plot I_{ds}–V_{gb} from part (a)–(c) using the same log drain current I_{ds} axis

e. Plot surface potentials (ϕ_{s0} and ϕ_{sL}) as a function of $(V_{gb} - V_{fb})$

4.5 Consider Basic MOS models. Explain physically why I–V characteristics of MOSFETs are more sensitive to temperature in the subthreshold region than they are in the strong inversion.

4.6 Show that in the subthreshold region of MOSFETs, the surface potential is given by:

$$\phi_{ss} = \left[-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gb} - V_{fb}} \right]^2$$

4.7 In weak inversion, the drain current I_{ds} is exponentially proportional to an inverse of (60 mV dec I^{-1})$(1 + C_d/C_{ox})$ at room temperature. Once strong inversion is reached, most of the gate charge resulting from higher V_{gs} value is balanced by channel charge Q_i not depletion charge. Write a simple expression, analogous to the slope expression above, which approximately models the MOSFET devices in strong inversion.

State any assumptions you make and explain your results.

4.8 Consider an MOS transistor on a uniformly doped *p*-type silicon substrate with doping concentration $N_a = 1\times10^{16}\,\text{cm}^{-3}$ at room temperature and $W = L = 10\ \mu\text{m}$. Assume $V_{fb} = 0$, $T_{ox} = 20$ nm; threshold voltage, $V_{th} = 0.7$ V, electron mobility = 600 $\text{cm}^2\,\text{V}^{-1}\,\text{sec}^{-1}$; $\lambda = 0.01\ \text{V}^{-1}$

a. Calculate and plot I_{ds} versus V_{ds} for $0.0 \le V_{ds} \le 5.0$ V with $V_{gs} = 2$, 3, 4 and 5 V on the same plot using following equations at different limits of V_{gs} shown:

i. $I_{ds} = \beta\left[V_{gs} - V_{th} - \left(V_{ds}/2\right)\right]V_{ds}$; for $V_{gs} > V_{th}$ and $V_{ds} \le \left(V_{gs} - V_{th}\right)$

ii. $I_{ds} = \left(\beta/2\right)\left(V_{gs} - V_{th}\right)^2$; for $V_{gs} > V_{th}$ and $V_{ds} \ge \left(V_{gs} - V_{th}\right)$

iii. $I_{ds} = \left(\beta/2\right)\left(V_{gs} - V_{th}\right)^2\left(1 + \lambda V_{ds}\right)$; for $V_{gs} > V_{th}$ and $V_{ds} \ge \left(V_{gs} - V_{th}\right)$

iv. Superimpose I_{dsat} versus V_{dsat} on the same plot;

where $\beta = \mu_s C_{ox}\left(W/L\right)$; clearly, label different operating regimes all different operating regions of MOSFETs and explain

4.9 Measured device data for a silicon nMOSFET are shown in Table E4.1 Considering the bulk-charge effect (α) in drain current I_{ds} calculate:

a. V_{th0}

b. λ

c. γ

d. β

using regional drain current model

4.10 In Section 4.4.4.4, the subthreshold region drain current is modeled using inversion charge at the source and drain ends. In this exercise, formulate the subthreshold region drain current (I_{ds}) model using the inversion carrier density at the source end $n(0)$ and drain end $n(L)$. Clearly state any assumptions you make.

a. Write an expression for the subthreshold region I_{ds} from Fick's first law of diffusion; assume that the concentration gradient of inversion carriers $\left(dn/dy\right)$ is constant along the channel to maintain a constant current flow through the device.

TABLE E4.1

Measurement Data to Extract the Basic nMOSFET Device Model Parameters

V_{gs} (V)	V_{ds} (V)	V_{bs} (V)	I_{ds} (mA)
2	5	0	40
5	5	0	536
5	5	−5	360
5	8	0	644
5	5	−3	420

b. Write down the expressions for the inversion carrier density $n(0)$ and $n(L)$ in terms of the surface potential ϕ_{ss}, bulk potential ϕ_B, and the appropriate channel potential $V_{ch}(y)$ at the respective terminal.

c. Assuming that the depth of the inversion layer is given by $X_{inv} = v_{kT}\sqrt{K_{si}\varepsilon_0/2qN_b\phi_{ss}}$, show that the subthreshold region drain current is given by Equation 4.114; where the parameters have their usual meanings as described in Section 4.4.4.4.

d. Following the procedure in Section 4.4.4.4, show that I_{ds} is given by Equation 4.118.

e. In the subthreshold region, a MOSFET device includes an oxide capacitor C_{ox} in series with a depletion capacitor C_d and any change in gate voltage V_{gs} causes corresponding change in ϕ_{ss}; consider a voltage divider between C_{ox} and C_d, and show that the ideality factor n is given by Equation 4.121.

f. Show that the final I_{ds} in the subthreshold region is given by Equation 4.122.