6

MOSFET Capacitance Models

6.1 Introduction

This chapter presents the dynamic compact MOSFET (metal-oxide-semiconductor field-effect transistor) models for analyzing the device performance under time-varying terminal voltages in circuit operation. The MOSFET device models developed in Chapters 4 and 5 are applicable to devices under DC or steady-state biasing condition, that is, when the terminal voltages do not vary with time. However, the real circuit operates under time-varying terminal voltages. Under such biasing condition, the device behavior is described by dynamic models. If the rate of change of terminal voltages is sufficiently small, the device operation can be described by a *small signal dynamic model*. On the other hand, if the rate of change of terminal voltages is large, the device is represented by a *large signal dynamic model*. In dynamic models, the device is represented by capacitors, resistors, current sources, and so on. The dynamic MOSFET models are essential part of circuit CAD (computer-aided design).

The dynamic operations of MOSFET devices are due to the capacitive effects of the device, resulting from the stored charges in the device. Thus, a capacitance model describing the intrinsic and extrinsic components of the device capacitance is an essential part of a compact model for circuit simulation besides DC model. In most circuit simulators, the same capacitance model is used for both the small signal AC analysis and the large signal transient analysis. A capacitance model is always based on *quasistatic assumptions*, that is, charge in a device can follow the varying terminal voltage instantaneously without any delay. In this chapter, first of all, a large signal dynamic model is described by developing models for intrinsic charges and capacitances of a large geometry device (large L and wide W). Then the models for short channel devices are discussed. Finally, the small signal linear model parameters required for small signal analysis are discussed.

6.2 Basic MOSFET Capacitance Model

The various capacitances present within an *n*-channel MOSFET are shown in Figure 6.1. The MOS transistor capacitances are categorically divided into two components: intrinsic and extrinsic, as shown in Figure 6.1. The region between the metallurgical source and drain junctions where the gate to source-drain (S/D) region is at flat band voltage is referred to as the intrinsic region.

- Intrinsic capacitances are between S/D metallurgical junctions.
- Extrinsic capacitances are outside the intrinsic part.

The extrinsic capacitances are divided into five components as shown in Figure 6.1. These are:

1. Outer fringing capacitances between the gate and the S/D region, C_{FO}
2. Inner fringing capacitances between the gate and the S/D region, C_{FI}
3. The overlap capacitances between the gate and heavily doped S/D regions C_{GSO} and C_{GDO} and between the gate and bulk region, C_{GBO} (not shown in Figure 6.1)
4. Overlap capacitances between the gate and the lightly doped S/D regions C_{GSL}, C_{GDL} (not shown in Figure 6.1)
5. S/D junction capacitances C_{JS} and C_{JD}

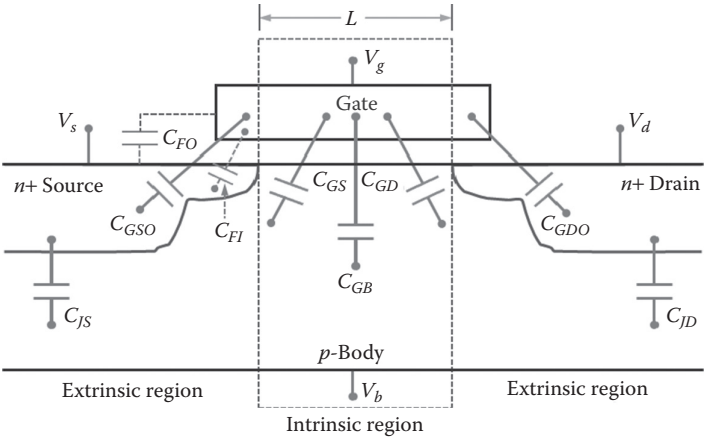

FIGURE 6.1
MOSFET capacitances: intrinsic capacitances between the S/D metallurgical junctions; extrinsic capacitances include overlap, fringing, and junction capacitances outside the active area of the device.

6.2.1 Intrinsic Charges and Capacitances

In a typical steady-state operation, the current flow through a MOSFET device is due to the transport of the mobile carriers (e.g., electrons in *n*-channel MOSFETs or nMOSFETs and holes in *p*-channel MOSFETs or pMOSFETs) from the source to drain under the applied drain voltage. This current is referred to as the *transport current* in transient analysis. In a dynamic operation, additional currents flow through the device due to the stored charges at the device terminals and are called the charging currents as shown in Figure 6.2.

Figure 6.2a shows the transient or dynamic currents i_g, i_s, i_d, and i_b flowing through the gate (g), source (s), drain (d), and bulk (b) terminals, respectively, of a MOSFET device. In Figure 6.2a, Q_G, Q_S, Q_D, and Q_B are the total gate, source, drain, and bulk charges, respectively, corresponding to four terminals of the MOSFET. These terminal charges are functions of the gate, source, drain, and bulk terminal voltages V_g, V_s, V_d, and V_b, respectively. Thus, in general

$$Q_j = f\left(V_g, V_s, V_d, V_b\right), \quad \text{where } j = G, S, D, B \tag{6.1}$$

From Kirchhoff's current law (KCL) for the total current, we have

$$i_g + i_s + i_d + i_b = 0 \tag{6.2}$$

and from the law of conservation of charge, we have

$$Q_G + Q_S + Q_D + Q_B = 0 \tag{6.3}$$

In order to calculate various charges of a MOSFET device, we assume *quasi-static operation* of the device [1]. In quasistatic operation, the terminal voltages are assumed to vary sufficiently slowly so that the distribution in the stored

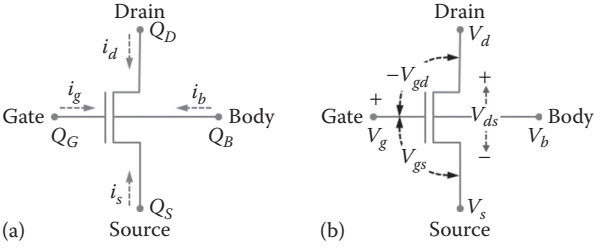

FIGURE 6.2
Schematic of a MOSFET as a circuit element: (a) transient currents i_g, i_s, i_d, and i_b flowing through the gate, source, drain, and body terminals, respectively and (b) terminal DC voltages, V_g, V_d, V_s and V_b at the gate, drain, source, and body terminals, respectively, where $V_{ds} = V_{gs} - V_{gd}$.

charges Q_G, Q_S, Q_D, and Q_B can follow the voltage variations. This implies that the terminal currents vary instantaneously with the terminal voltages. Thus, at any time t the charge per unit area is due to dynamic and DC operation is the same. The dynamic model developed by quasistatic assumption is called the *quasistatic model*. In practice, the quasistatic model works quite well for much of the circuit CAD. However, *this approach may fail, especially with long channel devices operating at high switching speeds, or when the load capacitance is very small*.

Assuming quasistatic operation, the total transient current at each terminal can be expressed as the sum of the time-dependent transport current and a charging current as

$$\begin{aligned} i_s(t) &= -I_s\left[V(t)\right] + \frac{dQ_S}{dt} \\ i_d(t) &= -I_d\left[V(t)\right] + \frac{dQ_D}{dt} \\ i_g(t) &= \frac{dQ_G}{dt} \\ i_b(t) &= \frac{dQ_B}{dt} \end{aligned} \tag{6.4}$$

where we assumed that no transport current is flowing to the gate ($I_g = 0$) and substrate ($I_b = 0$). In Equation 6.4, we have assumed that Q_S and Q_D are known. However, we only know the total inversion or channel charge Q_I so that

$$\begin{aligned} i_s(t) &= -I_s\left[V(t)\right] + \frac{dQ_S}{dt} \\ i_s + i_d &= I_{ds}\left[V(t)\right] + \frac{dQ_I}{dt} \end{aligned} \tag{6.5}$$

However, Equation 6.5 is unsuitable for circuit simulation, since circuit CAD requires separate expressions for i_s and i_d. Thus, in order to develop a dynamic MOSFET model for circuit CAD, it is necessary to derive expressions for Q_G, Q_B, and Q_I as functions of terminal voltages.

In order to derive the expressions for Q_G, Q_B, and Q_I as functions of terminal voltages, we use the corresponding known steady-state charges $Q_g(y)$, $Q_b(y)$, and $Q_i(y)$ per unit area at any point y along the length of the channel. By integrating these charges over the area of the active gate region we can obtain the corresponding total charge Q_G, Q_B, and Q_I. Now, the gate charge contained in a small area of device width W and length dy is $Q_g \cdot W \cdot dy$. Then integrating this charge over the channel length L gives the total gate charge Q_G as

$$Q_G = W\int_0^L Q_g(y)dy \tag{6.6}$$

Similarly, we can show

$$\begin{aligned} Q_I &= W\int_0^L Q_i(y)dy \\ Q_B &= W\int_0^L Q_b(y)dy \end{aligned} \tag{6.7}$$

Again, from the charge conservation principle,

$$Q_G + Q_I + Q_B = 0 \tag{6.8}$$

In Equation 6.8, we have neglected the total oxide charge (Q_o) since $Q_G >> Q_o$. In Equations 6.6 and 6.7, Q_G, Q_I, and Q_B are distributed charges. Therefore, the corresponding intrinsic capacitances must be modeled as distributed capacitances. However, such a model is not suitable for circuit CAD. Thus, for the simplicity of circuit CAD, these distributed capacitances are usually modeled as lumped two-terminal capacitances appearing between the gate, source, drain, and bulk or substrate terminals of a MOSFET. The Meyer model is one of such lumped capacitance model that is widely implemented in many circuit simulation tools [2].

The Meyer model was derived for long channel MOSFET devices. The most serious error in the model is that it violates the law of charge conservation [3]. However, due to the inherent simplicity of the Meyer model, it has been extensively used in simulating circuits that do not have charge conservation problems. The Meyer model is the default capacitance model for SPICE (Simulation Program with Integrated Circuit Emphasis) Levels 1–4. In order to overcome the deficiencies in the Meyer model, charge is used as a state variable in capacitance modeling. This is known as charge-based capacitance models [4–9]. We will first discuss the Meyer model and then develop a more accurate charge-based capacitance model.

6.2.2 Meyer Model

In Meyer model the distributed gate-channel capacitances are split into three lumped capacitances: gate to source (C_{GS}), gate to drain (C_{GD}), and gate to

bulk (C_{GB}). These are defined as the derivative of the total gate charge Q_G with respect to the source, drain, and bulk [Figure 6.2b], respectively, as given next:

$$C_{GS} = \left.\frac{\partial Q_G}{\partial V_{gs}}\right|_{V_{gd},gb}$$

$$C_{GD} = \left.\frac{\partial Q_G}{\partial V_{gd}}\right|_{V_{gs},gb} \tag{6.9}$$

$$C_{GB} = \left.\frac{\partial Q_G}{\partial V_{gb}}\right|_{V_{gs},gd}$$

where:
$V_{gd} = (V_{gs} - V_{ds})$
$V_{gb} = (V_{gs} - V_{bs})$

It is seen that the capacitances defined in Equation 6.9 imply that these capacitances are reciprocal; that is, both terminals of a capacitor are equivalent and the capacitance is symmetric, for example: $C_{GD} = C_{DG}$. In this case, the change in the charge Q_G due to V_{gd} may be due to the change either in the gate voltage V_g or in the drain voltage V_d. In Meyer model, the following assumptions are used to derive the capacitances:

1. MOSFET capacitances are reciprocal, that is, $C_{GB} = C_{BG}$, $C_{GD} = C_{DG}$, and $C_{GS} = C_{SG}$.
2. The bulk charge Q_b is constant along the length of the channel depending only on the applied bias V_{gb} and independent of V_{ds}. Thus, bulk-source (C_{BS}) and bulk-drain (C_{BD}) capacitances are zero.

From the law of conservation of charge given in Equation 6.8, we can express the total gate charge as

$$Q_G = -(Q_I + Q_B) = -W\int_0^L Q_i(y)dy - W\int_0^L Q_b(y)dy \tag{6.10}$$

where we have used the expressions for Q_I and Q_B from Equation 6.7. By assumption 2, the bulk charge density Q_b is a constant along the length of the channel and can be taken out of the integral. Thus, Equation 6.10 becomes

$$Q_G = -W\int_0^L Q_i(y)dy - Q_B \tag{6.11}$$

where:
$Q_B = WLQ_b$

Equation 6.11 is the generalized expression for Q_G in a MOSFET device. In order to calculate Q_G from Equation 6.11, any expression for Q_i used to calculate I_{ds} can be used. However, in deriving the Meyer intrinsic capacitance model, long channel expressions for Q_i and Q_b from Chapter 4 are used to derive Q_G and the capacitances in the different mode of operations of MOSFET devices as described next.

6.2.2.1 Strong Inversion

From Equations 4.68 and 4.70, the expressions for Q_b and Q_i, respectively, for long channel MOSFETs are given by

$$Q_b(y) = -\gamma C_{ox}\sqrt{2\phi_B + V_{sb}} \tag{6.12}$$

$$Q_i(y) = -C_{ox}\left[V_{gs} - V_{th} - V(y)\right] \tag{6.13}$$

where:
C_{ox} is the gate oxide capacitance per unit area
V_{th} is the threshold voltage
$V(y)$ is the voltage at any point y along the length of the channel from the source to drain

Since Q_i is a function of V, to integrate Equation 6.11 we first change the variable of integration from dy to dV using Equation 4.63 so that

$$dy = -\frac{W\mu_s}{I_{ds}}Q_i(y)dV \tag{6.14}$$

Now, combining Equations 6.11 through 6.14, we can show

$$Q_G = \frac{W^2\mu_s C_{ox}^2}{I_{ds}}\int_0^{V_{ds}}\left(V_{gs} - V_{th} - V\right)^2 dV - Q_B \tag{6.15}$$

where the limits of integration change from $y = 0$ to $V(y) = 0$, and $y = L$ to $V(y) = V_{ds}$. Again, using Q_i from Equations 6.13 through 6.14 and integrating the resulting expression from source to drain, we get the expression for I_{ds} (Equation 4.72)

$$I_{ds} = \mu_s C_{ox}\left(\frac{W}{L}\right)\left[V_{gs} - V_{th} - \frac{V_{ds}}{2}\right]V_{ds}; \quad V_{gs} > V_{th} \tag{6.16}$$

Now, from Figure 6.2b we get, $V_{ds} = (V_{gs} - V_{gd})$; then substituting for $V_{ds} = (V_{gs} - V_{gd})$ in Equation 6.16 we can write

$$\begin{aligned} I_{ds} &= \mu_s C_{ox}\left(\frac{W}{2L}\right)\left[2V_{gs} - 2V_{th} - \left(V_{gs} - V_{gd}\right)\right]\left(V_{gs} - V_{gd}\right) \\ &= \mu_s C_{ox}\left(\frac{W}{2L}\right)\left[\left(V_{gs} - V_{th}\right) + \left(V_{gd} - V_{th}\right)\right]\cdot\left[\left(V_{gs} - V_{th}\right) - \left(V_{gd} - V_{th}\right)\right] \\ &= \frac{W\mu_s C_{ox}}{2L}\left[\left(V_{gs} - V_{th}\right)^2 - \left(V_{gd} - V_{th}\right)^2\right] \end{aligned} \tag{6.17}$$

Now, substituting for I_{ds} from Equation 6.17 to Equation 6.15, we get

$$\begin{aligned} Q_G &= \frac{2WLC_{ox}}{\left(V_{gs} - V_{th}\right)^2 - \left(V_{gd} - V_{th}\right)^2}\int_0^{V_{ds}}\left(V_{gs} - V_{th} - V(y)\right)^2 dV - Q_B \\ &= \frac{2}{3}WLC_{ox}\left[\frac{\left(V_{gs} - V_{th} - V_{ds}\right)^3 - \left(V_{gs} - V_{th}\right)^3}{\left(V_{gd} - V_{th}\right)^2 - \left(V_{gs} - V_{th}\right)^2}\right] - Q_B \\ &= \frac{2}{3}WLC_{ox}\left[\frac{\left(V_{gd} - V_{th}\right)^3 - \left(V_{gs} - V_{th}\right)^3}{\left(V_{gd} - V_{th}\right)^2 - \left(V_{gs} - V_{th}\right)^2}\right] - Q_B \end{aligned} \tag{6.18}$$

where we have used $(V_{gs} - V_{ds}) = V_{gd}$ from Figure 6.2b. Then differentiating Equation 6.18 with respect to V_{gs}, V_{gd}, and V_{gb}, we obtain the intrinsic capacitance C_{GS}, C_{GD}, and C_{GB}, respectively, in the different operation regions of MOSFETs.

In the *linear region*, we get the expressions for the intrinsic capacitances from Equation 6.18 as

$$\begin{aligned} C_{GS} &= \frac{\partial Q_G}{\partial V_{gs}} = \frac{2}{3}WLC_{ox}\left[1 - \frac{\left(V_{gd} - V_{th}\right)^2}{\left(V_{gd} + V_{gs} - 2V_{th}\right)^2}\right] \\ C_{GD} &= \frac{\partial Q_G}{\partial V_{gd}} = \frac{2}{3}WLC_{ox}\left[1 - \frac{\left(V_{gs} - V_{th}\right)^2}{\left(V_{gd} + V_{gs} - 2V_{th}\right)^2}\right] \\ C_{GB} &= \frac{\partial Q_G}{\partial V_{gb}} = 0 \end{aligned} \tag{6.19}$$

Note that $C_{GB} = 0$ in the strong inversion is expected since the inversion charge in the channel from S to D shields the gate from the bulk and, therefore, prevents any response of Q_G due to substrate bias V_{bs}. Let us define $V_{gt} = V_{gs} - V_{th}$; then using $V_{gs} - V_{ds} = V_{gd}$ (Figure 6.2b), Equation 6.19 can be expressed as

$$\begin{aligned} C_{GS} &= \frac{\partial Q_G}{\partial V_{gs}} = \frac{2}{3} WLC_{ox}\left[1-\left(\frac{V_{gt}-V_{ds}}{2V_{gt}-V_{ds}}\right)^2\right] \\ C_{GD} &= \frac{\partial Q_G}{\partial V_{gd}} = \frac{2}{3} WLC_{ox}\left[1-\left(\frac{V_{gt}}{2V_{gt}-V_{ds}}\right)^2\right] \\ C_{GB} &= \frac{\partial Q_G}{\partial V_{gb}} = 0 \end{aligned} \tag{6.20}$$

In the saturation regime, we can obtain the expression for Q_G by replacing V_{ds} in Equation 6.18 by V_{dsat}. We know that for a long channel device in saturation, $V_{dsat} = V_{gs} - V_{th}$, and from Figure 6.2b, we get: $V_{ds} = V_{gs} - V_{gd} = V_{dsat}$ $(=V_{gs} - V_{th})$. Therefore, in the saturation region, $V_{gd} = V_{th}$. Then, substituting for $V_{gd} = V_{th}$ in Equation 6.18, we get

$$\begin{aligned} Q_G &= \frac{2}{3} WLC_{ox}\left[\frac{(V_{th}-V_{th})^3-(V_{gs}-V_{th})^3}{(V_{th}-V_{th})^2-(V_{gs}-V_{th})^2}\right]-Q_B \\ &= \frac{2}{3} WLC_{ox}(V_{gs}-V_{th})-Q_B \end{aligned} \tag{6.21}$$

From Equation 6.21, we get the *saturation region* intrinsic capacitances at $V_{ds} > V_{dsat}$

$$\begin{aligned} C_{GS} &= \frac{\partial Q_G}{\partial V_{gs}} = \frac{2}{3} WLC_{ox} \\ C_{GD} &= \frac{\partial Q_G}{\partial V_{gd}} = 0 \\ C_{GB} &= \frac{\partial Q_G}{\partial V_{gb}} = 0 \end{aligned} \tag{6.22}$$

Note that the saturation region capacitances are independent of V_{ds}. Since, in saturation, the channel is pinched off at the drain end, it is electrically isolated from the drain. Thus, Q_G is not influenced by a change in V_{ds} and the capacitances are independent of V_{ds}.

6.2.2.2 Weak Inversion

In the weak inversion region ($V_{gs} < V_{th}$), $Q_i << Q_b$ so that Equation 6.11 becomes

$$Q_G = -Q_B = W\int_0^L Q_b(y)dy = WLQ_b \tag{6.23}$$

Under the depletion approximation, the depletion charge density in the bulk for long channel devices is given by (Equation 4.101)

$$Q_b = -C_{ox}\gamma\sqrt{\phi_{ss}} \tag{6.24}$$

where the surface potential ϕ_{ss} in weak inversion is given by Equation 4.104

$$\phi_{ss} = \left[-\left(\frac{\gamma}{2}\right) + \sqrt{\frac{\gamma^2}{4} + V_{gb} - V_{fb}}\right]^2 \tag{6.25}$$

Thus, ϕ_{ss}, is practically independent of the position y along the channel. This means that Q_b is independent of position along the channel. Therefore, using for Q_b from Equation 6.24 and ϕ_{ss} from Equation 6.25, we get the expression for the gate charge in weak inversion from Equation 6.23 as

$$Q_G = -Q_B = -\frac{1}{2}WLC_{ox}\gamma^2\left[1 - \sqrt{1 + \frac{4}{\gamma^2}\left(V_{gb} - V_{fb}\right)}\right] \tag{6.26}$$

Now, differentiating Equation 6.26 with respect V_{gb} gives the gate-to-bulk capacitance C_{GB} in the subthreshold or weak inversion region as

$$C_{GB} = \frac{\partial Q_G}{\partial V_{gb}} = \frac{WLC_{ox}}{\sqrt{1 + \left(4/\gamma^2\right)\left(V_{gb} - V_{fb}\right)}} \tag{6.27}$$

In deriving Equation 6.27, we assumed that γ is constant independent of V_{bs}. This is true only for a uniformly doped substrate. In reality, MOSFETs are nonuniformly doped and γ is bias dependent as discussed in Chapter 4. Therefore, appropriate value of γ and its derivative must be used for accurate modeling of C_{GB} in the weak inversion regime of MOSFETs. Since in weak inversion, Q_G does not depend on V_{ds}, we can safely write

$$\begin{aligned} C_{GS} &= \frac{\partial Q_G}{\partial V_{gs}} = 0 \\ C_{GD} &= \frac{\partial Q_G}{\partial V_{gd}} = 0 \end{aligned} \tag{6.28}$$

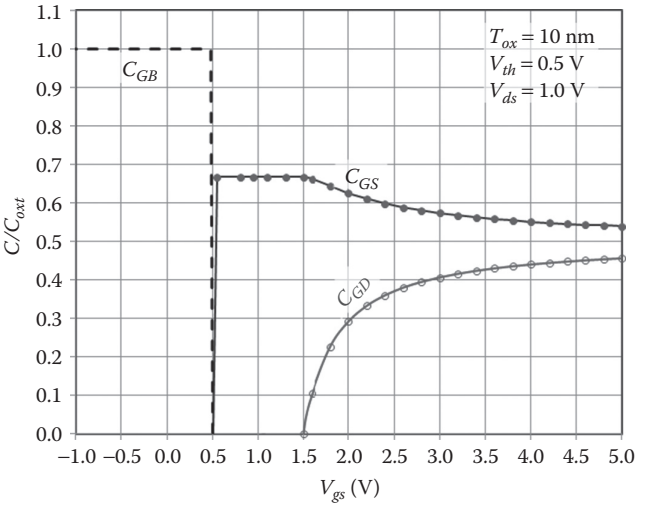

FIGURE 6.3
Plots of the intrinsic capacitances C_{GS}, C_{GD}, and C_{GB} associated with the gate terminal of MOSFET devices as a function of gate voltage V_{gs} for V_{ds} = 1 V; the plots are obtained by Equations 6.20, 6.22, and 6.27.

At $V_{gs} = V_{fb}$, the calculated value of C_{GB} from Equation 6.27 is not accurate due to the failure of the depletion approximation used in deriving Equation 6.27. However, because of the simplicity of calculation, Equation 6.27 is used for computing C_{GB} at weak inversion.

Figure 6.3 shows normalized plots of three capacitances as a function of V_{gs} for $V_{ds} = 1$. The capacitances are normalized with respect to the total gate capacitance given by

$$C_{oxt} = WLC_{ox} \tag{6.29}$$

Finally, the *accumulation* region capacitances are given by: $C_{GB} = C_{oxt}$, and $C_{GS} = 0 = C_{GD}$.

The gate capacitance C_{oxt} is the maximum capacitance of a MOSFET device that occurs in the accumulation condition. In the inversion region, that is, in the active mode of operation of the device, the maximum capacitance occurs in saturation and is equal to $(2/3)C_{oxt}$ as shown in Equation 6.22.

The Meyer model can be represented by a simple equivalent circuit as shown in Figure 6.4.

In Figure 6.4, C_{JS} and C_{JD} are the source-body and drain-body *pn*-junction capacitances, respectively.

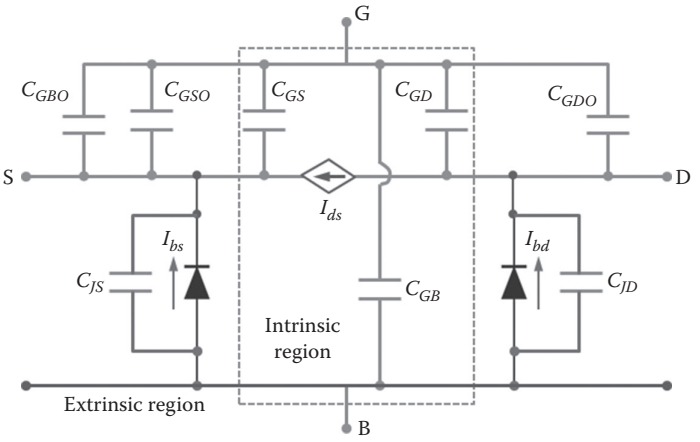

FIGURE 6.4
Complete equivalent circuit of a MOSFET device showing the extrinsic and Meyer's intrinsic capacitances.

6.2.3 Limitations of Meyer Model

The Meyer model is simple and predicts acceptable simulation results for most circuit analysis since its implementation in SPICE [10]. However, it is found to generate nonphysical simulation results when used to model circuits with charge storage nodes. The model incorrectly predicts the charge built up on these nodes in circuit simulation. It is found that the Meyer model is inadequate in predicting accurate capacitances in circuits such as MOS (metal-oxide-semiconductor) charge pumps [11], silicon on sapphire [4], dynamic random access memory, and switched-capacitor circuits [8]. This inaccuracy in simulation results when using the Meyer model is due the (1) charge nonconservation and (2) nonphysical reciprocity assumption.

The charge nonconservation problem has been extensively analyzed [8,11,12]. The detailed investigation of the Meyer model reveals that the incorrect implementation of the model in circuit CAD causes charge nonconservation [11]. However, in order to ensure charge conservation in modeling MOSFET capacitances, it is required to assign charges at each terminal of the device. With quasistatic assumption, the charges at any time t only depend on the values of the terminal voltages at the same time so that we can write

$$Q_j = Q_j\left(V_{gs}, V_{gd}, V_{gb}\right), \quad \text{where } j = G, S, D, B \tag{6.30}$$

Thus, the capacitance C_{ji} with $i = G$ (e.g., C_{GG}, C_{DG}, C_{SG}, and C_{BG}) in a MOSFET must satisfy the relation

$$C_{ji}\left(V_{gs}, V_{gd}, V_{gb}\right) \equiv \frac{dQ_j}{dV_g}, \quad \text{where } j = G, S, D, B; \text{ and } i = G \tag{6.31}$$

and the sum of the charges in the device must satisfy the law of charge conservation given by Equation 6.3, that is,

$$\sum_j Q_j = 0, \quad \text{where } j = G, S, D, B \tag{6.32}$$

In addition to the charge nonconservation problem, the assumption of capacitance reciprocity, $C_{ij} = C_{ji}$, in the Meyer model is more critical. It is shown that the assumption of reciprocity is inconsistent with the charge conservation law [13,14]. The detailed analysis shows that in order to ensure charge conservation principle, the reciprocity of the Meyer model requires Q_S to depend only on V_{gs} and Q_D to depend only on V_{gd}. This implies that $C_{GS} = C_{SG} \equiv dQ_S/dV_{gd}$ cannot be a function of V_{ds} or V_{bs} [14]. In reality, the channel charge can be modulated by both V_{ds} and V_{bs}. Therefore, the assumption of capacitance reciprocity is nonphysical. The nonreciprocal effect in MOSFETs is due to the fact that the channel charge is controlled by three or more terminal voltages. And, the reciprocal capacitors simply cannot be used to model the capacitive effects in a MOSFET device.

6.3 Charge-Based Capacitance Model

The charge-based capacitance modeling is one of the approaches to solve charge nonconservation problem in MOSFET capacitance modeling [4,15,16]. In this approach, the charges in the drain, gate, source, and bulk of a MOSFET are determined to use them as state variables in circuit simulation. Transient currents and the capacitances are obtained by differentiating the charges with respect to time and voltage, respectively. The charge-based capacitance model automatically ensures the charge conservation, as long as Equation 6.3 is satisfied, that is,

$$Q_G + Q_S + Q_D + Q_B = 0 \tag{6.33}$$

Since the terminal charge Q_j ($j = G, D, S, B$) is a function of terminal voltages V_g, V_s, V_d, and V_b, we can write the terminal current, i_j, as

$$i_j = \frac{dQ_j}{dt} = \frac{\partial Q_j}{\partial V_g}\frac{\partial V_g}{\partial t} + \frac{\partial Q_j}{\partial V_d}\frac{\partial V_d}{\partial t} + \frac{\partial Q_j}{\partial V_s}\frac{\partial V_s}{\partial t} + \frac{\partial Q_j}{\partial V_b}\frac{\partial V_b}{\partial t} \tag{6.34}$$

Equation 6.34 shows that each terminal of a MOSFET device has a capacitance with respect to the remaining three terminals. Thus, a four-terminal device has 16 capacitances that include 4 self-capacitances corresponding

to its four terminals and 12 nonreciprocal intrinsic capacitances. The 16 capacitances form the so called indefinite admittance matrix. Each element C_{ij} of this capacitance matrix describes the dependence of the charge at the terminal i with respect to the voltage applied at the terminal j with all other voltages held constant. For example, C_{GS} specifies the rate of change of Q_G with respect to the source voltage V_s keeping the voltages at the other terminals (V_g, V_d, and V_b) constant. Thus, in general

$$C_{ij} = \begin{cases} -\dfrac{\partial Q_i}{\partial V_j}, & i \neq j; \quad i, j = \text{G, S, D, B} \\ \dfrac{\partial Q_i}{\partial V_j}, & i = j \end{cases} \tag{6.35}$$

In Equation 6.35, the sign of any C_{ij} is chosen to keep all of the capacitance terms positive for well-behaved devices, that is, devices for which the charge at a node increases with an increase in the voltage at that node whereas decreases with an increase in the voltage at any other node. All 16 capacitances of the matrix C_{ij}, shown here, are not independent.

$$C_{ij} = \begin{bmatrix} C_{GG} & -C_{GD} & -C_{GS} & -C_{GB} \\ -C_{DG} & C_{DD} & -C_{DS} & -C_{DB} \\ -C_{SG} & -C_{SD} & C_{SS} & -C_{SB} \\ -C_{BG} & -C_{BD} & -C_{BS} & C_{BB} \end{bmatrix} \tag{6.36}$$

In Equation 6.36, each row must sum to zero for the matrix to be reference-independent and each column must sum to zero for the device description to be charge-conservative, which is equivalent to obeying KCL. One of these four capacitances, corresponding to each terminal of the device, is the self-capacitance, which is the sum of the remaining three capacitances. Thus, for example, the gate capacitance C_{GG} is given by

$$C_{GG} = C_{GS} + C_{GD} + C_{GB} \tag{6.37}$$

The 12 *inter-nodal* or *intrinsic capacitances* of a MOSFET device are also called the *trans-capacitances*. And, these capacitances are nonreciprocal. Thus, for example, C_{DG} and C_{GD} differ both in value and physical interpretation. Out of the 12 trans-capacitances, only 9 are independent: C_{GB}, C_{GS}, C_{GD}, C_{BG}, C_{BS}, C_{BD}, C_{DG}, C_{DS}, and C_{DB}. Therefore, if we evaluate the independent nine

capacitances, then the other three capacitances C_{SG}, C_{SD}, and C_{SB} can be determined from the following relations

$$\begin{aligned} C_{SG} &= C_{GB} + C_{GD} + C_{GS} - C_{BG} - C_{DG} \\ C_{SD} &= C_{BG} + C_{BD} + C_{BS} - C_{GB} - C_{DB} \\ C_{SB} &= C_{DG} + C_{DB} + C_{DS} - C_{GD} - C_{BD} \end{aligned} \tag{6.38}$$

Thus, it is evident from Equation 6.36 that to calculate MOSFET intrinsic capacitances we need to calculate the charges Q_G, Q_D, Q_S, and Q_B as a function of terminal voltages, and if we take these charges as independent state variables, then charge conservation will be guaranteed. Thus, charge-based capacitance model is obtained by integrating the terminal charges Q_G and Q_B given in Equations 6.6 and 6.7 over the length of the channel under the charge conservation principle given by Equation 6.8. Thus, Q_G and Q_B can be easily obtained by integrating the corresponding charge per unit area over the active gate region. However, Q_S and Q_D can only be determined from the channel charge Q_I, because both source and drain terminals are in intimate contact with the channel region. Therefore, it is necessary to partition the channel charge into charge Q_D associated with the drain terminal and a charge Q_S associated with the source terminal, such that

$$Q_I = Q_S + Q_D \tag{6.39}$$

Although this partition of Q_I into $(Q_S + Q_D)$ is not physically accurate, it does lead to MOSFET capacitance model, which agrees with the experimental results.

Channel Charge Partition: There are various approaches to partition Q_I into Q_S and Q_D [4–9,15–19]. These approaches vary from an equal division of Q_I across both terminals ($Q_S = Q_D = 0.5Q_I$) [7] to a Q_I multiplied by a "linear partitioning" or "weighted function" [4]. However, the channel-charge partition scheme proposed by Ward and Dutton [4] agrees very well with the experimental results.

The Ward–Dutton partition is derived from 1D (one-dimensional) continuity equation. Neglecting the generation-recombination in the channel region, 1D continuity equation (Equation 2.80 or 2.81) at a point y along the channel at any instant t can be expressed as

$$\frac{\partial I(y,t)}{\partial y} = -W\frac{\partial Q_i(y,t)}{\partial t} \tag{6.40}$$

Integrating Equation 6.40 along the channel from the source ($y = 0$) to an arbitrary point y along the channel, we get

$$\int_0^y \frac{\partial I(y',t)}{\partial y'} dy' = -W \int_0^y \frac{\partial Q_i(y',t)}{\partial t} dy'$$

or

$$I(y,t) - I(0,t) = -W \int_0^y \frac{\partial Q_i(y',t)}{\partial t} dy' \tag{6.41}$$

Again, integrating Equation 6.41 along the entire length of the channel, we get

$$\int_0^L I(y,t)dy - \int_0^L I(0,t)dy = -W \int_0^L \int_0^y \frac{\partial Q_i(y',t)}{\partial t} dy'dy \tag{6.42}$$

Since the integration is at any instant t, the right-hand side of the above equation can be rewritten by taking the time derivative outside the integral. Then integrating by parts and simplifying the resulted expression, we can show

$$I(0,t) = \frac{1}{L} \int_0^L I(y,t)dy + \frac{W}{L} \frac{\partial}{\partial t} \int_0^L \left(1 - \frac{y}{L}\right) Q_i dy \tag{6.43}$$

Equation 6.43 is the expression for the channel current at the position $y = 0$ at any time t, that is, the total current flowing through the source contact. The first term on the right-hand side is the average transport current in the channel at time t, that is, the DC current under quasistatic operation. Comparing Equation 6.43 with the expression for $i_s(t)$ in Equation 6.4, we find that the charge Q_S associated with the source is

$$Q_S = -W \int_0^L \left(1 - \frac{y}{L}\right) Q_i dy \tag{6.44}$$

An expression similar to Equation 6.43 can be derived for the drain current and the charge Q_D associated with the drain can be shown as

$$Q_D = -W \int_0^L \frac{y}{L} Q_i dy \tag{6.45}$$

Thus, we can now calculate the terminal charges Q_G, Q_B, Q_S, and Q_D from Equations 6.6, 6.7, 6.44, and 6.45, respectively, using the expression for Q_I from Equation 6.8 to ensure charge conservation. First of all, we will derive the charge expressions for the long channel devices and then modify those

charge expressions for short channel devices. In general, the expressions for Q_i and Q_b required for deriving the charge expressions (Equations 6.6 and 6.7) can be used from any DC current model for a MOSFET. However, in the following section, the widely used regional DC current model in circuit CAD tools is used to derive the expressions for charge-based capacitance model.

6.3.1 Long Channel Charge Model

In this section, the terminal charges are derived using the regional DC current model discussed in Section 4.4.4. Thus, similar to drain current model, the charge-based model also consists of different expressions for terminal charges for different regions of device operations.

6.3.1.1 Strong Inversion

In Equation 4.95, the channel charge density Q_i for a long channel MOSFET device is shown as

$$Q_i(y) = -C_{ox}\left[V_{gs} - V_{th} - \alpha V(y)\right] \tag{6.46}$$

and in Equation 4.91, the bulk-charge density for a long channel device is shown as

$$Q_b(y) = -C_{ox}\gamma\left[\delta V(y) + \sqrt{2\phi_B + V_{sb}}\right] \tag{6.47}$$

Since the total charge in the system must be zero, that is $Q_g + Q_i + Q_b = 0$, using Q_i and Q_b from Equations 6.46 and 6.47, respectively, we get

$$\begin{aligned} Q_g(y) &= C_{ox}\left[V_{gs} - V_{th} - \alpha V(y) + \delta\gamma V(y) + \gamma\sqrt{2\phi_B + V_{sb}}\right] \\ &= C_{ox}\left[V_{gs} - \left(V_{th} - \gamma\sqrt{2\phi_B + V_{sb}}\right) - (\alpha - \delta\gamma)V(y)\right] \end{aligned} \tag{6.48}$$

Now, from the threshold voltage (V_{th}) Equation 4.10 of a MOSFET device, we can show that $V_{th} - \gamma\sqrt{2\phi_B + V_{sb}} = V_{fb} + 2\phi_B$, and from Equation 4.96, we get, $(\alpha - \delta\gamma) = 1$. Then, Equation 6.48 can be expressed as

$$Q_g(y) = C_{ox}\left[V_{gs} - V_{fb} - 2\phi_B - V(y)\right] \tag{6.49}$$

Similarly, using Equations 4.10 and 4.96, Equation 6.47 can be expressed as

$$Q_b(y) = -C_{ox}\left[V_{th} - 2\phi_B - V_{fb} - (1-\alpha)V(y)\right] \tag{6.50}$$

Equations 6.46, 6.49, and 6.50 are used to calculate the terminal charges using Equations 6.6 and 6.7 along with Equations 6.44 and 6.45 for charge partitioning. Let us first calculate Q_S and Q_D using Equations 6.44 and 6.45, respectively. Since $Q_i(y)$ is known as a function of V, we first change the variable of integration dy in Equations 6.44 and 6.45 to dV using Equation 6.14 to get

$$\begin{aligned} Q_S &= -\frac{\mu_s W^2}{I_{ds}} \int_{V_s}^{V_d} \left(1 - \frac{y}{L}\right) Q_i \cdot Q_i dV \\ Q_D &= -\frac{\mu_s W^2}{I_{ds}} \int_{V_s}^{V_d} \frac{y}{L} Q_i \cdot Q_i dV \end{aligned} \tag{6.51}$$

To express y in terms of V_{ds} in Equation 6.51, we integrate Equation 6.14 from ($y = 0$, $V = V_s = 0$) to an arbitrary point (y, V) along the length of the channel using Equation 6.46 for Q_i. This yields

$$y = -\frac{W\mu_s}{I_{ds}} \int_0^V Q_i dV = \frac{\mu_s W C_{ox}}{I_{ds}} \left(V_{gs} - V_{th} - \frac{1}{2}\alpha V\right) V \tag{6.52}$$

At the drain end $y = L$ and $V = V_{ds}$ so that we have

$$I_{ds} = \mu_s C_{ox} \left(\frac{W}{L}\right) \left[V_{gs} - V_{th} - \frac{1}{2}\alpha V_{ds}\right] V_{ds}; \quad V_{gs} > V_{th} \tag{6.53}$$

Now combining Equation 6.51 with Equations 6.46 and 6.52 and carrying out the integration, we get after simplification the terminal charges in the *linear region* of device operation as

$$\begin{aligned} Q_D &= -WLC_{ox} \left[\frac{1}{2}\left(V_{gs} - V_{th}\right) - \frac{1}{3}\alpha V_{ds} + AB\right] \\ Q_S &= -WLC_{ox} \left[\frac{1}{2}\left(V_{gs} - V_{th}\right) - \frac{1}{6}\alpha V_{ds} + A(1 - B)\right] \end{aligned} \tag{6.54}$$

where the parameters A and B are defined as

$$\begin{aligned} A &= \frac{\alpha^2 V_{ds}^2}{12\left((V_{gs} - V_{th}) - (1/2)\alpha V_{ds}\right)} \\ B &= \frac{5(V_{gs} - V_{th}) - 2\alpha V_{ds}}{10\left((V_{gs} - V_{th}) - (1/2)\alpha V_{ds}\right)} \end{aligned} \tag{6.55}$$

When $V_{ds} = 0$, it is found from Equations 6.54 and 6.55, $Q_S = Q_D = (1/2)WLC_{ox}(V_{gs} - V_{th})$, which is obvious because of the symmetry.

The total gate charge Q_G can be obtained by integrating the gate charge density Q_g over the area of the active gate region as

$$Q_G = W\int_0^L Q_g(y)dy = \frac{\mu_s W^2}{I_{ds}}\int_0^{V_d} Q_g \cdot Q_i dV \tag{6.56}$$

where we have replaced the differential channel length *dy* with the corresponding differential potential drop *dV* using Equation 6.14. Substituting for Q_i and Q_g from Equations 6.46 and 6.49, respectively, and carrying out the integration results in the following expression for the charge Q_G, we get

$$Q_G = WLC_{ox}\left[V_{gs} - V_{fb} - 2\phi_B - \frac{1}{2}V_{ds} + \frac{A}{\alpha}\right] \tag{6.57}$$

Similarly, the total bulk charge Q_B can be written as

$$Q_B = W\int_0^L Q_b(y)dy = -\frac{\mu_s W^2}{I_{ds}}\int_0^{V_{ds}} Q_b \cdot Q_i dV \tag{6.58}$$

Again, substituting Q_i and Q_b from Equations 6.46 and 6.47 (or 6.50), respectively, and carrying out the integration yields

$$Q_B = -WLC_{ox}\left[\gamma\sqrt{2\phi_B + V_{sb}} - (1-\alpha)V_{ds}D\right] \tag{6.59}$$

where the parameter *D* is defined as

$$D = \frac{3\left(V_{gs} - V_{th}\right) - 2\alpha V_{ds}}{6\left[\left(V_{gs} - V_{th}\right) - (1/2)\alpha V_{ds}\right]} \tag{6.60}$$

It is seen from the first expression in Equation 6.59 that the bulk charge consists of two terms. The first term gives the total bulk charge due to the back bias V_{sb} and is related to the threshold voltage. The second term describes the additional charge induced by the drain bias. The second term reduces to zero when $V_{ds} = 0$.

It is very easy to verify that the sum of Q_G, Q_S, Q_D, and Q_B is zero.

Equations 6.54, 6.57, and 6.59 are the terminal charges for the *linear region* of the device operation. The corresponding charges in the *saturation region* are obtained by replacing V_{ds} by $V_{dsat} = \left(V_{gs} - V_{th}\right)/\alpha$ (Equation 4.98), in the

expressions for terminal charges in the linear region. Thus, the expressions for terminal charges Q_S, Q_D, Q_G, and Q_B in the *saturation region* are given by

$$\begin{aligned}
Q_D &= -\frac{4}{15} WLC_{ox}\left(V_{gs} - V_{th}\right) \\
Q_S &= -\frac{2}{5} WLC_{ox}\left(V_{gs} - V_{th}\right) \\
Q_G &= WLC_{ox}\left[V_{gs} - V_{fb} - 2\phi_B - \frac{1}{3\alpha}\left(V_{gs} - V_{th}\right)\right] \\
Q_B &= -WLC_{ox}\left[V_{th} - V_{fb} - 2\phi_B + \frac{1}{3\alpha}(1-\alpha)\left(V_{gs} - V_{th}\right)\right] \\
\therefore Q_I &= Q_s + Q_D = -\frac{2}{3} WLC_{ox}\left(V_{gs} - V_{th}\right)
\end{aligned} \tag{6.61}$$

It is observed from Equation 6.61 that the terminal charges in the saturation region are independent of V_{ds}. This is due to the fact that because of the channel pinch-off near the drain end of the device in saturation, the drain has no influence on the behavior of the device. Also, it is observed that the mobility degradation factor due to the gate field does not appear in the charge expressions. This is because of the global way of modeling the mobility, which cancels out while deriving the charges. Numerical device simulation results show that the mobility degradation has little effect on the terminal charges, thus validating the results obtained by analytical charge-based model [13].

6.3.1.2 Weak Inversion

In the weak inversion region of a MOSFET device, though the number of mobile charges at the interface is small, these charges are important for modeling the switching behavior of the device. Also, in this region, $Q_b >> Q_i$, and therefore, the bulk charges are not shielded by the inversion charge and behave differently compared to the strong inversion condition.

In order to derive expressions for the terminal charges in weak inversion, we assume that the current transport occurs by diffusion only as discussed in deriving the subthreshold drain current expression in Chapter 4. Indeed, this is a valid approximation for low gate voltages as discussed in Section 4.4.4.4. Then from Equation 4.106, the drain current at any point y along the channel is given by

$$I_{ds} = \mu_s W v_{kT} \frac{dQ_i}{dy} \tag{6.62}$$

Integrating Equation 6.62 from ($y = 0$, $Q_i = Q_{is}$) to any point (y, Q_i) along the channel and after simplification we can show

$$y = \frac{\mu_s W}{I_{ds}} v_{kT} \left(Q_i - Q_{is}\right) \tag{6.63}$$

where:
v_{kT} is the thermal voltage
Q_{is} is the mobile charge density at the source end

At the drain end of the channel $Q_i = Q_{id}$.

Let us first calculate the source and drain charge Q_S and Q_D, respectively. Substituting for dy and y from Equations 6.62 and 6.63, respectively, to the expression for Q_D in Equation 6.45, we get

$$Q_D = \frac{W}{L}\left(\frac{\mu_s W}{I_{ds}}\right)^2 v_{kT}^2 \int_{Q_{is}}^{Q_{id}} Q_i \left(Q_i - Q_{is}\right) dQ_i \tag{6.64}$$

which on integration and after simplification using Equation 6.62 for I_{ds} can be shown as

$$Q_D = \frac{1}{6} WL\left(2Q_{id} - Q_{is}\right) \tag{6.65}$$

Now, substituting for the charge densities Q_{is} and Q_{id} from Equation 4.113, we get the expression for the drain charge Q_D as

$$Q_D = -\frac{1}{6} WLC_d v_{kT} \exp\left(\frac{V_{gs} - V_{th}}{n v_{kT}}\right) \cdot \left[2\exp\left(-\frac{V_{ds}}{v_{kT}}\right) + 1\right] \tag{6.66}$$

where we have used Equation 4.117 to eliminate ϕ_B from the expressions for Q_{is} and Q_{id} in Equation 4.113. Equation 6.66 can also be expressed by using Equation 4.121 relating the depletion capacitance C_d and the ideality factor $n = \left[1 + \left(C_d / C_{ox}\right)\right]$ as

$$Q_D = -\frac{1}{6} WLC_{ox} (n-1) v_{kT} \exp\left(\frac{V_{gs} - V_{th}}{n v_{kT}}\right) \cdot \left[2\exp\left(-\frac{V_{ds}}{v_{kT}}\right) + 1\right] \tag{6.67}$$

Using similar procedures we can show that the expression for the source charge Q_S in the weak inversion region is given by

$$Q_S = -\frac{1}{6} WLC_{ox} (n-1) v_{kT} \exp\left(\frac{V_{gs} - V_{th}}{n v_{kT}}\right) \cdot \left[\exp\left(-\frac{V_{ds}}{v_{kT}}\right) + 2\right] \tag{6.68}$$

From Equations 6.67 and 6.68, we observe that at $V_{ds} = 0$ and $V_{gs} = V_{th}$, $Q_D = Q_S = 0.5\ WLC_{ox}(n-1)v_{kT}$. It is also observed from Equations 6.67 and 6.68 that Q_S and Q_D depend weakly on V_{ds}. This is due to fact that for V_{ds} greater than a few v_{kT}, the terms involving V_{ds} become negligible and therefore, $Q_S = 2Q_D$.

Since in weak inversion, the bulk charge Q_B is virtually independent of the S/D voltage V_{ds}, we can use Equation 6.24 for Q_B, which at the boundary of the strong inversion can be rewritten as

$$Q_B = -WLC_{ox}\gamma\sqrt{2\phi_B + V_{sb}} \tag{6.69}$$

Equation 6.69 is the same as the first term of the first expression in Equation 6.59. If the channel charge is assumed zero ($Q_I = 0$) in the subthreshold region, the gate charge becomes equal to the bulk charge. Thus, $Q_G = -Q_B$.

6.3.1.3 Accumulation

In the accumulation region of a MOSFET device operation, $V_{gb} < V_{fb}$; thus a thin layer of majority carriers are formed at the interface, forming a parallel plate capacitor with the gate. In this case, the bulk charge Q_B is simply written as

$$Q_B = -WLC_{ox}\left(V_{gs} + V_{sb} - V_{fb}\right) \tag{6.70}$$

Since there is no current flow, the gate charge is given by

$$Q_G = -Q_B = WLC_{ox}\left(V_{gs} + V_{sb} - V_{fb}\right) \tag{6.71}$$

6.3.2 Long Channel Capacitance Model

We can now derive the expressions for capacitances associated with a MOSFET using the equations derived for various charges in different regions of device operation and the definition of C_{ij} in Equation 6.35. The mathematics to derive 12 capacitances is basic, however involved and long. It is left as an exercise for the readers.

The expressions for C_{GD} and C_{DG} in the *linear region* are obtained by differentiating Q_G (Equation 6.57) with respect to V_d (or V_{ds}) and Q_D (Equation 6.54) with respect to V_g or V_{gs}, respectively, and using A and B defined in Equation 6.55, that is,

$$\begin{aligned} C_{GD} &= -\frac{\partial Q_G}{\partial V_d} = \frac{1}{2}WLC_{ox}\left[-1 + \frac{1}{\left(V_{gs} - V_{th}\right) - (1/2)\alpha V_{ds}}\left(A + \frac{1}{3}\alpha V_{ds}\right)\right] \\ C_{DG} &= -\frac{\partial Q_D}{\partial V_g} = \frac{1}{2}WLC_{ox}\left[1 + \frac{A}{\left(V_{gs} - V_{th}\right) - (1/2)\alpha V_{ds}}\left(1 - 4B\right)\right] \end{aligned} \tag{6.72}$$

The corresponding capacitances in the *saturation* region are obtained, either by differentiating the corresponding charges derived for saturation region (Equation 6.61) or by replacing V_{ds} with $V_{dsat} = (V_{gs} - V_{th})/\alpha$, in Equation 6.72. Thus, in the saturation we can show

$$\begin{aligned} C_{GD} &= 0 \\ C_{DG} &= -\frac{4}{15} WLC_{ox} \end{aligned} \tag{6.73}$$

Equations 6.72 and 6.73 clearly show the nonreciprocal nature of MOSFET terminal capacitances. It should be pointed out that C_{GD} is most important among the gate capacitances because its effect is multiplied by the voltage gain between the drain and gate nodes due to the Miller effect.

The expressions for C_{GS} and C_{SG} are obtained by differentiating Q_G (Equation 6.57) with respect to V_s and Q_S (Equation 6.54) with respect to V_g (or V_{gs}), respectively, and using A and B defined in Equation 6.55, that is,

$$\begin{aligned} C_{GS} &= -\frac{\partial Q_G}{\partial V_s} \\ &= WLC_{ox}\left[-\frac{1}{2} - A\left(\frac{\partial \alpha}{\partial V_{bs}}\frac{1}{\alpha^2} + \frac{2}{\alpha V_{ds}}\right) - \frac{A}{\alpha\left[V_{gs} - V_{th} - (1/2)\alpha V_{ds}\right]}\right. \\ &\quad \left.\left(-1 + \frac{\partial V_{th}}{\partial V_{bs}} + \frac{\alpha}{2} + \frac{1}{2}\frac{\partial \alpha}{\partial V_{bs}} V_{ds}\right)\right] \end{aligned} \tag{6.74}$$

$$C_{SG} = -\frac{\partial Q_S}{\partial V_g} = \frac{1}{2} WLC_{ox}\left[1 - \frac{A}{V_{gs} - V_{th} - (1/2)\alpha V_{ds}}(3 - 4B)\right] \tag{6.75}$$

The corresponding capacitances in the saturation region can be shown as

$$C_{GS} = WLC_{ox}\left[-1 - \frac{1}{3\alpha}\left(-1 + \frac{\partial V_{th}}{\partial V_{bs}}\right) - \frac{V_{gs} - V_{th}}{3\alpha^2}\frac{\partial \alpha}{\partial V_{bs}}\right] \tag{6.76}$$

$$C_{SG} = \frac{1}{5} WLC_{ox} \tag{6.77}$$

Again, the nonreciprocal nature of the capacitance is self-evident. The detailed model equations with discussions can be found in the literature [3]. Interested readers are encouraged to read the relevant references.

6.3.3 Short Channel Charge Model

In the derivation of long channel terminal charges and capacitances in the previous section, we have neglected the effects of velocity saturation, channel length modulation, and series resistance, since these effects are important only for short channel devices (Chapter 5). As in the case of drain current modeling, we need to consider these in modeling terminal charges for short channel devices. However, the final charge equations including these short channel effects become more complex.

For the simplicity of modeling capacitances for short channel MOSFETs, the long channel charge model has been used by modifying the body effect coefficient, α [8]. However, for accurate modeling of terminal charges and capacitances in short channel devices, short channel effects including carrier velocity saturation, channel length modulation, and S/D series resistance must be considered. In order to include the short channel effects in modeling charges and hence capacitances for short channel devices, I_{ds} expression (Equation 5.72) for short channel devices in the linear region is used. Repeating Equation 5.72, I_{ds} for short channel devices that includes SCE is given by

$$I_{ds} = WC_{ox}\left(V_{gs} - V_{th} - \alpha V\right) \cdot \frac{\mu_{eff} E_y}{1 + \left(E_y / E_c\right)} \tag{6.78}$$

Replacing E_y by $-dV/dy$ and rearranging, we get

$$dy = \left[\frac{\mu_{\text{eff}} WC_{ox}}{I_{ds}}\left(V_{gs} - V_{th} - \alpha V\right) - \frac{1}{E_c}\right] dV \tag{6.79}$$

where:

$E_c = 2v_{sat}/\mu_{eff}$ (Equation 5.70)

After integrating Equation 6.79, we get

$$y = \left[\frac{\mu_{\text{eff}} WC_{ox}}{I_{ds}}\left(V_{gs} - V_{th} - \frac{1}{2}\alpha V\right) - \frac{1}{E_c}\right] V \tag{6.80}$$

Substituting $y = L$ and $V = V_{ds}$ in Equation 6.80, we get the expression for linear region I_{ds} Equation 5.74. Equations 6.78 through 6.80 account for velocity saturation whereas μ_{eff} accounts for S/D series resistance.

Now, following the procedure used to derive terminal charges and capacitances for long channel MOSFET devices in Sections 6.3.1 and 6.3.2, we get the expressions for the (Q_D) drain and source (Q_S) charges in the linear region of device operation as

$$Q_D = -WLC_{ox}\left[\frac{1}{2}\left(V_{gs}-V_{th}\right)-\frac{1}{3}\alpha V_{ds}+A'B'\right]$$
$$Q_S = -WLC_{ox}\left[\frac{1}{2}\left(V_{gs}-V_{th}\right)-\frac{1}{6}\alpha V_{ds}+A'\left(1-B'\right)\right] \tag{6.81}$$

where

$$A' = A\cdot\left(1+\frac{V_{ds}}{LE_c}\right)$$
$$B' = B\cdot\left(1+\frac{V_{ds}}{LE_c}\right) \tag{6.82}$$

and, A and B are defined in Equation 6.55.

Comparing the expressions for Q_D and Q_S in Equation 6.81 for short channel devices with the corresponding expressions for long channel devices in Equation 6.54, we notice that the two equations have the same form differing only in parameters A' and B'. As can be seen from Equation 6.82, A' and B' include the velocity saturation factor. Thus, in the case for a long channel device, the product LE_c is very large, then $A' = A$, $B = B'$, and Equation 6.81 converges to Equation 6.54 as is expected.

Again, using the procedure for deriving Q_G for long channel devices, we can show for short channel devices

$$Q_G = \frac{\mu_s W^2}{I_{ds}}\int_0^{V_d} Q_g\cdot Q_i dV - \frac{W}{E_c}\int_0^{Vd} Q_g dV \tag{6.83}$$

Substituting for Q_i and Q_g from Equations 6.46 and 6.49, respectively, and carrying out the integration, we get after simplification

$$Q_G = WLC_{ox}\left[V_{gs}-V_{fb}-2\phi_B-\frac{1}{2}V_{ds}+\frac{A'}{\alpha}\right] \tag{6.84}$$

Here again, for long channel devices Equation 6.84 converges to Equation 6.57.

Similarly, we can show the bulk charge expression for short channel devices as

$$Q_B = -WLC_{ox}\left[\gamma\sqrt{2\phi_B+V_{sb}}+(\alpha-1)V_{ds}D'\right] \tag{6.85}$$

where

$$D' = D-\frac{1}{12\left[V_{gs}-V_{th}-(1/2)\alpha V_{ds}\right]}\cdot\frac{\alpha V_{ds}}{LE_c} \tag{6.86}$$

and, D is given by Equation 6.60.

In the case of short channel MOSFETs, the terminal charges and capacitances cannot be calculated just by substituting $V_{ds} = V_{dsat}$. However, for short channel devices, where velocity saturation and channel length modulation (CLM) become important, charge near the saturation consists of two components. One is the charge near the source region where the gradual channel approximation can be applied and the other is the charge near the pinch-off region at the drain-end where carrier velocity saturates. This two-section model creates a discontinuity in the capacitances from the linear to saturation regions, similar to the case of drain current modeling. Therefore, often the charge in the pinch-off is ignored for short channel modeling.

The effect of including velocity saturation in the charge expressions is a reduction in the amount of charge from its long channel value, which intuitively makes sense because carriers are velocity saturated. Although the effect of S/D resistance is not taken into account it is possible to include its effect externally.

In weak inversion, Q_I, and hence Q_S and Q_D, are assumed zero, similar to the long channel case. This means that $Q_G = -Q_B$ in weak inversion. For short channel devices, the bulk charge Q_B is still given by Equation 6.24, however, the long channel body factor γ is replaced by an effective value of γ, to account for the reduction in the bulk charge density due to short channel and narrow width effects as discussed in Chapter 5.

6.3.4 Short Channel Capacitance Model

The expressions for the terminal charges for short channel devices given in Section 6.3.3 are used to calculate the corresponding capacitances using the procedure discussed for the long channel devices. The mathematics is basic, however involved. Thus, we will not derive the final expressions for the capacitances.

It is difficult to accurately measure the capacitances for short channel MOSFETs unlike the long channel devices. This is attributed to very small value of capacitances (~1×10^{-18} F) and the difficulty in separating the small transient currents due to the capacitances associated with the source and drain terminals by the large steady-state current (I_{ds}) in small devices. Thus, most reported data on short channel capacitances are on the gate capacitances C_{GS}, C_{GD}, and C_{GB}.

The measured capacitances include the overlap capacitances, and as such, they do not entirely describe intrinsic capacitances. This is particularly true for short channel devices with lightly doped drain (LDD) regions. However, no such bias-dependent overlap is generally observed in short channel conventional S/D *pn*-junctions. The bias dependence of the overlap capacitance is due to the modulation of the lightly doped regions (*n*-region for nMOSFETs and *p*-region for pMOSFETs).

6.4 Gate Overlap Capacitance Model

The S/D overlap capacitances are parasitic elements that originate due to the encroachment of S/D implant profile under the gate region during IC (integrated circuit) fabrication processes. The postimplant thermal processing steps cause lateral diffusion of dopants under the gate and overlap of the S/D regions in the final device structure. Since in MOSFETs, S/D regions are normally symmetrical, the source overlap distance l_{ov} is same as that of the drain (Figure 6.5). Assuming the parallel plate formulation, the overlap capacitance C_{GSO} and C_{GDO} for the source and drain regions, respectively, can be approximated as

$$C_{GSO} = C_{GDO} = \frac{\varepsilon_0 K_{ox}}{T_{ox}} \cdot W l_{ov} = C_{ox} W l_{ov} \tag{6.87}$$

From Equation 6.87, the source and drain overlap capacitances per unit width C_{gso} and C_{gdo}, respectively, are given by

$$C_{gso} = C_{gdo} = C_{ox} l_{ov} \tag{6.88}$$

A third overlap capacitance that can be significant is due to the overlap between the gate and bulk as shown in Figure 5.7. This is the capacitance C_{GBO} that occurs due to the overhang of the transistor gate required at one end and is a function of the effective polysilicon width that is equivalent to the drawn channel lengths. Thus, if C_{gbo} is the gate to bulk overlap capacitance per unit length, then the total gate-to-bulk overlap capacitance becomes

$$C_{GBO} = C_{gbo} L_g \tag{6.89}$$

where:

L_g is the final physical gate length of MOSFET devices

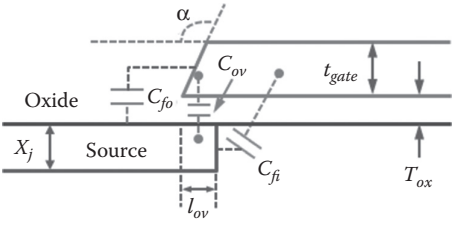

FIGURE 6.5
Different components of MOSFET gate overlap capacitance: C_{ov} due to S/D encroachment length l_{ov} under the gate, C_{fo} outer fringing, and C_{fi} inner fringing.

Typically, C_{GBO} is much smaller than C_{GSO}/C_{GDO} and, therefore, is often neglected.

In a MOSFET, in addition to the outer fringing capacitance, there is another parasitic capacitance that must be taken into account while calculating the overlap capacitance. Thus, MOSFET overlap capacitance can be approximated by the parallel combination of the (1) direct overlap capacitance C_{ov} between the gate and the S/D, (2) outer fringing capacitance C_{fo} on the outer side between the gate and S/D, and (3) inner fringing capacitance C_{fi} on the channel side (inner side) between the gate and side wall of the S/D junction such that [20]

$$\begin{aligned} C_{ov} &= \frac{\varepsilon_0 K_{ox}}{T_{ox}}\left(l_{ov}+\Delta\right) \\ C_{fo} &= \frac{\varepsilon_0 K_{ox}}{\alpha}\ln\left(1+\frac{t_{gate}}{T_{ox}}\right) \\ C_{fi} &= \frac{2\varepsilon_0 K_{si}}{\pi}\ln\left(1+\frac{X_j}{T_{ox}}\sin\beta\right) \end{aligned} \tag{6.90}$$

where:

X_j is the S/D junction depth

Therefore, the total overlap capacitance is given by

$$C_{gso}=C_{gdo}=\frac{\varepsilon_0 K_{ox}}{T_{ox}}\left(l_{ov}+\Delta\right)+\frac{\varepsilon_0 K_{ox}}{\alpha}\ln\left(1+\frac{t_{gate}}{T_{ox}}\right)+\frac{2\varepsilon_0 K_{si}}{\pi}\ln\left(1+\frac{X_j}{T_{ox}}\sin\beta\right) \tag{6.91}$$

In Equation 6.91, C_{ov} is the parallel plate component of the effective overlap distance (l_{ov} + Δ), where Δ accounts for the fact that polysilicon thickness has a slope of angle α. It is a correction factor of higher order and is given by

$$\Delta=\frac{T_{ox}}{2}\left[\frac{1-\cos\alpha}{\sin\alpha}+\frac{1-\cos\beta}{\sin\beta}\right] \tag{6.92}$$

where

$$\beta=\left(\frac{\pi}{2}.\frac{K_{ox}}{K_{si}}\right)$$

It is observed from Equation 6.90 that the inner fringing component C_{fi} (channel side) is much larger than the outer fringing component C_{fo} because $K_{si} \cong 3K_{ox}$, and in general, $\alpha > \pi/2$. Thus, it is clear from Equation 6.91

that if the overlap distance l_{ov} approaches zero, there will be an *overlap* capacitance present in MOSFET devices due to the fringing components C_{fo} and C_{fi}.

Although, the inner fringing capacitance C_{fi} is found to be gate and drain bias dependent, C_{fi} calculated from Equation 6.90 is its maximum value. The value of C_{fi} decreases with the increase in the gate voltage from the sub-threshold to strong inversion and approaches to zero in strong saturation. The overlap capacitance is bias dependent, particularly for advance CMOS (complementary metal-oxide-semiconductor) technology and thin gate oxide devices.

In advanced capacitance models [21,22], the bias dependence of overlap capacitance is considered by analytical expressions. Thus, the source overlap capacitance is given by the source charge overlap as

$$\frac{Q_{overlap,s}}{W_{active}} = \begin{cases} C_{GSO}V_{gs} - \dfrac{1}{2}C_{KAPPA}C_{GSL}\left(-1+\sqrt{1-\dfrac{4V_{gs}}{C_{KAPPA}}}\right), & V_{gs}<0; \\ \left(C_{GSO}+C_{KAPPA}C_{GSL}\right)\cdot V_{gs}, & V_{gs}\geq 0 \end{cases} \tag{6.93}$$

where:

C_{GSL} and C_{KAPPA} are the model parameters that account for the gate-bias dependence of the gate charge due to the source-body overlap region

Similarly, the drain overlap capacitance is given by

$$\frac{Q_{overlap,d}}{W_{active}} = \begin{cases} C_{GDO}V_{gd} - \dfrac{1}{2}C_{KAPPA}C_{GDL}\left(-1+\sqrt{1-\dfrac{4V_{gd}}{C_{KAPPA}}}\right), & V_{gd}<0; \\ \left(C_{GDO}+C_{KAPPA}C_{GDL}\right)\cdot V_{gd}, & V_{gd}\geq 0 \end{cases} \tag{6.94}$$

where:

C_{GDL} is a model parameter that accounts for the gate-bias dependence of the gate charge due to the drain-body overlap region

Then the total charge for the gate overlap over the source and drain regions is given by

$$Q_{overlap,g} = -\left(Q_{overlap,s}+Q_{overlap,d}\right) \tag{6.95}$$

A single equation for the overlap capacitance in both the accumulation and depletion regions is found through the smoothing functions $V_{gs,overlap}$ and $V_{ds,overlap}$ for the source and drain side, respectively.

$$V_{gs,overlap} = \frac{1}{2}\left[\left(V_{gs}+\delta_1\right)-\sqrt{\left(V_{gs}+\delta_1\right)+4\delta_1}\right]$$
$$V_{gd,overlap} = \frac{1}{2}\left[\left(V_{gd}+\delta_2\right)-\sqrt{\left(V_{gd}+\delta_2\right)+4\delta_2}\right] \quad (6.96)$$

where:
$\delta_1 = \delta_2 = 0.02$ V

And, the source overlap capacitance is given by the charge in the gate/source overlap region as

$$\frac{Q_{overlap,s}}{W_{active}} = C_{GSO}V_{gs} - C_{GSL}\left[V_{gs} - V_{gs,overlap} - \frac{1}{2}C_{KAPPA}\left(-1+\sqrt{1-\frac{4V_{gs,overlap}}{C_{KAPPA}}}\right)\right] \quad (6.97)$$

Similarly, the drain overlap capacitance is given from the charge in the gate/drain overlap region

$$\frac{Q_{overlap,d}}{W_{active}} = C_{GDO}V_{gd} - C_{GDL}\left[V_{gd} - V_{gd,overlap} - \frac{1}{2}C_{KAPPA}\left(-1+\sqrt{1-\frac{4V_{gd,overlap}}{C_{KAPPA}}}\right)\right] \quad (6.98)$$

Finally, the total charge for the gate overlap over the source and drain regions is given by

$$Q_{overlap,g} = -\left(Q_{overlap,s} + Q_{overlap,d}\right) \quad (6.99)$$

6.5 Limitations of the Quasistatic Model

The analytical expressions derived in Sections 6.2 and 6.3 for modeling the terminal charges and capacitances of a MOSFET device are based on the quasistatic assumption; that is, the terminal voltages vary sufficiently slowly so that the stored charges (Q_G, Q_S, Q_D, and Q_B) can follow the variation in terminal voltages. It has been found that for most of the digital circuits the quasistatic model predicts acceptable results if the rise time τ_r of the waveforms of the applied signal and the transit time τ_t associated with the DC operation of the device satisfy the relation [1]

$$\tau_r > N_{qs}\tau_t \tag{6.100}$$

where:

N_{qs} is a factor with a value between 15 and 25, depending on the application

τ_t is defined as the average time taken by an inversion carrier to travel the length of the channel

that is,

$$\tau_t = \frac{|Q_I|}{I_{ds}} \tag{6.101}$$

Now using Q_I from Equation 6.61 and saturation region I_{ds} from Equation 4.100, we get

$$\tau_t = \frac{4}{3}\alpha\frac{L^2}{\mu_s\left(V_{gs}-V_{th}\right)} = \frac{4}{3}\alpha\frac{L^2}{\mu_s V_{dsat}} \tag{6.102}$$

Equation 6.102 shows that the transit time is proportional to L^2. Thus, the transit time decreases with the decrease in L, resulting in higher speed of device operation. If the carriers are velocity saturated, then Equation 6.102 becomes invalid and the expressions for Q_I and I_{ds} discussed in Section 5.3 must be used to derive τ_t. However, a simple estimate for τ_t can be made by assuming that carriers are moving from source to drain with their scattering limited saturation velocity v_{sat} for the entire length of the channel rather than only a part of the channel. Since carriers cannot move faster than v_{sat}, the time required for the drain current to respond to the changes in the gate voltage is simply v_{sat}/L. Thus, in general

$$\tau_t > \frac{L}{v_{sat}} \tag{6.103}$$

For long channel devices it can be shown from Equation 6.103 that the switching is limited by the parasitic capacitances rather than the time required for the charge redistribution within the transistor itself. Thus, quasistatic operation is valid for modeling intrinsic capacitances of the most long channel MOSFET devices.

It should be pointed out that Equation 6.100 is only a rough rule of thumb and often, due to the significant extrinsic parasitic capacitances, this rule is not restrictive. For modeling nanoscale devices the time dependence in the basic charge equations must be considered. The resulting analysis is called non-quasistatic analysis.

6.6 S/D *pn*-Junction Capacitance Model

Source-drain *pn*-junction capacitances consist of three components: the bottom junction capacitance, sidewall junction capacitance along the isolation edge, and sidewall junction capacitance along the gate edge. An analogous set of equations are used for both sides but each side has a separate set of model parameters.

In Chapter 2, we have shown that the expression for junction diode capacitance is given by

$$C_j = \frac{C_{j0}}{\left[1-\left(V_d/\phi_{bi}\right)\right]^{mj}} \tag{6.104}$$

For IC *pn*-junctions, the value *mj* is in the range of $0.2 < mj < 0.6$. Plots of Equation 6.104 show that the capacitance C_j decreases as the reverse-biased $|V_d|$ increases ($V_d < 0$) as shown in Figure 2.28. However, Equation 6.104 shows that when the *pn*-junction is forward biased ($V_d > 0$), the capacitance C_j increases and becomes infinite at $V_d = \phi_{bi}$ as observed in Figure 2.28 (curve 1). This is because Equation 6.104 no longer applies due to depletion approximation becoming invalid. For simplicity of modeling forward-biased *pn*-junction capacitances, we can make a series expansion of Equation 6.104. Thus, for modeling the forward-biased *pn*-junction, Equation 6.104 is simplified by a series expansion of the denominator and by neglecting the higher order terms we can show

$$\left(1-\frac{V_d}{\phi_{bi}}\right)^{-mj} = 1+mj\frac{V_d}{\phi_{bi}}+\cdots \tag{6.105}$$

Then Equation 6.104 can be written as

$$C_j = \begin{cases} \dfrac{C_{j0}}{\left(1-\dfrac{V_d}{\phi_{bi}}\right)^{mj}}; & V_d < 0 \\ C_{j0}\left(1+mj\dfrac{V_d}{\phi_{bi}}\right); & V_d > 0 \end{cases} \tag{6.106}$$

6.6.1 Source-Body *pn*-Junction Diode

The source-side *pn*-junction capacitance can be calculated by

$$C_{bs} = A_{seff}C_{jbs} + P_{seff}C_{jbssw} + W_{effcj}NF \cdot C_{jbsswg} \tag{6.107}$$

where:

C_{jbs} is the unit-area bottom source-body junction capacitance
C_{jbssw} is the unit-length source-body junction sidewall capacitance along the isolation edge
C_{jbsswg} is the unit-length source-body junction sidewall capacitance along the gate edge
A_{seff} and P_{seff}, are the effective junction area and perimeter, on the source-side of the S/D diffusion, respectively
W_{effcj} and NF are the effective width of the S/D diffusions and the number of fingers, respectively

The components of the S/D *pn*-junction capacitances are obtained using the following expressions:

- C_{jbs} is calculated by

$$C_{jbs} = \begin{cases} CJS(T)\cdot\left(1-\dfrac{V_{bs}}{PBS(T)}\right)^{-MJS}, & V_{bs} < 0 \\ CJS(T)\cdot\left(1+MJS\dfrac{V_{bs}}{PBS(T)}\right), & V_{bs} \geq 0 \end{cases} \tag{6.108}$$

- C_{jbssw} is calculated by

$$C_{jbssw} = \begin{cases} CJSWS(T)\cdot\left(1-\dfrac{V_{bs}}{PBSWS(T)}\right)^{-MJSWS}, & V_{bs} < 0 \\ CJSWS(T)\cdot\left(1+MJSWS\dfrac{V_{bs}}{PBSWS(T)}\right), & V_{bs} \geq 0 \end{cases} \tag{6.109}$$

- C_{jbsswg} is calculated by

$$C_{jbsswg} = \begin{cases} CJSWGS(T).\left(1-\dfrac{V_{bs}}{PBSWGS(T)}\right)^{-MJSWGS}, & V_{bs} < 0 \\ CJSWGS(T).\left(1+MJSWGS\dfrac{V_{bs}}{PBSWGS(T)}\right), & V_{bs} \geq 0 \end{cases} \tag{6.110}$$

6.6.2 Drain-Body Junction Diode

The drain-side *pn*-junction capacitance can be calculated by

$$C_{bd} = A_{deff}C_{jbd} + P_{deff}C_{jbdsw} + W_{effcj}NF\cdot C_{jbdswg} \tag{6.111}$$

where:

C_{jbd} is the unit-area bottom drain-body junction capacitance
C_{jbdsw} is the unit-length drain-body junction sidewall capacitance along the isolation edge
C_{jbdswg} is the unit-length drain-body junction sidewall capacitance along the gate edge
A_{deff} and P_{deff} are the effective junction area and perimeter on the drain-side of the source-drain diffusion, respectively

- C_{jbd} is calculated by

$$C_{jbd} = \begin{cases} CJD(T)\cdot\left(1-\dfrac{V_{bs}}{PBD(T)}\right)^{-MJD}, & V_{bd}<0; \\ CJD(T)\cdot\left(1+MJD\dfrac{V_{bs}}{PBD(T)}\right), & V_{bd}\geq 0 \end{cases} \tag{6.112}$$

- C_{jbdsw} is calculated by

$$C_{jbdsw} = \begin{cases} CJSWD(T)\cdot\left(1-\dfrac{V_{bs}}{PBSWD(T)}\right)^{-MJSWD}, & V_{bd}<0; \\ CJSWD(T)\cdot\left(1+MJSWD\dfrac{V_{bs}}{PBSWD(T)}\right), & V_{bd}\geq 0 \end{cases} \tag{6.113}$$

- C_{jbdswg} is calculated by

$$C_{jbdswg} = \begin{cases} CJSWGD(T)\cdot\left(1-\dfrac{V_{bs}}{PBSWGD(T)}\right)^{-MJSWGD}, & V_{bd}<0; \\ CJSWGD(T)\cdot\left(1+MJSWGD\dfrac{V_{bs}}{PBSWGD(T)}\right), & V_{bd}\geq 0 \end{cases} \tag{6.114}$$

In the above model equations, the compact model parameters are represented by *upper-case* letters.

6.7 Summary

This chapter presented the dynamic MOSFET models for small signal analysis of MOSFETs in very-large-scale-integrated circuits using quasistatic assumptions. MOSFET device capacitances are separated into intrinsic and

extrinsic or parasitic capacitances. First of all, the widely used simple Meyer intrinsic capacitance model is presented. We have derived the expressions for the terminal charges and capacitances and discussed the merits and demerits of the Meyer model. In order to overcome the limitations of Meyer model, more accurate charge-based capacitance model for both the long and short channel devices are presented. The validity and limitations of quasi-static assumptions in capacitance modeling are also discussed. Finally, the extrinsic capacitances such as the MOSFET S/D overlap capacitance and S/D junction capacitances are presented.

Exercises

6.1 Complete the mathematical steps to show that the linear region capacitances of MOSFETs are given by Equation 6.20.

6.2 Plot the normalized capacitance C/C_{oxt} versus $(V_{gs} - V_{th})$ characteristics for each of the components of gate capacitance C_{GB}, C_{GS}, and C_{GD} for an nMOSFET device with $W = 1$ μm, $L = 250$ nm, and $T_{ox} = 10$ nm; consider the biasing condition $-2.0\ V < V_{gs} < 3.0\ V$ and $V_{ds} = 1$, 2, and 3 V. Clearly state any assumptions you make and explain your plots.

6.3 Show that the channel charge partition for a MOSFET device with channel length L and channel width W at the drain end is given by Equation 6.45.