9

Compact Models for Ultrathin Body FETs

9.1 Introduction

This chapter presents compact models for the emerging ultrathin-body (UTB) field-effect-transistors (FETs). The UTB FETs include *multiple-gate* or *multigate* FinFETs and silicon-on-insulator (SOI) multigate UTB-FETs (UTB-SOI FETs) [1,2]. FinFETs and UTB-SOI FETs have emerged as the real alternatives to MOSFETs (metal-oxide-semiconductor field-effect transistors) and planar CMOS (complementary metal-oxide-semiconductor) technology to surmount the continuous scaling challenges of MOSFET devices. The continuous miniaturization of the conventional planar MOSFET devices has become more challenging at the same rate of Moore's law [3–6] due to several fundamental device-physics constraints such as short channel effects (SCEs). Shrinking the gate length, L, in the decananometer regime degrades the transfer characteristics of planar MOSFETs, degrades the subthreshold swing (S), and decreases V_{th} (e.g., V_{th} roll-off) [3] as discussed in Chapter 5. This implies that the scaled MOSFETs cannot be turned off easily by lowering the gate voltage V_g due to SCEs [7]. Because of SCEs, the device characteristics become increasingly sensitive to L variations and process-induced variability imposes a serious challenge in continued scaling of bulk MOSFETs as discussed in Chapter 8 [8,9]. The early theoretical and modeling approaches on SCEs [10–12] suggest increasing the gate control by reducing the gate dielectric thickness in proportion to L, which increases manufacturing process complexity. Another constraint for the continuous scaling of conventional bulk MOSFETs is controlling leakage current in scaled devices [12]. It is observed that at gate length below 20 nm, the leakage paths several nanometers below the silicon-dielectric interface (subsurface leakage paths) are primarily responsible for the leakage current. These leakage paths are weakly controlled by the gate irrespective of gate oxide thickness and their potential barriers can be easily lowered by drain bias V_d through the enhanced electric field coupling to the drain, referred to as the drain-induced barrier lowering [12]. This new challenge to scaling L led to engineering efforts on channel-profile engineering, shallow source-drain extensions (SDE), and halo implants around SDEs as discussed in Chapter 5 [13–19].

In order to overcome the increasing challenges in continuous scaling of the conventional planar MOSFETs, the major research and development efforts for the last two decades have been exploring alternative device architectures and materials [20–28]. Among the exploratory devices, FinFETs [29–36] and UTB-SOI MOSFETs [37–40] have emerged as the most promising devices for advanced nanometer scale VLSI (very-large-scale-integrated) technology and beyond. The multiple-gates of multigate FETs offer strong electrostatic control over the channel and reduce the coupling between the source and drain in the subthreshold region, thus enabling continuous scaling of FETs. Multigate FETs have a great potential to mitigate the risk of process variability by using undoped channel. The efforts are under way to enable large-scale manufacturing of multigate FETs [41–44]. A reduction of four orders of magnitude in the leakage current over the 32 nm planar manufacturing process has been reported [29]. UTB-SOI FETs [45], deeply depleted channel MOSFETs [46], and BH-halo MOSFETs [47] are close competitors to the FinFET architecture along with IBM's aggressively scaled planar MOSFET down to the 10 nm node [48]. Thus, ultrathin body enables continuous scaling down of FETs by overcoming the major scaling constraints such as SCE and random discrete doping (RDD) of the conventional bulk MOSFETs discussed in Chapters 5 and 8. For computer analysis of the performance of these emerging multigate FETs in VLSI circuits, compact models are critical. This chapter presents surface potential–based compact models for multigate FET devices.

9.2 Multigate Device Structures

The desirables from any alternative device structure include surmounting the impending L scaling barrier, preserving today's CMOS technology as much as possible, and using innovative device architectures to eliminate major problems in scaled planar MOSFETs including undesirable leakage currents and excessive static power. Among the alternative architectures, FinFETs [29–36] and UTB-MOSFETs [37–40] are found to offer solutions to major issues for the continuous scaling of FETs. Both of these structures show potential to eliminate the leakage paths that are far from the gate(s) by limiting the thickness of semiconductor body in the immediate vicinity of the gate(s) [29].

9.2.1 Bulk-Multigate Device Structure

Figure 9.1 shows a 3D cross section of an ideal double-gate MOSFET (DG-MOSFET) device structure [49]. As shown in Figure 9.1, the structure consists of a thin film of undoped silicon body, referred to as the *fin*, a front

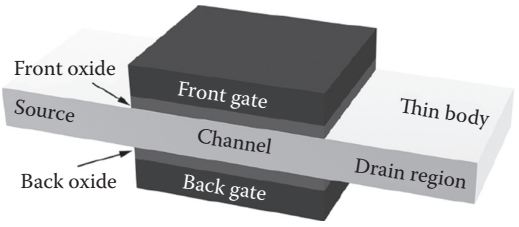

FIGURE 9.1
3D cross section of an ideal DG-MOSFET device structure with an undoped thin film silicon body; all leakage paths are close to the gates due to thin body, thus suppressing the short-channel effects. (Data from N. Paydavosi et al., *IEEE Access*, 1, pp. 201–215, 2013.)

and a back gate oxide layers, a source and a drain regions, and front and back gates. If the body is sufficiently thin, any line drawn between the source and drain including possible leakage paths would not be far from one of the gates. In this structure, channel doping is not required for suppressing SCEs. Thus, RDD, a major contributor to the variation in the performance of IC devices and VLSI circuits, is eliminated [8,9].

Figure 9.2 shows a typical manufacturable version of the multiple-fin FinFET device structure commonly referred to as the *multigate* structure [50]. The fin can be fabricated on SOI or cost-effective bulk silicon substrates using the standard patterning and etching technologies.

Let us consider an ideal symmetric double-gate FinFET (DG-FinFet) structure with channel length L and the channel thickness defined by fin

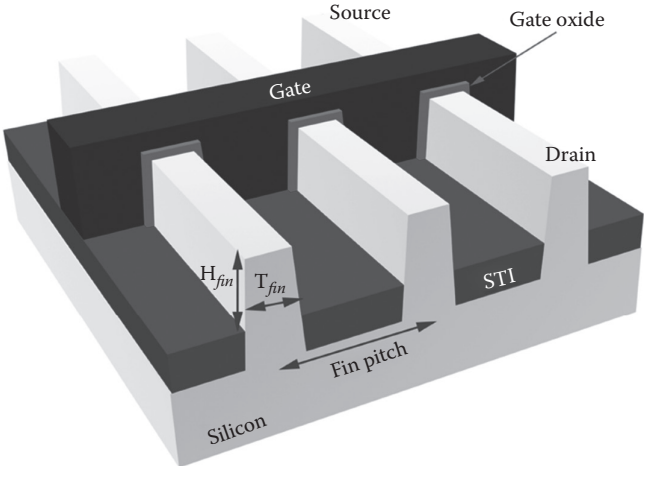

FIGURE 9.2
3D cross section of a typical multifin FinFET structure used in manufacturing; in the structure, W is the channel width, H_{fin} is the fin height, and $T_{fin} \equiv t_{fin}$ is the fin thickness. (Data from N. Paydavosi et al., *IEEE Access*, 1, pp. 201–215, 2013.)

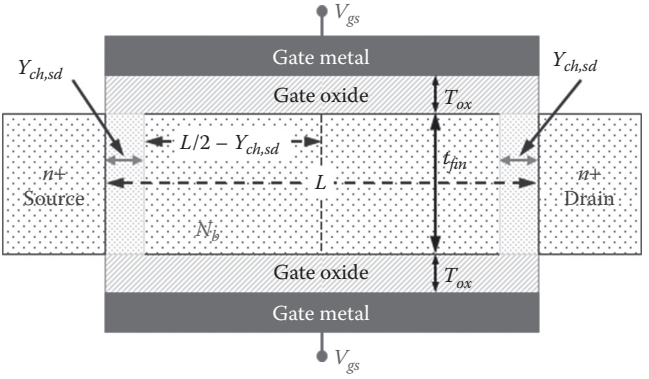

FIGURE 9.3
A typical symmetric DG-nMOSFET device structure: t_{fin}, T_{ox}, and N_b are the fin thickness, gate oxide thickness, and body doping concentration, respectively; $Y_{ch,sd}$ is the depletion width in the y direction along the channel due to the applied drain bias V_{ds}.

thickness t_{fin} as shown in Figure 9.3. In order to ensure a complete gate control of the channel, it is required that t_{fin} is completely depleted by gate bias V_{gs} so that the fin depletion width ($X_{ch,g}$) satisfies the relation

$$X_{ch,g} \geq \frac{t_{fin}}{2} \tag{9.1}$$

and, in order to suppress source-drain punchthrough, the lateral channel depletion ($Y_{ch,d}$) due to V_{ds} at each end of the channel must be such that the neutral channel length ($L/2 - Y_{ch,sd}$) in the y direction along the channel must satisfy

$$X_{ch,g} << \frac{L}{2} - Y_{ch,sd} \tag{9.2}$$

From the above inequalities, we can show that in order to suppress SCE, the device structure must satisfy the conditions given in Equations 9.1 and 9.2. Combining Equations 9.1 and 9.2 and expressing $Y_{ch,d}$ in terms of equivalent gate oxide thickness (Equation 3.82), we get the condition for *scaling* FinFET device structure

$$\frac{t_{fin}}{2} + \frac{K_{si}}{K_{ox}} T_{ox} << \frac{L}{2} \tag{9.3}$$

Typically, $Y_{ch,d}$ is very small. Therefore, the scaling rule for FinFETs can safely be defined by

$$\frac{t_{fin}}{2} << \frac{L}{2} \tag{9.4}$$

Thus, if the fin is sufficiently thin with a thickness, t_{fin}, smaller than L, then SCEs are suppressed and subthreshold slope (S) is expected to be near its ideal value of about 60 mV per decade (at room temperature) [29]. Thus, the new device architecture results in a new *scaling rule* given in Equation 9.3; that is, L can be scaled by maintaining the condition $t_{fin} < L$, relaxing the scaling of gate dielectric and body doping.

In 1988 and 1999, 45 and 18 nm working DG-FinFETs, respectively, were reported [30,31]. Subsequently, 10 nm double-gate [32], 10 nm triple-gate (Q gate) [33], 5 nm nanowire [34], and 3 nm all-around gate [35] FinFETs were reported.

9.2.2 UTB-SOI Device Structure

Figure 9.4 shows 3D cross section of an ideal UTB-SOI transistor structure. If t_{fin} in an SOI-MOSFET is only several nanometers (e.g., thinner than about one-half of L), the leakage paths far from the gate will be eliminated and SCEs can be significantly suppressed. It is found that the transistor leakage current is reduced by about ten times for every nanometer drop in t_{fin} [37]. The UTB-SOI MOSFETs require SOI substrates with extremely uniform silicon films (sub-nanometer uniformity). In 2009, SOI wafer supplier, Soitec, developed SOI wafers with a desired tolerance of ±0.5 nm using a process called *smart cut* [51]. It is reported that UTB-SOI MOSFETs with $t_{fin} \approx 3$ nm have been experimentally realized [52]. The most attractive channel materials for UTB-SOI MOSFETs are the *monolayer* semiconductors such as graphene [22], MoS_2 [23], and WSe_2 monolayer [53].

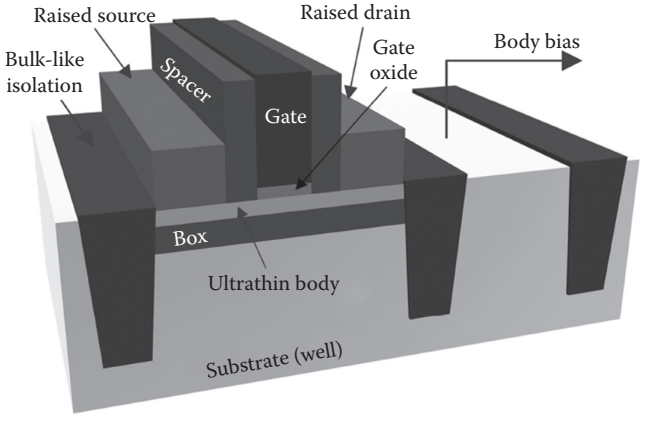

FIGURE 9.4
3D cross section of an ultrathin body SOI MOSFET device structure: the body can be a thin film of silicon, or any monolayer semiconductors; appropriate thickness of the buried oxide, BOx can be used as the back gate oxide to bias the body for the target dynamic V_{th} shift. (Data from N. Paydavosi et al., *IEEE Access*, 1, pp. 201–215, 2013.)

In a UTB transistor, the thickness of the buried oxide (BOx) layer is reduced to use the substrate immediately below the BOx as a back gate to bias the body of the device and to enable a multi-V_{th} technology, especially for system-on-chip design [54–56].

The multiple-gate FET structures can be classified as (1) common multigate (CMG) structure where a common gate terminal is used to bias the device and the gate dielectric thicknesses is the same and (2) independent multigate (IMG) structure where gates are independently biased and the gate dielectric thickness is different for each gate.

9.3 Common Multiple-Gate FinFET Model

The term common gate defines all gates in the multigate (double-gate or triple-gate or quadruple-gate) FinFET, which are electrically interconnected and are biased at the same electrical terminal voltage. It is also assumed that the gate work functions and the dielectric thicknesses on all sides to the silicon fin are the same. However, the carrier mobilities in the inversion are dependent on crystal orientations and/or strain.

9.3.1 Core Model: Poisson-Carrier Transport

The core CMG model is formulated using gradual channel approximation (GCA) [57], described in Chapter 4, and assuming physical effects such as mobility degradation can safely be neglected. Several basic models have been proposed for the FinFET, where charge [58] and surface potential [59,60] modeling approaches have been mainly used for model formulations. The core model described in the following section is based on the solution of Poisson's drift/diffusion equations for a long channel DG-FinFET assuming a finite doping in the channel [29]. The reported simulation data obtained by the core model agree very well with the numerical device simulation data [60,61].

9.3.1.1 Electrostatics

For the simplicity of model formulation, let us consider 2D (two-dimensional) cross section of an ideal *n*-type FinFET device structure as a common double-gate transistor as shown in Figure 9.5. First of all, we obtain surface potential ϕ_s within the device by solving 1D Poisson's equation given by (Equation 3.30)

$$\frac{d^2\phi(x,y)}{dx^2} = -\frac{q}{K_{si}\varepsilon_0}\left[p(x,y) - n(x,y) + N_d^+(x,y) - N_a^-(x,y)\right] \tag{9.5}$$

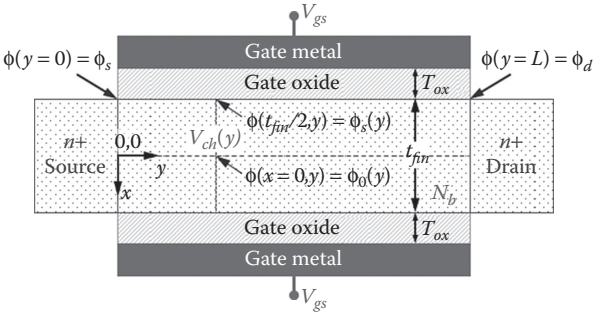

FIGURE 9.5
Schematic of an idealized symmetric common DG-nMOSFET device used to derive device equations: T_{ox}, t_{fin}, and N_b are the gate oxide thickness, fin or body thickness, and body doping concentration, respectively; the origin of the coordinate system (0,0) is at the center at ($L = 0$, $t_{fin}/2$); ϕ_s and ϕ_d are the surface potentials at the source and drain ends of the device, respectively.

where:

$\phi(x, y)$ is the electrostatic potential at any point (x, y) in the channel
q is the magnitude of the electronic charge
K_{si} and ε_0 are the dielectric constant of the silicon channel (fin) and permittivity of free space, respectively
$p(x, y)$, $n(x, y)$, $N_d^+(x, y)$, and $N_a^-(x, y)$ are the hole, electron, ionized donor, and ionized acceptor concentrations at any point (x, y) of the semiconductor substrate, respectively

For a *p*-type substrate, the minority carrier concentration at any point (x, y) of the substrate is given by (Equation 3.40)

$$n(x,y) \cong \frac{n_i^2}{p(x)} = \frac{n_i^2}{N_a} \exp\left[\frac{\phi(x,y)}{v_{kT}}\right] \tag{9.6}$$

where:

N_a is the acceptor doping concentration in a *p*-type substrate (assuming complete ionization)
n_i is the intrinsic carrier concentration
v_{kT} is the thermal voltage given by kT/q
k and T are the Boltzmann constant and ambient temperature, respectively

Again, from Equation 3.35, we can show that for a *p*-type substrate

$$\phi_B = v_{kT} \ln\left(\frac{N_a}{n_i}\right) \tag{9.7}$$

and

$$\frac{n_i^2}{N_a} = n_i \exp\left(-\frac{\phi_B}{v_{kT}}\right) \tag{9.8}$$

where:
ϕ_B is the bulk potential

Typically, FinFETs are undoped or lightly doped channel devices; therefore, we consider only the inversion carrier electron concentration $n(x, y)$ at any point (x, y) given by Equation 9.6 and uniformly doped p-type body doping concentration, $N_a(x, y) \equiv N_b$. Let us assume that $V_{ch}(y)$ is the channel potential at any point y and GCA as described in Chapter 4 is valid [57]. Then for a double-gate FET (DG-FET) shown in Figure 9.5, we can express Poisson's Equation 9.5 as

$$\frac{d^2\phi(x,y)}{dx^2} = \frac{q}{K_{si}\varepsilon_0}\left\{n_i \exp\left[\frac{\phi(x,y) - \phi_B - V_{ch}(y)}{v_{kT}}\right] + N_b\right\} \tag{9.9}$$

where:
$V_{ch}(y)$ is given by $V_{ch}(0) = V_s$ at the source and $V_{ch}(L) = V_d$ at the drain

From Equation 9.9, the electrostatic potential $\phi(x, y)$ at any point (x, y) in the channel can be written as

$$\phi(x,y) \cong \phi_1(x,y) + \phi_2(x,y) \tag{9.10}$$

In Equation 9.10, $\phi_1(x, y)$ is the contribution to $\phi(x, y)$ due to the inversion carriers without the effect of the ionized body dopants, and $\phi_2(x, y)$ is the contribution to $\phi(x, y)$ due to body dopants, N_b. Therefore, we have

$$\frac{d^2\phi_1(x,y)}{\partial x^2} = \frac{qn_i}{K_{si}\varepsilon_0}\exp\left[\frac{\phi(x,y) - \phi_B - V_{ch}(y)}{v_{kT}}\right] \tag{9.11}$$

$$\frac{d^2\phi_2(x,y)}{\partial x^2} = \frac{qN_b}{K_{si}\varepsilon_0} \tag{9.12}$$

If t_{fin} is less than the width of the depletion region, then for a certain gate bias V_g, the silicon fin is fully depleted and consequently the inversion carriers are spread throughout the entire body. Thus, $Q_i >> Q_b$, and therefore, we can safely neglect the term containing N_b in Equation 9.9 and the channel potential is obtained by solving Equation 9.11.

We know that for a symmetric double-gate structure, the vertical component of the electric field E_x is zero at the center, that is, at $x = 0$, $d\phi_1/dx = 0$

and $\phi_1(x=0, y) = \phi_0(y)$; then using Equation 3.47 and following the procedure described in Section 3.4.2, we get $\phi_1(x, y)$ by integrating Equation 9.11 twice as

$$\phi_1(x,y) = \phi_0(y) - 2v_{kT} \ln\left(\cos\left\{ \sqrt{\frac{q}{2K_{si}\varepsilon_0 v_{kT}} \frac{n_i^2}{N_b} \exp\left[\frac{\phi_0(y) - V_{ch}(y)}{v_{kT}} \right]} \cdot \frac{x}{2} \right\} \right) \tag{9.13}$$

where:

$\phi_0(y)$ is the potential at the center of the body as shown in Figure 9.5 and we have used Equation 9.8 to express ϕ_B in terms of n_i and N_b

Similarly, in order to solve for $\phi_2(x, y)$, we apply the boundary conditions: $E_x = 0$ at the center of the channel ($x = 0$) and $\phi_2(x = 0, y) = 0$, and integrate Equation 9.12 twice. Again, using Equation 3.47, we can express Equation 9.12 as

$$\frac{d}{dx}\left(\frac{\partial \phi_2(x,y)}{\partial x} \right)^2 = 2\frac{qN_b}{K_{si}\varepsilon_0} \frac{d\phi_2(x,y)}{dx} \tag{9.14}$$

Now, integrating Equation 9.14 from $d\phi_2(x = 0, y)/\mathrm{d}x = 0$, $\phi_2(x = 0, y) = 0$ to any point $d\phi_2(x, y)/\mathrm{d}x$, $\phi_2(x, y)$ we get

$$\int_0^{d\phi_2/dx} d\left(\frac{\partial \phi_2(x,y)}{\partial x} \right)^2 = 2\frac{qN_b}{K_{si}\varepsilon_0} \int_0^{\phi_2(x,y)} d\phi_2(x,y) \tag{9.15}$$

After integration and simplification, we get from Equation 9.15

$$\frac{d\phi_2(x,y)}{\sqrt{\phi_2(x,y)}} = \sqrt{\frac{2qN_b}{K_{si}\varepsilon_0}} \cdot dx \tag{9.16}$$

Integrating Equation 9.16, from $x = 0$, $\phi_2(x = 0, y) = 0$ to any point x, $\phi_2(x, y)$, we can show

$$\phi_2(x,y) = \frac{qN_b x^2}{2K_{si}\varepsilon_0} \tag{9.17}$$

The surface potential $\phi_s(y)$ at any point y along the surface is obtained by evaluating the sum of $\phi_1(x,y)$ and $\phi_2(x,y)$ at the surface ($x = -t_{fin}/2$) such that

$$\phi_s(y) \cong \phi_1\left(-\frac{t_{fin}}{2}, y \right) + \phi_2\left(-\frac{t_{fin}}{2}, y \right) \tag{9.18}$$

In Equation 3.23 we have shown that

$$V_{gs} = V_{fb} + \phi_s - \frac{Q_s}{C_{ox}} \tag{9.19}$$

where:
V_{gs} is the gate voltage
V_{fb} is the flat-band voltage
Q_s is the total charge in the body
C_{ox} is the gate oxide capacitance per unit area, given by $K_{ox}\varepsilon_0/T_{ox}$, with K_{ox} and T_{ox} are the permittivity of oxide and oxide thickness, respectively

Then from Gauss's law at the channel/oxide interface, we get

$$Q_s = -K_{si}\varepsilon_0 E_{xs} \tag{9.20}$$

where:
E_{xs} is the vertical component of the electric field at the surface

Substituting Equation 9.20 in Equation 9.19, we get

$$V_{gs} = V_{fb} + \phi_s(y) + \frac{K_{si}\varepsilon_0 E_{xs}}{C_{ox}} \tag{9.21}$$

Now, following the procedure to obtain E_{xs} for bulk MOS (metal-oxide-semiconductor) capacitor system in Equation 3.51, we can show for a DG-FET device

$$\frac{d}{dx}\left(\frac{d\phi}{dx}\right)^2 = \frac{2q}{K_{si}\varepsilon_0}\left\{n_i \exp\left[\frac{\phi(x,y)-\phi_B-V_{ch}(y)}{v_{kT}}\right]+N_b\right\}\frac{d\phi}{dx} \tag{9.22}$$

We integrate Equation 9.22 from center potential $\phi(x=0,y)\equiv\phi_0(y)$, $d\phi(x=0,y)/dx=0$ to any point $\phi(x, y)$ and $d\phi(x, y)/dx$ to get

$$\int_0^{d\phi/dx} d\left(\frac{d\phi}{dx}\right)^2 = \frac{2qn_i}{K_{si}\varepsilon_0}\int_{\phi_0(y)}^{\phi(x,y)}\left\{\exp\left[\frac{\phi(x,y)-\phi_B-V_{ch}(y)}{v_{kT}}\right]+\frac{N_b}{n_i}\right\}d\phi \tag{9.23}$$

After integration and simplification, we can express Equation 9.23 as

$$\left[\frac{d\phi(x,y)}{dx}\right]^2 = \frac{2qn_i}{K_{si}\varepsilon_0}\left(\begin{array}{l} v_{kT}\left\{\exp\left[\frac{\phi_s(y)}{v_{kT}}\right]-\exp\left[\frac{\phi_0(y)}{v_{kT}}\right]\right\}\cdot\exp\left[\frac{-\phi_B-V_{ch}(y)}{v_{kT}}\right] \\ +\exp\left(\frac{\phi_B}{v_{kT}}\right)\left[\phi(y)-\phi_0(y)\right] \end{array}\right) \tag{9.24}$$

$$= E_s^2(x) \equiv E_{xs}^2$$

where in Equation 9.24, we have used Equation 9.7 for N_b/n_i. Thus, the vertical electric field at any point y along the surface of the channel is given by

$$E_{xs} = \sqrt{\frac{2qn_i}{K_{si}\varepsilon_0}\left[\begin{array}{l} v_{kT}\left\{\exp\left[\frac{\phi_s(y)}{v_{kT}}\right]-\exp\left[\frac{\phi_0(y)}{v_{kT}}\right]\right\}\cdot\exp\left[\frac{-\phi_B-V_{ch}(y)}{v_{kT}}\right] \\ +\exp\left(\frac{\phi_B}{v_{kT}}\right)\cdot\left[\phi_s(y)-\phi_0(y)\right] \end{array}\right]} \tag{9.25}$$

Combining Equations 9.21 and 9.25, we get

$$V_{gs} = V_{fb} + \phi_s(y) + \frac{K_{si}\varepsilon_0}{C_{ox}}\sqrt{\frac{2qn_i}{K_{si}\varepsilon_0}\left(\begin{array}{l} v_{kT}\left\{\exp\left[\frac{\phi_s(y)}{v_{kT}}\right]-\exp\left[\frac{\phi_0(y)}{v_{kT}}\right]\right\}\cdot\exp\left[\frac{-\phi_B-V_{ch}(y)}{v_{kT}}\right] \\ +\exp\left(\frac{\phi_B}{v_{kT}}\right)\cdot\left[\phi_s(y)-\phi_0(y)\right] \end{array}\right)} \tag{9.26}$$

Equations 9.18 and 9.26 represent a self-consistent system of equations that can be solved to obtain $\phi_0(y)$ and $\phi_s(y)$ for a fully depleted DG-FET structure under a set of external biases.

In the partially depleted DG-FETs, the depletion width X_d is bias dependent. At the edge of depletion region, $\phi_1(x = X_d, y) = 0$. With these changes, the surface potential can be derived for the partially depleted devices similar to the fully depleted devices. It can be shown that for the partially depleted body

$$\phi_1\left(x=\frac{t_{si}}{2}, y\right) = -2v_{kT}.\ln\left(\cos\left\{\sqrt{\frac{q}{2K_{si}\varepsilon_0 v_{kT}}\frac{n_i^2}{N_b}\exp\left[\frac{-V_{ch}(y)}{v_{kT}}\right]}\cdot\frac{X_d}{2}\right\}\right) \tag{9.27}$$

$$V_{gs} = V_{fb} + \phi_s(y) + \frac{K_{si}\varepsilon_0}{C_{ox}}\sqrt{\frac{2qn_i}{K_{si}\varepsilon_0}\left(\begin{array}{l} v_{kT}\left\{\exp\left[\frac{\phi_s(y)}{v_{kT}}\right]-1\right\}.\exp\left[\frac{-\phi_B-V_{ch}(y)}{v_{kT}}\right] \\ +\exp\left(\frac{\phi_B}{v_{kT}}\right)\cdot\phi_s(y) \end{array}\right)} \tag{9.28}$$

In order to obtain continuous expressions for terminal currents and charges, it is necessary to capture the transition between the fully depleted and partially depleted regimes in a smooth manner. Also, the solution of Equations 9.27 and 9.28 is computationally intensive due to the complex $\phi_2(x, y)$ term. To overcome these issues, a simplified expression is used for $\phi_2(x,y) = \phi_{pert}$ which is continuous between the partially depleted and fully depleted regimes. Here, ϕ_{pert} is used as a small perturbation term. Thus, using ϕ_{pert}, a surface potential in both the regimes is calculated through a single continuous equation. The transformation variable β is the argument of the cosine function in $\phi_1(t_{fin}/2, y)$ in Equation 9.13

$$\beta \equiv \frac{t_{fin}}{2}\sqrt{\frac{q}{2K_{si}\varepsilon_0 v_{kT}}\frac{n_i^2}{N_b}\exp\left[\frac{\phi_0(y)-V_{ch}(y)}{v_{kT}}\right]} \tag{9.29}$$

and, from Equation 9.17, $\phi_{pert} \equiv \phi_2(t_{fin}/2, y)$ is given by

$$\phi_{pert} \equiv \phi_2\left(\frac{t_{fin}}{2}, y\right) = \frac{qN_b}{2K_{si}\varepsilon_0}\frac{t_{fin}^2}{4} \tag{9.30}$$

Thus, through a change of variable, the unified surface potential ϕ_s equation can be written as

$$\begin{aligned} f(\beta) \equiv \ln(\beta) - \ln(\cos\beta) - \frac{V_{gs}-V_{fb}-V_{ch}}{2v_{kT}} + \ln\left(\frac{2}{t_{fin}}\sqrt{\frac{2K_{si}\varepsilon_0 v_{kT}N_b}{qn_i^2}}\right) \\ + \frac{2K_{si}\varepsilon_0}{t_{fin}C_{ox}}\cdot\sqrt{\beta^2\left[\frac{\exp\left(\phi_{pert}/v_{kT}\right)}{\cos^2\beta}-1\right]+\frac{\phi_{pert}}{v_{kT}^2}\left[\phi_{pert}-2v_{kT}\ln(\cos\beta)\right]} = 0 \end{aligned} \tag{9.31}$$

Equation 9.31 (implicit in β) is the basic surface potential equation (SPE) in Berkeley Short Channel IGFET Model (BSIM) CMG [50]. It is solved by first using an analytical approximation for the initial guess [61], followed by two Householder's cubic iterations (third-order Newton-Raphson iterations); together these make the model numerically robust and accurate. The surface potentials at the source end ϕ_{s0} and drain end ϕ_{sL} are calculated by setting $V_{ch}(y = 0) = V_s$ and $V_{ch}(y = L) = V_d$, respectively. For a lightly doped body, Equation 9.31 can be further simplified [62] to speed up the simulation.

From Equation 9.30: if $\phi_{pert} \approx 0$, then in Equation 9.31 we have $\exp\left(\phi_{pert}/v_{kT}\right) = 1$ and $\left(\phi_{pert}/v_{kT}^2\right)\left[\phi_{pert} - 2v_{kT}\ln(\cos\beta)\right] \approx 0$. Then

$$\left[\frac{\exp\left(\phi_{pert}/v_{kT}\right)}{\cos^2\beta}-1\right] = \frac{1}{\cos^2\beta}-1 = \tan^2\beta$$

Therefore, we can simplify Equation 9.31 as

$$\begin{aligned} \ln(\beta) - \ln(\cos\beta) - \frac{V_{gs}-V_{fb}-V_{ch}}{2v_{kT}} + \ln\left(\frac{2}{t_{fin}}\sqrt{\frac{2K_{si}\varepsilon_0 v_{kT}N_b}{qn_i^2}}\right) \\ + \frac{2K_{si}\varepsilon_0}{t_{fin}C_{ox}}\beta\tan\beta = 0 \end{aligned} \tag{9.32}$$

A separate surface potential expression is used for the cylindrical gate geometry [63].

9.3.1.2 Drain Current Model

The drain-to-source current I_{ds} for the long channel DG-FinFETs is obtained from the solution of drift-diffusion equation (Equation 4.63)

$$I_{ds}(y) = \mu(T) W Q_i(y) \frac{dV_{ch}}{dy} \tag{9.33}$$

where:
- $\mu(T)$ is the low-field and temperature-dependent mobility
- W is the total effective width
- Q_i is the inversion charge per unit area in the upper half part of the body

Equation 9.33 includes drift and diffusion transport mechanisms through the use of the quasi-Fermi potential. Integrating both sides of Equation 9.33, and considering the fact that under quasistatic operation I_{ds} is constant along the channel, we can express Equation 9.33 in its integral form:

$$I_{ds} = \left(\frac{W}{L}\right)\mu(T)\int_{Q_{is}}^{Q_{id}} Q_i \frac{dV_{ch}}{dQ_i} dQ_i \tag{9.34}$$

where:
- L is the effective channel length
- Q_{is} and Q_{id} are the inversion charge densities at the source and drain ends, respectively

From the relation $Q_S = (Q_i + Q_b)$, we get

$$\begin{aligned} Q_{is} &= C_{ox}\left(V_{gs} - V_{th} - \phi_{s0}\right) - Q_b \\ Q_{id} &= C_{ox}\left(V_{gs} - V_{th} - \phi_{sL}\right) - Q_b \end{aligned} \tag{9.35}$$

From Gauss's Law, we get the total charge in the fin, $Q_S = -K_{si}\varepsilon_0 E_{xs}$; then we can show from Equation 9.25

$$Q_s(y) = \sqrt{2qn_i K_{si}\varepsilon_0 \left[\begin{array}{l} v_{kT}\left(e^{\left[\phi_s(y)/v_{kT}\right]} - e^{\left[\phi_0(y)/v_{kT}\right]}\right).e^{\left\{\left[-\phi_B - V_{ch}(y)\right]/v_{kT}\right\}} \\ + e^{\left[\phi_B/v_{kT}\right]}.\left[\phi_s(y) - \phi_0(y)\right] \end{array}\right]} \tag{9.36}$$

Note that the second term in the square bracket is due to bulk charge. For lightly doped body, $Q_b << Q_i$; therefore, neglecting the bulk charge term in Equation 9.36, we can express inversion charge as

$$Q_i(y) \approx \sqrt{2qn_i K_{si}\varepsilon_0 \left[v_{kT}\left(e^{\left[\phi_s(y)/v_{kT}\right]} - e^{\left[\phi_0(y)/v_{kT}\right]}\right).e^{\left\{\left[-\phi_B - V_{ch}(y)\right]/v_{kT}\right\}}\right]} \tag{9.37}$$

Equation 9.37 can be further simplified as

$$Q_i(y) = \sqrt{2qn_iK_{si}\varepsilon_0 v_{kT}}\, e^{\left[\phi_s(y)-\phi_B-V_{ch}(y)/2v_{kT}\right]}\sqrt{1-e^{\left[\phi_0(y)-\phi_s(y)/v_{kT}\right]}} \tag{9.38}$$

In strong inversion $\phi_s(y) >> \phi_0(y)$; therefore, $\sqrt{1-e^{\left[\phi_0(y)-\phi_s(y)/v_{kT}\right]}}$ approaches 1. In weak inversion, we can simplify this term assuming liner profile from $x = 0$ to $x = -t_{fin}/2$. If E_{avg} is the average electric field in the region between $x = -t_{fin}/2$ to the mid-potential at $x = 0$, then using Gauss's law, we can write

$$E_{avg} = -\frac{d\phi(y)}{dx} = \frac{Q_i}{K_{si}\varepsilon_0} \tag{9.39}$$

If we assume that surface potential varies linearly from center potential $\phi_0(y)$ to the surface potential $\phi_s(y)$, then Equation 9.39 can be expressed as

$$-\frac{d\phi(y)}{dx} = \frac{\phi_s(y)-\phi_0(y)}{t_{fin}/2} = \frac{Q_i}{K_{si}\varepsilon_0} \tag{9.40}$$

Thus, the inversion charge is given by

$$\phi_s(y)-\phi_0(y) = \frac{Q_i}{\left(2K_{si}\varepsilon_0\right)/t_{fin}} = \frac{Q_i}{2C_{si}} \tag{9.41}$$

where $C_{si} = K_{si}\varepsilon_0/t_{fin}$; substituting Equation 9.41 in Equation 9.38 and performing Taylor's series expansion, the inversion charge for lightly doped DG-FETs is given by

$$Q_{i,LD}(y) \approx \sqrt{2qn_iK_{si}\varepsilon_0 v_{kT}}\,.\exp\left[\frac{\phi_s(y)-\phi_B-V_{ch}(y)}{2v_{kT}}\right].\sqrt{\frac{Q_i(y)}{Q_i(y)+2C_{si}v_{kT}}} \tag{9.42}$$

Equation 9.42 is an implicit equation in Q_i and is solved iteratively to obtain drain current from Equation 9.33. Using $Q_s \approx Q_{i,LD}$ in Equation 9.19, we can compute V_{gs} versus inversion charge $Q_{i,LD} = -C_{ox}\left(V_{gs}-V_{fb}-\phi_s\right)$.

Similarly, the inversion charge density for heavily doped DG-FETs can be shown as

$$Q_{i,HD}(y) \approx \sqrt{2qn_iK_{si}\varepsilon_0 v_{kT}}\,.\exp\left[\frac{\phi_s(y)-\phi_B-V_{ch}(y)}{2v_{kT}}\right].\sqrt{\frac{Q_i(y)}{Q_i(y)+2Q_b}} \tag{9.43}$$

From the similarities of charge expressions in Equations 9.42 and 9.43, a unified expression is used to calculate the inversion charge density for a wide range of devices as a function of Q_b and is given by

$$Q_i(y) = \sqrt{2qn_iK_{si}\varepsilon_0 v_{kT}}\,.\exp\left[\frac{\phi_s(y)-\phi_B-V_{ch}(y)}{2v_{kT}}\right]\sqrt{\frac{Q_i(y)}{Q_i(y)+Q_0}} \tag{9.44}$$

where:
$Q_0 = 2Q_b + 5C_{si}v_{kT}$, with $C_{si} = K_{si}\varepsilon_0/t_{fin}$
Q_b is the fixed depletion charge and is given by qN_bt_{fin}

It is reported that the unified charge density model agrees very well with the inversion charge density calculated using an exact equation for a wide range of body doping concentration [60]. Then from Equation 9.44, the gradient in $V_{ch}(y)$, term dV_{ch}/dQ_i can be calculated as a function of Q_i using a simple but accurate implicit equation for Q_i [60]

$$\frac{dV_{ch}}{dy} = \frac{d\phi_s}{dy} + v_{kT}\frac{dQ_i}{dy}\left(\frac{2Q_b + 5C_{si}v_{kT}}{Q_i + 2Q_b + 5C_{si}v_{kT}} - \frac{2}{Q_i}\right) \tag{9.45}$$

Equation 9.34 can be integrated analytically using Equation 9.44 to calculate dV_{ch}/dQ_i to obtain the following basic equation for I_{ds}

$$I_{ds} = \left(\frac{W}{L}\right)\mu(T)\cdot\left[\frac{Q_{is}^2 - Q_{id}^2}{2C_{ox}} + 2v_{kT}\left(Q_{is} - Q_{id}\right) - v_{kT}Q_0\ln\left(\frac{Q_0 + Q_{is}}{Q_0 + Q_{id}}\right)\right] \tag{9.46}$$

Equation 9.46 describes the drain current model for symmetric DG-FETs. The model equation predicts the drain current in all operation regions: subthreshold, linear, and saturation of both fully depleted and lightly depleted channel symmetric DG-FETs. Figure 9.6 shows the simulated *I–V* characteristics of a bulk FinFET device obtained by multigate drain current model with the measured data.

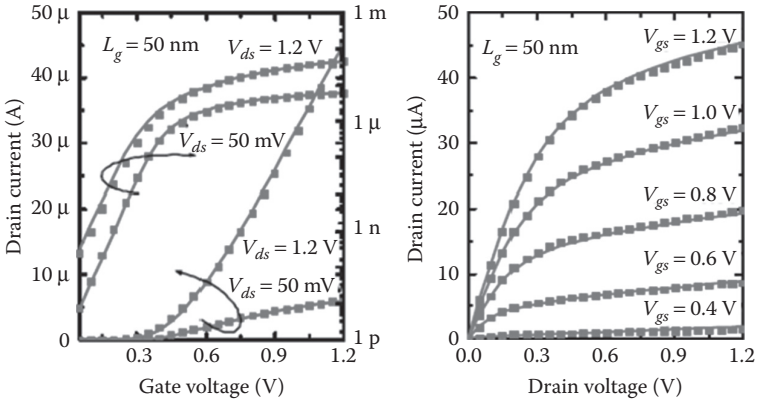

FIGURE 9.6
Drain current model used to compare the measured and simulated *I–V* characteristics of moderately doped symmetric bulk *n*-channel FinFET devices: (a) $I_{ds} - V_{gs}$ characteristics for different V_{ds}; (b) $I_{ds} - V_{ds}$ characteristics for different V_{gs}. Device data are $L = 50$ nm, $t_{fin} = 25$ nm, and TiN gate with equivalent $T_{ox} = 1.95$ nm; symbols are measured data and lines represent compact drain current model. (Data from M.V. Dunga et al., *IEEE Symposium on VLSI Technology*, pp. 60–61, 2007.)

A unique behavior of lightly doped DG-FETs with thin body is that the inversion charge is no longer confined to interface and the entire film is inverted. For any gate voltage, the electrostatic potential increases at the interfaces as well as in the volume of the film in all mode of device operation: the depletion, weak inversion, and the strong inversion. As a result, the potential shift or total band bending exceeds $2\phi_B$ in every region and in the entire film. This is referred to as the *volume inversion* [61, 63–65]. Due to volume inversion (1) the potential as well as the inversion carrier density is nearly independent of the position inside the body because of the negligible potential drop between the surface and the center of the body as shown in Figure 9.7a; (2) the potential as well as the inversion charge density is weakly dependent on the body thickness; any small increase in the gate voltage in the subthreshold region increases the potential throughout the entire body, causing inversion in the entire body; and (3) since the electronic potential is virtually independent of the body thickness, the total integrated charge inside the body is proportional to the body thickness. Thus, as a result of volume inversion, the subthreshold region drain current is also proportional to t_{fin} as shown in Figure 9.7.

9.3.2 Modeling Physical Effects of Real Device

This subsection briefly reviews some of the real-device effects for the modern multigate transistors, highlighting the key physical effects and implementations, and outlining the proper references for further details.

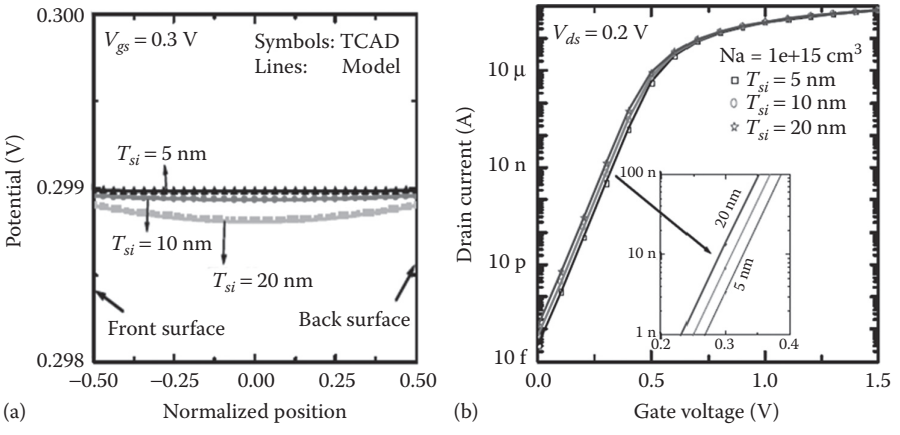

FIGURE 9.7
Drain current model showing volume inversion in lightly doped DG-nMOSFETs: (a) simulated potential profile in the body between the front and back surfaces in volume inversion; (b) subthreshold $I_{ds} - V_{gs}$ plots for different body thicknesses showing volume inversion (flat potential profile) simulated by the drain current model and numerical device simulation (TCAD); symbols represent TCAD and lines represent compact model; device data are $N_a = 1 \times 10^{15}$ cm^{-3} and $T_{ox} = 2$ nm; ($T_{si} \equiv t_{fin}$). (Data from M.V. Dunga et al., *IEEE Symposium on VLSI Technology*, pp. 60–61, 2007.)

9.3.2.1 Short Channel Effects

SCEs originate from 2D electrostatics where the drain significantly affects the potential barrier at the source due to its close proximity to source region. SCEs degrade the device performance through V_{th} roll-off and S degradation.

There are several approaches to model SCEs [66–70]. However, the approach assuming a parabolic potential function perpendicular to the silicon-insulator interface to solve the 2D Poisson's equation is shown to maintain a balance between the model accuracy and model computation time [68,69].

V_{th} roll-off: In order to model V_{th} roll-off in DG-FETs, 2D Poisson's equation is solved in the x direction into the body and in the y direction along the length of the channel, assuming that the inversion charge is negligible and the electric field E_x is independent of y whereas the electric field E_y is independent of x. Then assuming a parabolic potential distribution along the x direction, the minimum potential at the center of the channel $\phi_0(y)$ is determined [70]. Then the minimum potential $\phi_{c,min}$ [61] is expressed in terms of the terminal voltages V_{gs} and V_{ds}, L, and the characteristic field-penetration length λ, and is defined as

$$\lambda \equiv \sqrt{\frac{K_{si}\varepsilon_0}{2K_{ox}\varepsilon_0}\left(1+\frac{K_{ox}\varepsilon_0 t_{si}}{4K_{si}\varepsilon_0 t_{ox}}\right)t_{fin}t_{ox}} \tag{9.47}$$

λ is known as the scale length that defines the extent of penetration of the electric field from the drain into the body as function of physical parameters T_{ox} and t_{fin} and, therefore, the amount of SCE in a transistor. The change in V_{th} is then defined as

$$\Delta V_{th}\left(L,\lambda,V_{ds}\right) \equiv \lim_{L\to\infty}\phi_{c,min}\left(L,\lambda,V_{gs},V_{ds}\right) \tag{9.48}$$

The term $\Delta V_{th}(L, \lambda, V_{ds})$ is further enhanced with more parameters for simplicity of the parameter extraction procedure and to improve modeling accuracy [71]. In BSIM-CMG model, ΔV_{th} is subtracted from V_{fb} [72–74].

Figure 9.8 shows the dependence of ΔV_{th} on the gate oxide thickness and silicon body thickness. As the oxide thickness and body thickness decrease, the gate control on the body increases, thus suppressing SCE as expected [64].

Subthreshold slope degradation: The subthreshold swing, S, in a planar MOSFET is defined as (Equation 4.124)

$$S \equiv \left(\frac{d\left[\log\left(I_{ds}\right)\right]}{dV_{gs}}\right)^{-1} \cong \ln(10)v_{kT}\left(1+\frac{C_d}{C_{ox}}+\frac{C_{IT}}{C_{ox}}+\frac{C_{DSC}}{C_{ox}}\right) \tag{9.49}$$

where:

C_d is the depletion capacitance associated with the depletion region

C_{IT} is the capacitance due to interface states

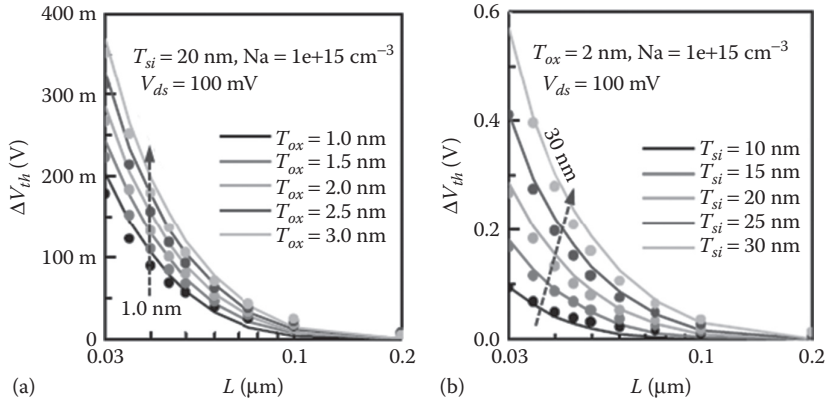

FIGURE 9.8
Drain current model used to simulate SCE in lightly doped DG-nMOSFETs through threshold voltage roll-off for different: (a) oxide thickness and (b) body thickness; symbols represent TCAD and lines represent compact model ($T_{si} \equiv t_{fin}$). (Data from M.V. Dunga et al., *IEEE Symposium on VLSI Technology*, pp. 60–61, 2007.)

C_{DSC} is the coupling capacitance between source/drain to channel, which has similar L, λ, and V_{ds} dependencies as ΔV_{th} discussed earlier

The degradation in subthreshold swing is then modeled through a modification in v_{kT} as

$$nv_{kT} \equiv \left(1 + \frac{C_d + C_{IT} + C_{DSC}}{C_{ox}}\right) v_{kT} \tag{9.50}$$

where nv_{kT} is substituted for v_{kT} in all bias-dependent calculations.

9.3.2.2 Quantum Mechanical Effects

Quantum mechanical confinement of inversion carriers is well known in bulk MOSFETs for a long time [13,75,76]. The large vertical electric field leads to strong band bending at the surface and the inversion carriers are confined to dimensions along the length and width of the transistor as shown in Figure 9.9a. This carrier confinement, also known as electrical confinement (EC), leads to splitting of energy bands into discrete sub-bands, which reflects as an increase in the threshold voltage of the transistor and a decrease in the gate capacitance, both of which act to reduce the current drive of the transistor [13,61].

In the case of DG-FETs, unlike bulk FETs, there is strong carrier confinement even at low electric fields, making the QME (quantum mechanical effect) even more complex [77]. The carriers are bounded by gate insulator on two sides, which is similar to carriers confined in a rectangular well [61,78–80].

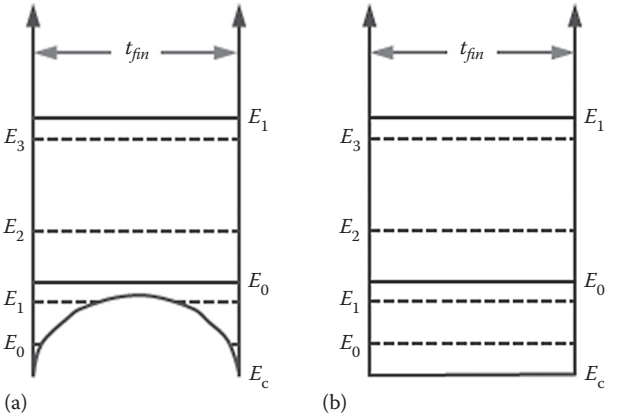

FIGURE 9.9
Energy-band diagrams showing the carrier confinement and associated quantization of electronic energy levels in DG-MOSFETs: (a) electrical confinement due to band bending at the top and bottom gate silicon/SiO_2 interface and (b) structural confinement due to ultrathin body.

This is referred to as structural confinement (SC) since it arises from the very physical structure of DG-FET as shown in Figure 9.9b. In order to capture the QME in its entirety it is necessary to model the effect of both EC and SC (Figure 9.9) on the performance of DG-FETs. Several groups have reported different analytical and numerical approaches to capture the QME in DG-FETs [78–80].

The quantum mechanical confinement of the inversion carriers increases the device V_{th}, degrades the gate capacitance, and reduces the effective width of the device (see Figure 9.7a) due to a shift in the inversion charge centroid as discussed in Section 3.4.2.2 (Figure 3.19) away from the Si/SiO2 interface [13,61]. A shift in the bottom of the conduction/valence band due to the SC [61] is used to modify V_{ch} at the source and drain SPEs. In order to model EC, the bias-dependent charge centroid thickness Δz is used to modify T_{ox} (Equation 3.82) and calculate the reduction in the width of the device [79]. The simulation results are in an excellent agreement with those calculated from a self-consistent Schrödinger–Poisson approach [61].

9.3.2.3 Mobility Degradation

Similar to surface mobility degradation in bulk MOSFETs discussed in Section 5.3.1 (Figure 5.9b), the degradation of carrier mobility in FinFET also occurs due to four main scattering mechanisms: Coulomb scattering, acoustic phonon scattering, surface roughness scattering, and optical phonon scattering. The first three scattering mechanisms have vertical (transverse) field dependency and they are each dominant at different regions of device operation: Coulomb scattering at weak inversion, acoustic phonon scattering at mid-inversion, and surface roughness scattering at strong inversion (Figure 5.9b).

Similar to bulk MOSFETs (Section 5.3.1), these mechanisms together are modeled through a submodel called *low field mobility degradation* and used to get the *effective* mobility [71].

At high lateral field due to high applied V_{ds}, the dominant scattering mechanism is optical phonon scattering since the electrons are able to gain enough energy to emit optical phonons. This high lateral field scattering causes the carrier velocity saturation. The velocity saturation is calculated using a submodel called *current saturation* and it degrades the drain-to-source current directly [71].

9.3.2.4 Series Resistances

In thin body source-drain transistors, series resistance is large. In order to reduce the parasitic resistances in FinFETs and UTB transistors, raised source-drain regions are used in device architecture [Figure 9.4]. Thus, the parasitic source-drain resistance submodel includes a bias-dependent extension resistance R_{ext}, a spreading resistance R_{sp}, and a distributed contact resistance R_{con}.

The components of contact resistance include resistance ΔR_s of the raised source-drain bulk regions and silicon/silicide inter-face resistance ΔR_c. And, R_{con} is modeled as a lumped resistance using a distributed network.

The spreading resistance R_{sp} is due to *current crowding* as the current flows from the raised drain region into the drain extension; this results in an increase in the resistance by R_{sp}. The spreading resistance is, modeled in terms of the device and source-drain areas and a shape parameter [81].

The extension resistance R_{ext} contributes the most to the series resistance. The fringe field from the gate can cause surface accumulation at the interfaces of the extension region and the gate oxide/offset spacer; this modulates the resistivity of the region and makes R_{ext} bias-dependent. R_{ext} is modeled as a resistance network with two bias-independent resistances R_{ext1} and R_{ext2}, and a bias-dependent resistance R_{acc}. Since the exact extension doping profile is often unknown, analytical expressions with fitting parameters are used to obtain the values of these components of R_{ext} [81].

9.4 Independent Multiple-Gate FET Model

The model developed for common-gate FinFETs cannot be used for transistors with different gate dielectric thickness and independently biased gate terminals. In this section, we will derive a surface potential–based compact model targeted for UTB-SOI MOSFETs. The model could be used for computer analysis of emerging devices including graphene nanoribbon transistors [22,23,52]. Many of the real-device effects presented for a CMG model can be used with appropriate changes for independent gate operation. Thus, only a description of the core model is presented in the following section.

9.4.1 Electrostatics

In order to derive electrostatic potential of asymmetric independent DG-FETs, let us consider 2D cross-sectional view of the channel as shown in Figure 9.10. The asymmetric independent DG-FET includes different front- and back-gate dielectric thicknesses (T_{ox1} and T_{ox2}) and different gate-work functions (ϕ_{M1} and ϕ_{M2}). Since the threshold voltage of an independent DG-FET can be optimized by adjusting the back-gate bias (V_{bg}), there is no need for significant body doping, N_b. Therefore, we can develop surface potential-based model using a lightly doped body so that $Q_b << Q_i$.

Let us consider GCA, Boltzmann's distribution function, an undoped channel, and only the dominant mobile carriers in deriving the surface potential. Then Poisson's equation can be written as

$$\frac{d^2\phi(x,y)}{dx^2} = \frac{q}{K_{si}\varepsilon_0}\left\{n_i \exp\left[\frac{\phi(x,y)-V_{ch}(y)}{v_{kT}}\right]\right\} \tag{9.51}$$

Again, using the identity (Equation 3.47) $(d/dx)(d\phi/dx)^2 = 2(d\phi/dx)\cdot(d^2\phi/dx^2)$ in Equation 9.51 and integrating the resultant expression along the x axis, we can show that

$$E_{s1}^2 - E_{s2}^2 = \frac{2qn_i v_{kT}}{K_{si}\varepsilon_0}\left\{\exp\left[\frac{\phi_{s1}-V_{ch}(y)}{v_{kT}}\right] - \exp\left[\frac{\phi_{s2}-V_{ch}(y)}{v_{kT}}\right]\right\} \tag{9.52}$$

where:

E_{s1} and E_{s2} are the surface electric fields at the front and back gates, respectively

ϕ_{s1} and ϕ_{s2} are the front and back surface potentials, respectively, as shown in Figure 9.10

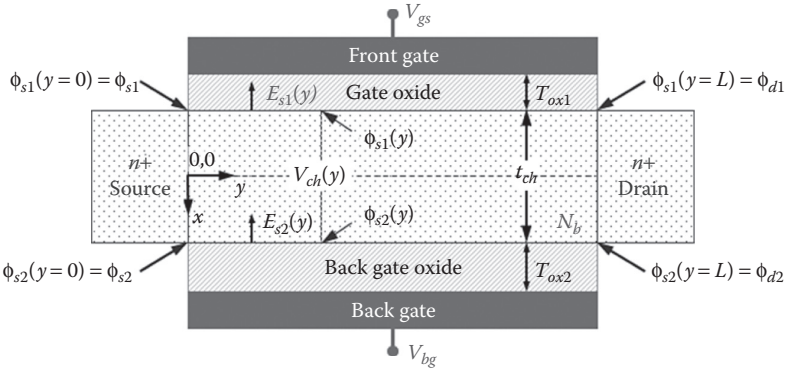

FIGURE 9.10
2D cross-sectional view of the channel region of a planar independent DG-FET; T_{ox1} and T_{ox2} are the front and back gate oxide thickness, respectively; t_{ch} and N_b are the substrate thickness and doping concentration, respectively.

Using Gauss's law at the front- and back-gate silicon surfaces, we can write

$$E_{s1} = \frac{1}{K_{si}\varepsilon_0} C_{ox1}\left(V_{fg} - V_{fb1} - \phi_{s1}\right)$$
$$E_{s2} = \frac{1}{K_{si}\varepsilon_0} C_{ox2}\left(V_{bg} - V_{fb2} - \phi_{s2}\right) \tag{9.53}$$

where:

V_{fg} and V_{bg} are the front- and back-gate voltages, respectively
V_{fb1} and V_{fb2} are the flat band voltages for the front and back gates, respectively
C_{ox1} and C_{ox2} are the front- and back-gate oxide capacitances given by $K_{ox}\varepsilon_0/T_{ox1}$ and $K_{ox}\varepsilon_0/T_{ox2}$, respectively, where T_{ox1} and T_{ox2} are the front and back oxide thicknesses, respectively, and K_{ox} is the dielectric constant of oxide

Substituting Equation 9.53 in Equation 9.52, we get an implicit equation in ϕ_{s1} and ϕ_{s2}.

Now, in order to solve the implicit Equation 9.52 with two interdependent unknowns, ϕ_{s1} and ϕ_{s2}, the back surface is approximated to be always in weak inversion. Using the equation for the potential of a capacitive divider node held between the two potentials ϕ_{s1} and V_{bg}, we can write

$$\phi_{s2} = \alpha_{si}\phi_{s1} + \alpha_{ox}\left(V_{bg} - V_{fb2}\right) \tag{9.54}$$

where

$$\alpha_{si} = \frac{C_{si}}{C_{si} + C_{ox2}}; \alpha_{ox} = \frac{C_{ox2}}{C_{si} + C_{ox2}}$$

and, $C_{si} = K_{si}\varepsilon_0/t_{ch}$, with t_{ch} being the channel thickness.

Substituting Equation 9.54 in Equation 9.52, the implicit SPE for the IMG transistor basic model is obtained

$$f \equiv \left[\frac{C_{ox1}\left(V_{fg} - V_{fb1} - \phi_{s1}\right)}{K_{si}\varepsilon_0}\right]^2 - \left[\frac{V_{bg} - V_{fb2} - \phi_{s2}}{t_{ch} + \left(K_{si}/K_{ox}\right)T_{ox2}}\right]^2 - \frac{2qn_i v_{kT}}{K_{si}\varepsilon_0}\exp\left(\frac{\phi_{s1} - V_{ch}}{v_{kT}}\right)$$
$$+ \frac{2qn_i v_{kT}}{K_{si}\varepsilon_0}\exp\left[\frac{\alpha_{ch}\phi_{s1} + \alpha_{ox}\left(V_{bg} - V_{fb2}\right) - V_{ch}}{v_{kT}}\right] = 0 \tag{9.55}$$

Equation 9.55 is solved using Householder's method to obtain the front surface potential and electric field, ϕ_{s1} and E_{s1}, respectively, at the source end (by setting $V_{ch}(y = 0) = V_s$) [82]. The front surface potential and electric field, ϕ_{d1} and E_{d1}, are also found for the drain end (by setting $V_{ch}(y = L) = V_d$). The corresponding back-gate surface potentials ϕ_{s2} and ϕ_{d2} and electric fields E_{s2} and E_{d2} are then computed from Equations 9.54 and 9.53, respectively.

Finally, assuming lightly doped body, that is, $Q_b << Q_i$, so that $Q_s \cong Q_i$, we get the expression for the inversion charge density as

$$Q_i = K_{si}\varepsilon_0\left(E_{s1} - E_{s2}\right) \tag{9.56}$$

9.4.2 Drain Current Model

For long channel UTB-FET devices, the drain current is derived by solving drift-diffusion transport expression given by Equation 9.33. Integrating both sides of Equation 9.33 and considering the fact that under quasistatic operation I_{ds} is constant along the channel, it is possible to express Equation 9.33 in its integral form as

$$I_{ds} = \left(\frac{W}{L}\right)\mu(T)\int_0^L Q_i(y)\left[\frac{dV_{ch}(y)}{dy}\right]dy \tag{9.57}$$

Again, assuming that the back surface is weak, a simplified form of surface potential expression

$$E_{s1}^2 - E_{s2}^2 = \frac{2qn_i v_{kT}}{K_{si}\varepsilon_0}\left[\exp\left(\frac{\phi_{s1} - V_{ch}}{v_{kT}}\right)\right] \tag{9.58}$$

is used to compute the drain current by following the procedure described next:

1. Solving for E_{s1} in Equation 9.58 and using it in Equation 9.56, we can write

$$Q_i(y) = \sqrt{2qn_i K_{si}\varepsilon_0 v_t\left\{\exp\left[\frac{\phi_{s1} - V_{ch}(y)}{v_t}\right]\right\} + \left(K_{si}\varepsilon_0 E_{s2}\right)^2} - K_{si}\varepsilon_0 E_{s2} \tag{9.59}$$

2. Taking the derivatives of both sides of Equation 9.59 with respect to y, it is possible to write

$$Q_i(y)\frac{dV_{ch}(y)}{dy} = Q_i(y)\frac{d\phi_{s1}(y)}{dy} - \eta v_{kT}\frac{dQ_i(y)}{dy} \tag{9.60}$$

where

$$\eta = 2 - \frac{2\varepsilon_{si}E_{s2}(y)}{Q_i(y) + 2\varepsilon_{si}E_{s2}(y)} \tag{9.61}$$

Here, η varies from 1 to 2 going from subthreshold to strong inversion and is a function of y. To simplify the integral in Equation 9.57, η can be approximated to be independent of position, thus replacing $Q_i(y)$ and $E_{s2}(y)$ by their average values at the source and drain ends.

3. Evaluating the integral in Equation 9.57 using Equation 9.60 leads to the following basic equation for I_{ds} [49]

$$I_{ds} = \left(\frac{W}{L}\right)\mu(T)\cdot\left[\frac{Q_{is}+Q_{id}}{2} + v_{kT}\left(\phi_{s1,d}-\phi_{s1,s}\right) + \eta v_{kT}\left(Q_{is}-Q_{id}\right)\right] \tag{9.62}$$

The model has been extensively verified for a wide range of reliability and scalability [83]

9.5 Dynamic Model

9.5.1 Common Multigate *C–V* Model

This section presents the dynamic model of the CMG DG-FETs for transient analysis of the devices in circuit CAD. The intrinsic capacitance model that describes the transient behavior of the transistors are derived from the terminal charges as described in Chapter 6.

For DG-FETs, the total charge in the body is given by the charges on the top- and bottom-gate electrodes. The total charge is computed by integrating the charge along the channel. Since the two gates are electrically interconnected, we have

$$Q_G = 2WC_{ox}\int_0^L \left[V_{gs}-V_{fb}-\phi(y)\right]\cdot dy \tag{9.63}$$

where:

Q_G denotes the charge on the electrically interconnected gate

The inversion charge in the body is divided between the source and the drain terminals using Ward–Dutton charge partition approach discussed in Chapter 6 [84,85]. The charge on source terminal (Q_S) is given by

$$Q_S = -2WC_{ox}\int_0^L \left(1-\frac{y}{L}\right)\cdot\left[V_{gs}-V_{fb}-\phi(y)-\frac{Q_b}{C_{ox}}\right]\cdot dy \tag{9.64}$$

Using charge conservation principle, the charge on the drain terminal (Q_d) can be expressed as

$$Q_D = -2WC_{ox}\int_0^L \frac{y}{L}\left[V_{gs}-V_{fb}-\phi(y)-\frac{Q_b}{C_{ox}}\right]\cdot dy \tag{9.65}$$

The surface potential as a function of the position y along the length of the transistor, $\phi_s(y)$ is obtained using current continuity. Current continuity states that the current is conserved along the length of the transistor.

$$I_d(L) = I_d(y), \quad \text{where } 0 \le y \le L \tag{9.66}$$

The expression for the drain current in Equation 9.46 is very complex and is not practical for applying current continuity. For the purpose of determining $\phi_s(y)$, a simplified version of *I–V* model as shown below is used [61,72]

$$I_{ds}(y) = 2\mu \cdot \left(\frac{W}{y}\right)\left[g(Q_{is}) - g(Q_{id})\right] \tag{9.67}$$

where the function $g(Q_i(y))$ follows from Equation 9.46 after neglecting the third term in the square bracket is defined as

$$g(Q_i) = \frac{Q_i^2}{2C_{ox}} + 2v_{kT}Q_i \tag{9.68}$$

The approximate Equations 9.67 and 9.68 retain good accuracy in the strong inversion regime but overestimate the drain current in the subthreshold regime. The advantage of using a mathematically simple analytical expression for terminal charges outweighs the resulting error in the accuracy of *C–V* model in the subthreshold regime. Using Equations 9.67 and 9.68, $\phi_s(y)$ can be expressed as

$$\frac{y}{l}.(B - \phi_{s0} - \phi_{sL}) \cdot (\phi_{sL} - \phi_{s0}) = \left[B - \phi_{s0} - \phi_s(y)\right] \cdot (\phi_s(y) - \phi_{s0}) \tag{9.69}$$

where ϕ_{s0} and ϕ_{sL} represent the surface potential at the source and drain ends, respectively, and the parameter *B* is defined as

$$B = 2\left(V_{gs} - V_{fb} - \frac{Q_b}{C_{ox}} + 2v_{kT}\right) \tag{9.70}$$

The terminal charges are obtained by substituting $\phi_s(y)$ in Equations 9.63 through 9.65 and evaluating of the integrals [73] so that

$$\begin{aligned}
Q_G &= 2WLC_{ox}\left[V_g - V_{fb} - \frac{\phi_{s0} + \phi_{sL}}{2} + \frac{(\phi_{sL} - \phi_{s0})^2}{6(B - \phi_{sL} - \phi_{s0})}\right] \\
Q_D &= -2WLC_{ox}\left[\frac{V_g - V_{fb} - (Q_b/C_{ox})}{2} - \frac{\phi_{s0} + \phi_{sL}}{4} + \frac{(\phi_{sL} - \phi_{s0})^2}{60(B - \phi_{sL} - \phi_{s0})}\right. \\
&\quad \left. + \frac{(5B - 4\phi_{sL} - 6\phi_{s0}).(B - 2\phi_{sL}) \cdot (\phi_{s0} - \phi_{sL})}{60(B - \phi_{sL} - \phi_{s0})^2}\right] \\
Q_S &= -(Q_{fg} + Q_{bg} + Q_B + Q_D)
\end{aligned} \tag{9.71}$$

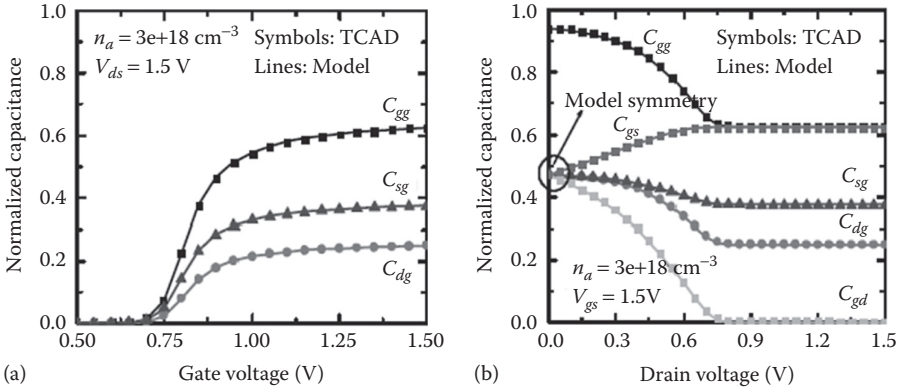

FIGURE 9.11
Dynamic model of symmetric DG-MOSFETs: modeling transcapacitances as a function of (a) gate voltage and (b) drain voltage; Model symmetry is seen at $V_{ds} = 0$ where $C_{dg(gd)} = C_{sg(gs)}$; n_a = body doping concentration; symbols represent TCAD and lines represent compact model. (Data from F. M.V. Dunga et al., *IEEE Symposium on VLSI Technology*, pp. 60–61, 2007.)

The expressions for terminal charges are continuous and are valid over subthreshold, linear, and saturation regimes of operation.

Equation 9.71 forms the *C–V* model for BSIM-CMG. The terminal charges are used as state variables in the circuit simulation. All the capacitances are derived from the terminal charges to ensure charge conservation. The capacitances are defined as

$$C_{ij} = \frac{\partial Q_i}{\partial V_j} \tag{9.72}$$

where:

i and j denote the multigate FET terminals

Note that C_{ij} satisfies

$$\sum_i C_{ij} = \sum_j C_{ij} = 0 \tag{9.73}$$

due to charge conservation.

The capacitances from *C–V* model are plotted as a function of gate voltage and drain voltage in Figure 9.11a and b, respectively.

9.5.2 Independent Multigate *C–V* Model

We model the *C–V* using a charge-based approach [84,85] to ensure charge conservation. The charge associated with each terminal is modeled. The capacitive current flowing into each terminal is expressed as the time derivative of charge.

$$I_x = \frac{dQ_x}{dt} = \sum_y C_{xy} \frac{dV_y}{dt} \tag{9.74}$$

where $x, y = d, fg, bg, s$; each transcapacitance is defined as

$$C_{xy} = \frac{\partial Q_x}{\partial V_y} \tag{9.75}$$

The charge associated with the front gate fg can be calculated as

$$Q_{fg} = W \int_0^L C_{ox1} \left[V_{fg} - \Delta\Phi_1 - \phi_{s1}(y) \right] dy \tag{9.76}$$

where:

$\Delta\Phi_1$ is the work function of the front gate with reference to that of $n+$ source

In order to integrate Equation 9.76, the relation between front surface potential $\phi_{s1}(y)$ and position y is needed. This can be obtained by applying current continuity to Equation 9.62.

$$I_{ds}.y = \mu(T).W \left\{ \frac{Q_{is} + Q_i(y)}{2} \left[\phi_{s1}(y) - \phi_{s1,s} \right] + v_{kT} \left[Q_{is} - Q_i(y) \right] \right\} \tag{9.77}$$

Since $Q_i(y)$ is unknown, the capacitor divider approximation is used to relate the front surface potential ϕ_{s1} and charge Q_i:

$$Q_i(y) = C_{ox1} \left[V_{fg} - \Delta\Phi_1 - \phi_{s1}(y) \right] + \frac{C_{ox2} C_{si}}{C_{ox2} + C_{si}} \left[V_{bg} - \Delta\Phi_2 - \phi_{s2}(y) \right] \tag{9.78}$$

Combining Equations 9.77 and 9.78 and noting that $Q_{is} = Q_{is} \left[\phi_{s1}(y) = \phi_{s1,s} \right]$, we obtain the position dependence of surface potential as

$$y = \mu C_{ox1} \frac{W}{I_{ds}} \left[\phi_{s1}(y) - \phi_{s1,s} \right] \left\{ \begin{array}{l} V_{fg} - \Delta\Phi_1 - \dfrac{\phi_{s1,s} - \phi_{s1}(y)}{2} \\ + \gamma_c . \left[V_{bg} - \Delta\Phi_2 - \dfrac{\phi_{s1,s} - \phi_{s1}(y)}{2} \right] + v_{kT} \left(1 + \gamma_c \right) \end{array} \right\} \tag{9.79}$$

where:

$$\gamma_c = \frac{C_{ox2} \,||\, C_{si}}{C_{ox1}}$$

Substituting Equation 9.79 in Equation 9.76 and performing integration, we get

$$Q_{fg} = C_{ox1}WL\left\{V_{fg} - \Delta\Phi_1 - \frac{\phi_{s1,s} + \phi_{s1,d}}{2} + \frac{B'\left(\phi_{s1,d} - \phi_{s1,s}\right)^2}{6\left[A' - B'\left(\phi_{s1,d} + \phi_{s1,s}\right)\right]}\right\} \tag{9.80}$$

where

$$A' = V_{fg} - \Delta\Phi_1 + \gamma_c \cdot \left(V_{bg} - \Delta\Phi_2\right) + v_{kT}\left(1 + \gamma_c\right) \tag{9.81}$$

and,

$$B' = \frac{1}{2}\left(1 + \gamma_c\right) \tag{9.82}$$

The charge associated with the back gate can be simply calculated by replacing $\phi_{s1,s(d)}$ with $\phi_{s2,s(d)}$, swapping $\left(V_{fg} - \Delta\Phi_1\right)$ and $\left(V_{bg} - \Delta\Phi_2\right)$, and swapping C_{ox1} and C_{ox2} in Equation 9.80, following an argument of symmetry.

The front- and back-gate charges are further partitioned into a source component and a drain component according to Ward–Dutton charge partition method [84,85]. The drain charge associated with the front gate is given by [79]

$$Q_{D1} = -W\int_0^L C_{ox1}\left[V_{fg} - \Delta\Phi_1 - \phi_{s1}(y)\right]\frac{y}{L}dy \tag{9.83}$$

After using Equation 9.79 and integrating, we obtain

$$Q_{D1} = -\frac{C_{ox1}WL}{2}\left\{\begin{array}{l} V_{fg} - \Delta\Phi_1 - \dfrac{\phi_{s1,s} + \phi_{s1,d}}{2} + \dfrac{B\left(\phi_{s1,d} - \phi_{s1,s}\right)^2}{30\left[A - B\left(\phi_{s1,s} + \phi_{s1,d}\right)\right]} \\ -\dfrac{\left(5A - 4B\phi_{s1,d} - 6B\phi_{s1,s}\right).\left(A - 2B\phi_{s1,d}\right)\left(\phi_{s1,d} - \phi_{s1,s}\right)}{30\left[A - B\left(\phi_{s1,s} + \phi_{s1,d}\right)\right]^2} \end{array}\right\} \tag{9.84}$$

Similarly, the drain charge, Q_{D2} associated with the back gate is obtained by replacing $\phi_{s1,s(d)}$ with $\phi_{s2,s(d)}$, swapping $\left(V_{fg} - \Delta\Phi_1\right)$ and $\left(V_{bg} - \Delta\Phi_2\right)$, and swapping C_{ox1} and C_{ox2} in Equation 9.84.

The total drain charge is the sum of Q_{D1} and Q_{D2}. Since Q_S, Q_D, Q_{fg}, and Q_{bg} must sum up to 0, the source charge can be calculated as

$$Q_S = -Q_{fg} - Q_{bg} - Q_D \tag{9.85}$$

Similar to Figure 9.11, the transcapacitances can be computed from the above terminal charges.

9.6 Summary

This chapter presented an overview of the present state-of-the-art surface potential–based compact models of thin-body CMG and IMG FET devices for circuit CAD. Each device model consists of a core model for large devices and real device submodels to analyze the physical and geometrical effects on these devices. The basic features of the model include capturing the important physics of thin-body multigate transistors such as the volume inversion and the dynamic V_{th} shift for body bias in ultrathin body transistors. The models are valid for digital as well as analog circuit analysis with the *C–V* models that simulate the transcapacitances. This chapter is intended to provide readers the present state-of-the-art modeling activities in thin-body FET devices. The detailed models and modeling methodologies including updates can be found in the literature [74].

Exercises

9.1 Complete the mathematical steps following the procedure described in Chapter 3 to derive Equation 9.13 for channel potential $\phi_1(x, y)$ at any point (x, y) in the channel of a typical symmetric DG-MOSFET device.

9.2 Complete the mathematical steps following the procedure described in Chapter 3 to derive Equation 9.17 for channel potential $\phi_2(x, y)$ at any point (x, y) in the channel of a typical symmetric DG-MOSFET device.

9.3 Use Equations from exercises 9.1 and 9.2 to derive:

a. Vertical electrical field at any point y along the channel of the symmetric DG-MOSFET device

b. Gate voltage for a fully depleted symmetrical DG-MOSFET structure

9.4 What is the volume inversion in DG-MOSFETs? Describe the effect of volume inversion on DG-MOSFET device performance.

9.5 Describe the difference between the electrical and structural Quantum Mechanical effects in DG-MOSFETs; qualitatively plot the centroid of inversion charge as a function of body thickness. Explain your results.