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Beyond-CMOS Transistor Models: Tunnel FETs

10.1 Introduction

As the CMOS (complementary metal-oxide-semiconductor) technology approaches its ultimate scaling limit of MOSFET (metal-oxide-semiconductor field-effect transistors) device miniaturization, extensive global search for beyond-CMOS devices has been continued to *rebooting computing*. This new device technology must be *green* (i.e., energy efficient) and continue to increase packing density of devices as well as device functionalities in an IC (integrated circuit) chip in the same rate as the CMOS technology. A number of potential beyond-CMOS devices involving present as well as new state variables and communication frameworks have been reported [1–3]. Among the potential beyond-CMOS devices, the devices that compete directly with the MOSFETs in power, area, and speed in the commercial temperature range 0°C–75°C and can utilize the existing CMOS facility are of special interest to device technologists and IC manufacturers. These devices are aimed at supply voltages less than a 0.5 V with subthreshold swing (S) lower than that of MOSFETs.

The scaled MOSFET devices, discussed in Chapter 5, are limited by short channel effect (SCE) and S. As discussed in Chapter 9, the ultrathin-body (UTB) MOSFETs are adopted to surmount the challenges of SCEs. However, S in UTB-MOSFETs is still limited by the Boltzmann distribution of carriers to a minimum value of 60 mV per decade of channel current at room temperature. Therefore, the devices that can achieve switching mechanisms less than 60 mV per decade are highly desirable for beyond-CMOS *green IC technology*. The potential device structures with the desirable characteristics include tunneling [4–6], impact ionization [7–10], ferroelectric dielectrics [11], and mechanical gate [12–14] field-effect transistors (FETs). Among the emerging devices, the tunnel FET (TFET) is one of the potential candidates for beyond-CMOS technology that can be controlled at voltages well under a volt with steep S and does not have the delays associated with positive feedback that are intrinsic to impact ionization, ferroelectricity, and mechanical devices [15].

Therefore, in this chapter, an overview of the present state-of-the-art compact modeling activities on TFETs is presented. First of all, the basic features of TFET device structure are presented. Then the physics of TFET device operation is discussed. And, finally, the compact modeling activities on TFETs for circuit CAD is presented. TFET as a green transistor has the potential to provide an acceptable device performance as the supply voltage approaches to 0.1 V beyond-CMOS devices.

10.2 Basic Features of TFETs

The most commonly referred TFETs are gated *p-i-n* diodes or gated *p-n* diodes with an *intrinsic channel* as shown in Figure 10.1. In order to switch the device on, the *pn*-junction is reverse biased and a voltage (V_g) is applied to the gate to modulate the device characteristics. In order to be consistent with MOSFET device technology, the names of the TFET device terminals are chosen such that the biasing conditions for MOSFETs and TFETs are the same. Since a reverse bias with $V_g > 0$, $V(n+) > 0$, and $V(p+) = 0$ is needed across the *p-i-n* structure to trigger tunneling similar to the biasing condition of an nMOSFET with $V_g > 0$, $V_d > 0$, and $V_s = 0$, the *n*+ region of a *p-i-n* TFET in Figure 10.1 is referred to as its drain and *p*+ region as its source for an *n*-type TFET (nTFET). Similarly, for a *p*-type TFET (pTFET), *p*+ region is referred to as the drain and *n*+ region is the source to be consistent with biasing condition of a pMOSFET device discussed in Chapters 4 and 5.

Thus, Figure 10.1 shows an nTFET device structure, with a heavily doped *p*+ source region and a heavily doped *n*+ drain region. On the other hand, in a pTFET, the source is doped with *n*+ and the drain is doped with *p*+. It is observed from Figure 10.1 that a *p-i-n* TFET device structure is similar to that of a conventional MOSFET except that the source is doped with the opposite dopant type with respect to the drain [4]. Thus, as shown in Figure 10.1,

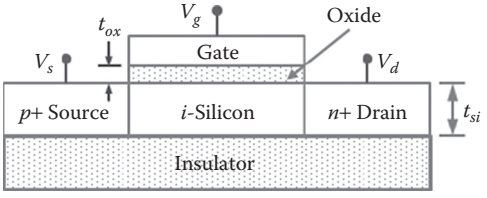

FIGURE 10.1
2D cross section of an ideal single gate *p–i–n* TFET device structure with a *p*+ source, an intrinsic silicon (*i*-silicon) channel, and an *n*+ drain regions on an insulating substrate; t_{ox} and t_{si} are the gate oxide thickness and body thickness, respectively; V_s, V_g, and V_d are the source, gate, and drain voltages, respectively.

a typical TFET device includes an ultrathin body on the top of a buried oxide layer, a gate electrode placed on the top of an ultrathin-gate dielectric, and a heavily doped source region with doping type opposite to a heavily doped drain region.

In principle, the same *p-i-n* TFET device structure shown in Figure 10.1 can be used for *n*-type or *p*-type operation by appropriate biasing conditions. In this respect, if a TFET is designed with symmetry between the *n*+ and *p*+ regions including similar doping levels, gate alignment, and geometries, the device shows *ambipolar behavior*, that is, the transfer characteristics resemble those of a pTFET when $V_{gs} < 0$ and $V_{ds} < 0$, and those of an nTFET when $V_{gs} > 0$ and $V_{ds} > 0$. Thus, in principle, the TFET is an ambipolar device showing *p*-type behavior with dominant hole conduction and *n*-type behavior with dominant electron conduction.

In another embodiment, a TFET can be used as a *fully depleted channel* device [16]. In the case of a fully depleted channel TFET, the metal gate work function of the gate is chosen to fully deplete the channel in the off-state. In the on-state, the Zener tunneling is enabled [17]. In order to achieve high current density, abrupt doping profiles are required with degenerately doped *n*+ and *p*+ regions [16].

One of the key challenges of TFET fabrication is that the gate must be self-aligned to the junction. If the gate is underlapped, that is, the junction is moved outside the gate edge, the field control is degraded along with the degradation of *S*. And, if the gate is overlapped, that is, the junction is under the gate metal, the field in the on-condition depletes carriers on the source side of the junction decreasing the tunneling injection. Thus, the gate must be placed with a high precision approaching that of the lateral potential variation length, which is typically less than 10 nm [18] in these heavily doped TFET structures.

Similar to MOSFETs, the gate control of the channel in TFETs can be improved by using double-gate (DG) structures. In order to increase the on-current (I_{on}), a degenerately doped pocket region can be used under the gate [19]. In addition to increasing I_{on}, the pocket also offers lower *S* by aligning the gate field with the internal tunnel junction field. TFET device structure is continuously evolving with the development of process technology to minimize access resistance, form abrupt degenerate junctions, self-align gate, and realize ultrathin channel.

A TFET-type device structure has been studied by Stuetzer [20] in 1952 predating Esaki's discovery of *pn*-interband tunneling [21]. In this study, the basic characteristics along with the ambipolar nature of the current–voltage (*I*–*V*) characteristics have been reported in the field gating of a lateral germanium *pn*-junction. This study also shows the dependence of the transistor characteristics on gate placement with respect to the *pn*-junction. In 1977, Quinn et al. [22] designed a surface-channel MOS tunnel junction by replacing the *n*+ source region of an nMOSFET device with a highly degenerate *p*+ source region to measure the sub-band splitting and transport properties of

tunneling between a bulk source and a two-dimensional (2D) surface channel. This device structure is essentially a *lateral* TFET. The first known vertical TFET has been reported by Leburton et al. [23] in 1988 in the design of a high-speed transistor with the gate to control the *negative differential resistance* (NDR).

In 1992, Baba [24] independently proposed the lateral TFET device structure similar to that reported by Quinn to use the gate of the transistor in controlling NDR. This transistor has been referred to as the *surface tunnel transistor* (STT). In the 1990s, the STTs fabricated in different semiconductor materials such as gallium arsenide (GaAs), silicon-on-insulator (SOI), silicon (Si), and indium gallium arsenide (InGaAs) have been widely studied to show NDR at room temperature [25–33]. In this period, the focus of the STTs has been on field control of the forward-biased characteristic of the Esaki tunnel junction and in ways to utilize the NDR characteristics.

The interest on TFET as the potential device for beyond-CMOS technology has grown since the reported gating of the reverse Zener tunneling current of STTs to achieve better scaling due to the absence of punch-through by Reddick and Amartunga in 1995 [34]. Subsequently, the gating of the Zener side of the tunnel junction of a fabricated Si *vertical* TFET along with its potential for low off-current (I_{off}) relative to the MOSFET has been reported by Hansch et al. in 2000 [35]. In 2004, the device characteristics of a lateral SOI TFET have been reported by Aydin et al. [36], and low S in the TFET has been reported by Wang et al. [4], Bhuwalka et al. [5], and Appenzeller et al. [6]. Theoretically, it is shown that in a TFET, $S < 60$ mV per decade at room temperature [37,38]. However, less than 60-mV per decade S has been reported in only a few TFETs based on carbon nanotubes (CNTs) [6,39], Si [40–43], germanium (Ge) [44], and p+Ge/n+Si [45] channels. TFET device structure is constantly evolving to outperform CMOS devices in comparable technology node [46].

10.3 Basic Theory of TFET Operation

10.3.1 Energy Band Diagram

The basic operating principle of a TFET can be understood from the energy band diagram shown in Figure 10.2 of the ideal device structure, shown in Figure 10.1. In Figure 10.2, the energy band diagram of a p–i–n TFET device under various biasing conditions is shown with reference to the structure in Figure 10.1. Figure 10.2a shows that in the off-state with zero bias ($V_{gs} = 0 = V_{ds}$), the majority carriers in the channel as well as in the drain regions see unsurmountable large potential barriers for tunneling and the only current flow through the device is due to the reverse-biased leakage current of the p–i–n structure. When a positive gate bias ($V_{gs} > 0$) is applied at the gate, the source channel junction is reverse biased, and therefore, the energy band of the channel region bends downward as shown in Figure 10.2b.

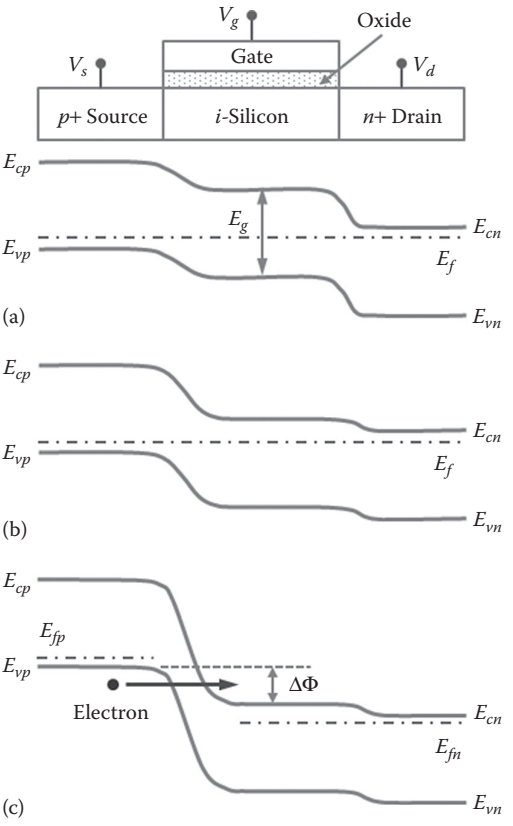

FIGURE 10.2
Energy band diagram taken laterally along the length of the *p-i-n* TFET structure: (a) off-state with $V_{gs} = V_{ds} = 0$; (b) gate modulation of the channel by $V_{gs} > 0$ and $V_{ds} = 0$; and (c) on-state with $V_{gs} > 0$ and $V_{ds} > 0$ leading to nFET-type behavior with the current flow set by the overlap of valence band electrons with the unfilled channel conduction band states. $\Delta\Phi$ is the window of tunneling; E_{cn} and E_{cp} represent the conduction band energies of the *n*-type and *p*-type semiconductors, respectively; E_{vn} and E_{vp} represent the valence band energies of the *n*-type and *p*-type semiconductors, respectively; E_f is the equilibrium Fermi level; E_{fn} and E_{fp} are the quasi-Fermi potentials of the *n*-type and *p*-type regions, respectively, under the applied bias; and E_g is the energy gap.

An additional positive drain bias ($V_{ds} > 0$) pulls down the Fermi levels in both the *n*-type drain and *i*-channel regions. If the downward shift of the bands is large enough to narrow the bandgap formed by the overlap of the conduction band and valence band at the source-channel junction, a tunneling path will be formed, allowing electrons to tunnel from the source to *i*-channel, as shown in Figure 10.2c. The tunneled electrons then move toward the *n*+ drain by drift-diffusion process, generating current flow in TFET devices. The gate modulation of the overlap region, defined as the *tunneling width* ($\Delta\Phi$), allows TFETs to achieve a lower *S* compared to the conventional MOSFETs.

10.3.2 Tunneling Mechanism

In a TFET the primary injection mechanism of charge carriers is *interband* tunneling [21] in which the charge carriers transfer from one energy band into another at a heavily doped *p*+*n*+ junction in contrast to MOSFETs where the charge carriers are thermally injected over a barrier. Interband tunneling was first observed in 1957 by Esaki [21] while studying narrow forward-biased *p*–*n* junctions called tunnel diode. However, the interband tunneling concept was first used by Zener in 1934 to explain the dielectric breakdown at a high electric field [17] and is known as the *Zener tunneling*, which is also referred to as the *band-to-band tunneling* (BTBT).

The Zener or interband tunneling can be realized in a reverse-biased *p-i-n* structure as shown in Figure 10.2. In a TFET, the interband tunneling can be switched *on* and *off* abruptly by controlling the band bending in the channel region by applying V_{gs}. As shown in Figure 10.2a, for a *p-i-n* TFET structure at $V_{gs} = 0$, the tunneling barrier is large, and the device is in the off-state. A $V_{gs} > 0$ pulls the energy bands down and reduces the tunneling barrier. Due to reduced energy barrier, the carriers can tunnel from the valence band in the source to the conduction band in the channel and the tunneling current increases. For a *p*+*n*+ tunnel junction, the tunneling current is determined by integrating the product of charge flux and the tunneling probability $T(E)$ from the energy states on the *p*+ side to those on the *n*+ side. And, $T(E)$ is calculated by applying Wentzel–Kramers–Brillouin (WKB) approximation of the *triangular* potential (Figure 10.3) at the tunnel junction [47–49] and is given by

$$T(E) \cong \exp\left(-\frac{4\sqrt{2m^{*}E_g^3}}{3q\hbar F}\right) \tag{10.1}$$

where:
m^* is the effective mass
E_g is the energy of the bandgap
q is the electronic charge
$\hbar$ is the reduced Plank's constant
F is the maximum electric field at the tunneling junction

Equation 10.1 derived by WKB approximation works properly in direct bandgap semiconductors, such as indium arsenide (InAs), and has limited accuracy for silicon and Ge structures or when quantum effects and phonon-assisted tunneling become dominant [50]. However, it has been successfully applied for all TFET devices.

Equation 10.1 is a general expression for interband tunneling transmission and can be modified appropriately for tunneling mechanism in TFETs. In Figure 10.3b, it is shown that the height and the width of the triangular potential barrier are $\Delta\Phi + E_g$ and λ, respectively. The magnitude of F corresponds

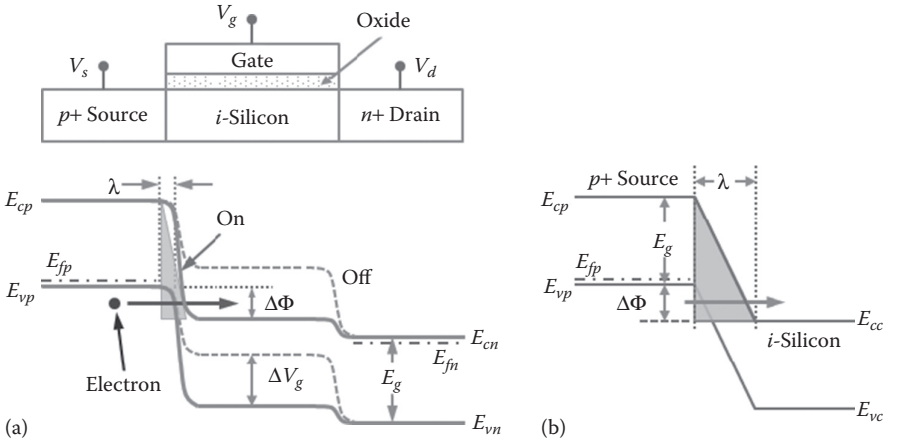

FIGURE 10.3
Interband tunneling mechanism in a TFET: (a) energy band diagram along the length of the *p-i-n* TFET in the on-state (solid lines) and off-state (broken lines). In the off-state, no empty states are available in the channel for tunneling from the source, so the off current is very low; increasing V_g pulls the conduction band energy of the channel below the valence band energy of the source so that interband tunneling can occur. This switches the device to the on-state in which electrons in the energy window, ΔΦ, can tunnel from the source valence band into the channel conduction band; (b) expanded schematic of the source-channel tunneling region showing the WKB approximation of the triangular potential barrier; λ is the screening tunneling length; ΔΦ is the window of tunneling; E_{cn} and E_{cp} represent the conduction band energies of the *n*-type and *p*-type semiconductors, respectively; E_{vn} and E_{vp} represent the valence band energies of *n*-type and *p*-type semiconductors, respectively; E_{fn} and E_{fp} are the quasi-Fermi potentials of the *n*-type and *p*-type regions under the applied bias; and E_g is the energy gap; and E_{cc} and E_{vc} are the conduction band and valence band energy of the channel, respectively.

to the slope of the energy bands, so that $qF = (\Delta\Phi + E_g)/\lambda$. Therefore, the tunneling probability for TFETs is given by [51]

$$T(E) \cong \exp\left[-\frac{4\lambda\sqrt{2m^* E_g^3}}{3\hbar\left(E_g + \Delta\Phi\right)}\right] \tag{10.2}$$

where:
ΔΦ is the energy range over which the tunneling can take place
λ is the *screening length* shown in Figure 10.3

There are four important conditions to trigger interband tunneling: available states to tunnel from, available states to tunnel to, a sufficiently narrow energy barrier for tunneling to occur, and conservation of momentum [48]. For interband tunneling in an indirect band gap semiconductor such as silicon, crystal *phonons* are necessary to conserve momentum. Therefore, E_g in the numerator of Equation 10.2 is replaced by $E_g - E_p$, where E_p is the phonon

energy and the effective mass m^* must then be changed to *reduce effective mass* m_r^* in the tunneling direction for accurate prediction of tunneling current in the indirect semiconductors.

In Equation 10.2, λ describes the spatial extent of the transition region at the source-channel interface as shown in Figure 10.3 and depends on the biasing condition and device dimension. λ is also known as the *screening length*, *natural length*, and *Debye length* that physically refers to the spatial extent of the electric field or the length over which an electric charge has an influence before being screened out by the opposite charges around it [52]. For all silicon TFETs, λ is given by [51]

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{a_g \varepsilon_{ox}} t_{ox} t_{si}} \tag{10.3}$$

where:

ε_{si} and t_{si} are the dielectric permittivity and thickness of silicon (or semiconductor material), respectively

ε_{ox} and t_{ox} are the dielectric permittivity and thickness of the gate dielectric

For a single-gate device, the parameter $a_g = 1$, whereas for a double gate, $a_g = 2$ [53]. Although, Equation 10.3 is derived to describe the conventional MOSFET behavior, it has been shown to be applicable for TFETs with appropriate use of the material parameters [51].

Using Equation 10.2 for $T(E)$, the drain current in a TFET device under high V_{gs} and V_{ds} is given by

$$I_{ds} = A \int_{E_c(C)}^{E_v(S)} \left[f_s(E) - f_d(E) \right] . T(E) N_D N_S . dE \tag{10.4}$$

where:

$f_s(E)$ and $f_d(E)$ are the source- and drain-side Fermi-Dirac distributions (Equation 2.3)

N_S and N_D are the corresponding density of states

A is the area of the device

For a *p-i-n* TFET band structure (Figure 10.3b), the integral ranges from E_{cc} (channel conduction band) to E_{vp} (source valence band) represent the range of energies over which tunneling takes place. Note that Equation 10.4 is similar to the conventional tunnel diode equation [48]. This is justified for TFETs since the channel quasi-Fermi level is in equilibrium with the drain Fermi level at high V_{gs} and V_{ds}.

One of the challenges in TFETs is to achieve high on current I_{on} (at $V_{gs} = V_{ds}$) that depends on $T(E)$ as given in Equation 10.4. From Equation 10.1, we notice that $T(E)$ can be increased by increasing the electric field F (which is

proportional to $(\Delta\Phi + E_g)/\lambda$) along the channel. Higher F can be achieved by different ways: (1) thinner t_{ox} or higher dielectric constant (high-k) gate oxide; (2) low E_g channel materials such as silicon germanium (SiGe) or Ge [54,55] or a thin layer of SiGe material between the source and the channel [56]; and (3) light-m_r* materials for source-channel junction. Low E_g channel materials increase I_{off} of TFETs and, therefore, require device optimization.

10.3.3 Device Characteristics

Let us consider a *p-i-n* structure for an nTFET device operation as shown in Figure 10.3. Figure 10.3a shows the off-state of the device with zero bias and on-state with $V_{gs} > 0$ and $V_{ds} > 0$. In the TFET off-state (broken line curve in Figure 10.3a), the conduction band edge of the channel is located above the valence band edge of the source, so interband tunneling is suppressed, leading to a very small off-state current (I_{off}) that is dictated by the reverse-biased *p-i-n* diode. The application of a $V_{gs} > 0$ pulls the energy bands down (solid line curve in Figure 10.3a). As soon as the channel conduction band is pulled below the source valence band, electrons from the source valence band can tunnel into the empty states of the channel conduction band. However, only the electrons within the *energy window* $\Delta\Phi$ can tunnel into the channel as shown in Figure 10.3a since the electrons from the high-energy ($E > kT$) tail of the Fermi distribution $f_s(E)$ are effectively cut off by the bandgap in the source as shown in Figure 10.4 and do not participate in the transport process [51].

To illustrate the interband tunneling from the degenerately doped *p*+ source of the *p-i-n* structure, only source-channel junction along with the Fermi

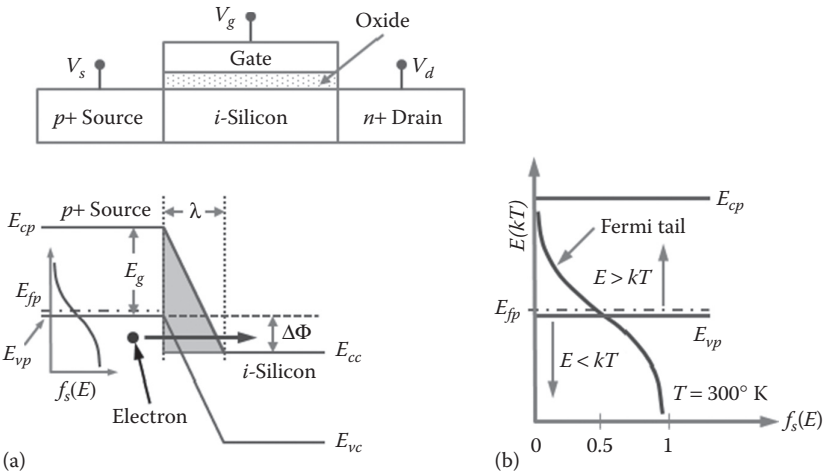

FIGURE 10.4
Energy band diagram of the source-channel *p-i-n* TFET device along the length of the device: (a) interband tunneling of carriers from the low energy ($E < kT$) regimes of the source Fermi distribution $f_s(E)$ and (b) expanded Fermi distribution of the source region at room temperature.

distribution function $f_s(E)$ of the source electrons is shown in Figure 10.4a, whereas Figure 10.4b shows the expanded $f_s(E)$ versus E distribution. Since the electrons with $E > kT$ of $f_s(E)$ are effectively filtered out from tunneling as shown in Figure 10.4, the current transport in TFETs is a *sub-kT* process. Thus, it can be considered that the electronic system is effectively *cooled down* acting as a conventional MOSFET at a lower temperature. Thus, in a TFET, primarily the cold carriers participate in the transport process, resulting in a subthreshold slope of less than 60 mV per decade. Note that in MOSFETs the subthreshold conduction is limited by Boltzmann distribution with higher-*kT* process (Chapters 4 and 5), thus limiting S to 60 mV per decade of current at room temperature.

The interband tunneling process in a TFET shown in Figure 10.4 is similar to a band-pass filter action wherein the high energy carriers are filtered out. This filtering function enables to achieve an S of below 60 mV per decade of current for TFETs. However, the channel conduction band E_{cc} can be pulled up or down by a small change in V_{gs}, that is, the tunneling width can be effectively changed by V_{gs} [38,49]. As a result, the value of S in a TFET is not a constant and depends on V_{gs} increasing with the increasing V_{gs}.

The above described physical mechanism of electron transport can be used to plot the transfer characteristics ($I_{ds} - V_{gs}$) of TFET devices. Again, let us consider a *p-i-n* TFET structure shown in Figure 10.5. As V_{gs} increases from $V_{gs} = 0$ to a certain trigger point, $V_{gs} = V_{off}$ at which the channel conduction band edge E_{cc} is pulled down to align with the source valence band edge, $E_{vp} \approx E_{fp}$; only the leakage current I_{off} of the *p-i-n* junction flows through the device as shown in Figure 10.5b. As V_{gs} increases above V_{off}, the overlap between E_{cc} and E_{vp} gradually increases triggering interband tunneling

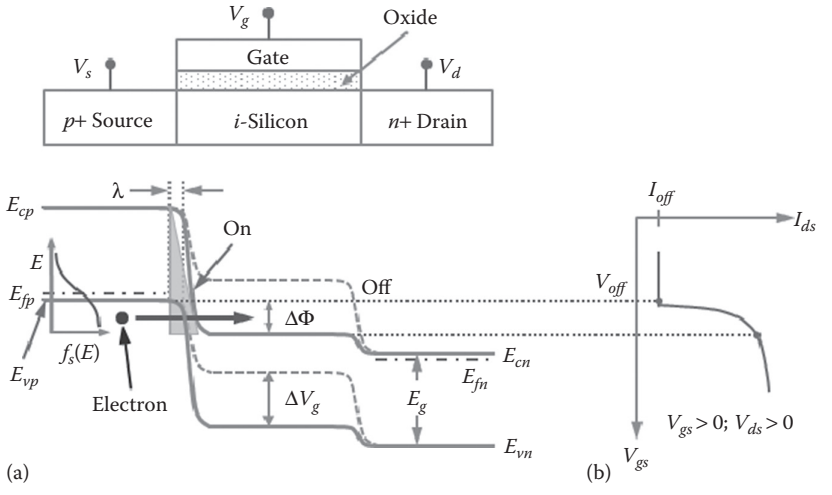

FIGURE 10.5
Current transport in a *p-i-n* TFET operation: (a) energy band diagram along the length of the *n*TFET in the on and off-states and (b) I_{ds} versus V_{gs} characteristics.

and the drain current I_{ds} increases. Since the *Fermi tail* of f_s(E) is cut off from the tunneling window, only the electrons with $E < kT$ contribute to current transport, resulting in a sharp increase in I_{ds} with *steep slope* as shown in Figure 10.5b. On further increase of V_{gs} to the target supply voltage, the tunneling window reaches the corresponding final width $\Delta\Phi$ and the sub-kT electrons tunnel from the source to the channel. The tunneled electrons are then transported to the drain by supply voltage, V_{ds}, generating a steady flow of I_{ds} in the device as shown in Figure 10.5b.

In TFETs, I_{off} is low due to the filtering of electrons from the high energy Fermi tail. The value can be further reduced by widening the tunneling barrier at drain junction [4,16,57].

10.3.4 Subthreshold Swing

In Chapter 4, we have shown that S for a MOSFET device is defined by $S = \left(d \log I_{ds} / dV_{gs}\right)^{-1}$ in units of mV per (decade I_{ds}). For the TFETs, the tunnel current can be described approximately by [48]

$$I_{ds} \cong aV_{eff} F \exp\left(-\frac{b}{F}\right) \tag{10.5}$$

where:

a and b are the coefficients that depend on the material properties of the tunnel junction and the cross-sectional area of the device

V_{eff} and F are the effective reverse bias and electric field at the tunnel junction, respectively

The coefficients a and b are given by [16,38]

$$\begin{aligned} a &= \frac{Aq^3\sqrt{2m_r^*}}{8\pi^2\hbar^2\sqrt{E_g}} \\ b &= \left(-\frac{4\sqrt{2m_r^* E_g^3}}{3q\hbar}\right) \end{aligned} \tag{10.6}$$

The derivative of I_{ds} expression given in Equation 10.5 can be used to obtain a general expression for S of TFETs [38] as

$$S = \frac{dV_{gs}}{d\left(\log I_{ds}\right)} = \ln(10)\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{gs}} + \frac{F+b}{F^2}\frac{dF}{dV_{gs}}\right]^{-1} \tag{10.7}$$

Equation 10.7 shows that S for TFETs depends on two terms that are not explicitly limited by kT/q unlike in MOSFETs. It is observed from Equation 10.7 that low S can be achieved by maximizing the two terms in the denominator. First of

all, if we optimize the device in such a way so that $dV_{eff}/dV_{gs} \approx 1$, then the first term in the denominator of Equation 10.7 is inversely related to V_{gs}. Under this condition, S will decrease with decreasing V_{gs}. This can be achieved by TFET gate engineering so that V_{gs} directly controls the tunnel junction bias or band overlap $\Delta\Phi$, that is, gate has strong electrostatic control. The efficient gate electrostatics can be realized using a thin high-k gate dielectric and an ultrathin body channel region. Secondly, S can also be minimized by maximizing the second term in the denominator of Equation 10.7. This occurs when the gate is placed to align the applied field with the internal field of the tunnel junction so that the gate field adds to the internal field to increase the tunneling probability.

From the discussion of Equation 10.7, it is clear that S is a function of V_{gs} in sharp contrast to the conventional MOSFETs. This means that $\log(I_{ds}) - V_{gs}$ plot in the subthreshold region is not a straight line and S does not have a unique value as shown in Figure 10.5b. The value of S is lowest at the lowest V_{gs}, and increases as V_{gs} increases. Due to the changing values of S along $I_{ds} - V_{gs}$ curve it is useful to clearly define it for device characterization.

Several definitions have been used for TFET S [16,57,58]. The most commonly used method is to take the tangential inverse slope of $I_{ds} - V_{gs}$ curve at the steepest part of the characteristic called the *point swing* as shown in Figure 10.6. Bhuwalka et al. [58] and Boucart and Ionescu [57] have defined subthreshold region by an average swing as shown in Figure 10.6 and is given by

$$S_{avg} = \frac{V_{th} - V_{off}}{\log\left(I_{th} / I_{off}\right)} \tag{10.8}$$

where:

V_{th} is the threshold voltage

V_{off} is the voltage below V_{th} at which the drain current I_{off} is minimum

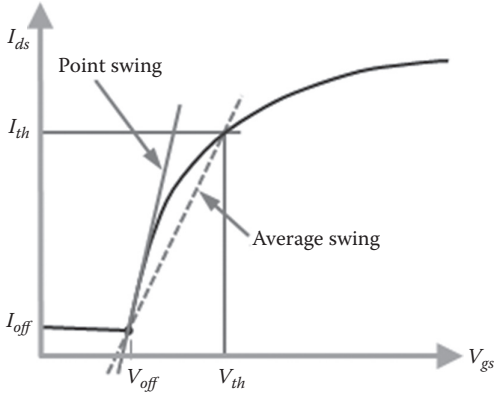

FIGURE 10.6
Subthreshold swing defined as a point swing is obtained at the steepest point of the $I_{ds} - V_{gs}$ curve and an average swing is defined as the average from turn-on to threshold voltage.

To use S_{avg}, it is important to use the appropriate value of V_{th} for accurate modeling of TFET device and circuit performance [59,60].

Another definition for S has been used to account for the voltage scaling attribute of low-S devices [16]. In this method, V_{th} is defined at $V_{th} = V_{dd}/2$; then the corresponding current $I_{th} = I_{ds}(V_{gs} = V_{dd}/2)$, where V_{dd} is the target supply voltage. In this definition, it is assumed that $V_{off} = 0$ so that $I_{off} = I_{ds}$ at $V_{gs} = 0$. Then the effective S is given by

$$S = \frac{V_{dd}}{2\log\left(I_{th} - I_{off}\right)} \tag{10.9}$$

The basic DC performance of TFETs is characterized by specifying I_{on}, V_{dd}, and S. The TFET devices offer current gain, voltage gain, and input–output isolation, and have the basic attributes required for a complementary logic technology in a Boolean logic architecture. The current saturates with the saturation set by the source injection. Due to the ambipolarity, *the nTFET and pTFET devices can be designed to produce equal currents by using the same tunnel junction, that is, equal gate widths offer equal* I_{on} *and symmetric layouts are possible.* Since the Fermi tail is cut off by the bandgap, the S is not limited to 60 mV per decade and I_{off} can be significantly lower than that of MOSFETs.

The *scaling rule* for TFETs is different from that of the MOSFETs in which many parameters must be scaled simultaneously to keep the same electric field throughout the device [61]. In a TFET, the high electric fields exist only at the junctions. The current is determined by λ so that the device characteristics is independent of the length L of the intrinsic channel region for $L > L_{crit}$ (~20 nm for silicon TFETs) [61,62]. For $L > L_{crit}$ the *p-i-n* leakage becomes predominant. Thus, TFETs have a great potential to be devices for beyond-CMOS technology.

10.4 TFET Design Considerations

Typically, all-silicon TFET devices offer the lowest I_{off} and S, however, very low I_{on}; for example, for an nTFET $I_{off} < 100$ fA μm^{-1}, $S < 44$ mV per decade of I_{ds}, and $I_{on} < 0.1$ μA μm^{-1} [63]. Thus, the primary objective of TFET optimization is to achieve the highest possible I_{on} along with the lowest S over many orders of magnitude of I_{ds} and lowest possible I_{off}. To outperform CMOS transistors, the target parameters for TFETs are: I_{on} in the range of hundreds of mA; $S_{avg} << 60$ mV per decade for five decades of current at $T = 300$ K; $I_{on}/I_{off} > 1 \times 10^5$; and $V_{dd} < 0.5$ V. Since S decreases with V_{gs} [63], TFETs are targeted and optimized for low-voltage operation.

Equations 10.4 and 10.7 show that the tunneling current and S depend on the tunneling probability $T(E)$ of the source-channel junction. Therefore, in

order to realize a high I_{on} and a steep slope, $T(E)$ of the source tunneling barrier should be close to unity for a small change in V_g. From Equation 10.2, it is found that $T(E)$ depends on λ, E_g, and m^*. Thus, high barrier transparency (i.e., $T(E) \sim 1$) can be achieved by minimizing E_g, m^*, and λ. Now, E_g and m^* depend on the materials of the TFET device structure, whereas λ depends on the device architecture including geometry, doping profiles, and gate capacitance [16,64,65]. Therefore, the performance of TFETs can be improved by *device architecture* and *energy band engineering*, that is, using low-E_g and low-m_r^* materials for forming the tunnel junction.

One way to improve TFET device performance by device architecture is to minimize λ. A small λ offers a strong modulation of the channel energy bands by the gate. This small value of λ, can be achieved by using a high-κ gate dielectric [57] with manufacturable ultrathin equivalent oxide thickness, ultrathin body [49,64], and degenerately doped abrupt doping profile of the tunnel junction [65,66]. Another technique to improve I_{on} by device architecture is to maximize the gate modulation of the tunneling barrier width by an appropriate alignment of the tunneling path with the direction of the electric field modulated by the gate. By overlapping the gate with the tunneling region, or designing a source region covered with an epitaxial *i*-channel layer under the top gate, I_{on} can be improved by a factor of more than 10 along with a low S_{avg} [19,67–69].

In addition to optimizing TFET device structure to improve device performance, the improvement in I_{on} and S can be achieved by band engineering, that is, use low-E_g and low-effective mass m_r^* materials to increase interband tunneling. This is achieved by heterostructure TFETs with different source materials with respect to the channel and drain, creating *staggered bandgap* structures. Device optimization should apply to both *n*- and *p*-type TFETs simultaneously, to offer a complementary TFET (CTFET) technology for logic circuits.

In heterostructure TFETs, a low E_g source material is used to reduce the width of the energy barrier at the source junction in the on-state, whereas a large E_g drain material is used to create the largest possible width of the energy barrier at the drain junction in the off-state to keep a low I_{off}. The device performance depends on the band's lineup with each other at the heterojunction [5,70,71]. The reported data show that a combination of steep S and high I_{on} can be achieved with moderate doping and a staggered band lineup [72,73].

In a reported theoretical study on staggered bandgap structures, the CTFET devices have been optimized by changing the source material from silicon to low E_g materials Ge and InAs for nTFETs and pTFETs, respectively [63]. The numerical simulation data on 50 nm silicon channel length of Ge-source nTFETs and InAs-source pTFETs show an improvement of I_{on} by a factor of 480 and 162, respectively, at $V_{ds} = V_{gs} = 1$ V over the identically designed all-silicon TFETs. For example, the simulated Ge-source nTFETs and InAs-source pTFETs show I_{on} of 244 μA μm^{-1} and 83 mA μm^{-1}, respectively, with much lower I_{on}/I_{off} than the comparable CMOS devices and $S \sim 60$ mV per decade of I_{ds} [63]. Thus, the heterostructure TFETs have a great potential to meet the target performance objectives of CTFET technology operating at $V_{dd} << 0.5$ V [70,71,74,75].

As discussed earlier, though all-silicon TFETs offer very low I_{on} than the conventional MOSFETs, they have shown lowest I_{off} with a small S. The current drivability in all-silicon TFETs can be improved by using high-k gate dielectric, abrupt doping profile at the tunnel junction, a thinner body, higher source doping, a double gate, a gate oxide aligned with the intrinsic region, and a shorter i-region (and gate length) [41,76–78]. A recent study on sub-60 nm all-silicon TFET devices shows $I_{on} \sim 100\ \mu A\ \mu m^{-1}$ [79].

In order to improve I_{on} by low m_r^* materials tunneling junction, III–V semiconductor-based TFETs are used in energy band engineering. The group III–V materials provide small tunneling mass as well as different band-edge alignments. Early experimental data on homojunction InGaAs p-i-n TFETs show higher I_{on} at a lower V_{gs} than all-silicon TFETs. [80,81]. Though the reported S is high, it is still above the thermal limit of MOSFETs [82]. The effective E_g can be further reduced by using III–V material-based hetrostructures with enhanced device performance compared to the homojunctions [70–72,83–85]. In this context, the tunneling barrier can be reduced by using InAs and GaAsSb for the source with AlGaSb and InGaAs for the channel.

The nanowire TFETs show a great potential for CTFET technology to mitigate the risk of lattice mismatch and defective material growth in InAs source and silicon channel pTFETs [70,86,87]. Experimental data on InAs-silicon Esaki tunnel diodes show high tunneling current and well-defined abrupt silicon-InAs heterojunction [87,88]. The vertical nanowire TFETs with *gate-all-around* device architecture offers an optimal geometry for minimizing λ and best electrostatic control [89]. The fabricated vertical n-i-p InAs–Si–Si nanowire heterojunction TFETs with InAs as a low E_g source [90] show a great promise for nanowire CTFETs.

CNT and graphene nanoribbons (GNR) are excellent choices for TFETs in terms of device architecture and energy band engineering due to the light m_r^* of their charge carriers, low and direct bandgap, and excellent electrostatic control of the gate over the ultrathin body channel. The ongoing theoretical and limited experimental studies show a great potential for carbon-based TFETs [6,51,91–93]. However, for the practical implementation of GNR-TFETs, a number of issues must be addressed including the influence of line edge roughness on the bandgap and transport properties and their effects on TFET device performance [94,95].

10.5 Compact TFET Models

From the discussions in Sections 10.3 and 10.4, it is found that CTFET technology is a viable candidate for beyond-CMOS technology due to its steep-slope complementary devices with $S < 60$ mV per decade at low V_{gs}, enabling supply voltage scaling nearing 0.1 V [67]. For concurrent development of

CTFET technology and TFET-based IC chips, there has been a tremendous interest in TFET-based exploratory novel circuit design [96,97]. However, due to the lack of available compact TFET models for circuit CAD, lookup tables or behavioral models are used for circuit analysis [98,99]. Recently, a number of current and capacitance models for TFET devices have been reported [100–107]. These reports include device models for multigate TFETs [100,104,106,107] as well as for heterojunction nanowire TFETs. Recently, Zhang et al. [103,107] reported a workable compact model and coded it with Verilog-A for public use. However, a general-purpose compact TFET model for circuit simulation is not yet available. Therefore, the underlying physical concepts to develop compact TFET models are presented in this section.

10.5.1 Threshold Voltage Model

Let us consider a *p-i-n* TFET device structure on an SOI substrate with heavily doped *p*+ source, intrinsic channel, and *n*+ drain regions as shown in Figure 10.7a. The energy band diagram at the source-channel tunnel junction of the device in the on-state is shown in Figure 10.7b. Since the *p*+ source region is degenerately doped, the Fermi level E_{fp} of the source-side tunneling junction is assumed at or below the valence band E_{vp} as shown in Figure 10.7b.

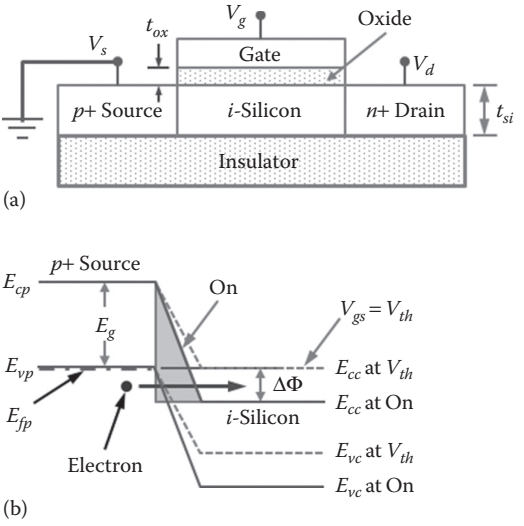

FIGURE 10.7
Threshold voltage modeling for TFETs: (a) 2D cross section of an ideal single gate *p–i–n* TFET device structure with a *p*+ source, an *i*-silicon channel, and an *n*+ drain regions on an SOI substrate; t_{ox} and t_{si} are the gate oxide thickness and body thickness, respectively; V_s, V_g, and V_d are the source, gate, and drain voltages, respectively and (b) energy band diagram of the source-channel junction along the length of the device at the threshold condition (broken lines) and on-state (solid lines).

Now, we define the threshold voltage V_{th} of TFETs as the gate voltage V_{gs} at which the interband tunneling sets in at the source-channel junction [106]. In other words, V_{th} is the value of the V_{gs} at which the Fermi energy level E_{fp} in the p+ source region aligns with the conduction band energy level E_{cc} in the channel as shown in Figure 10.7b. Considering the i-channel region as a conventional *long channel* MOSFET device, an inversion layer is formed at $V_{gs} = V_{th0}$, where V_{th0} is the long channel threshold voltage of the i-channel MOSFET is given by (Equation 4.13)

$$V_{th0} = V_{fb} + 2\phi_B + \gamma\sqrt{2\phi_B} \tag{10.10}$$

where:
$\gamma = \sqrt{2K_{si}\varepsilon_0 q N_b}\,/C_{ox}$ and is defined in Equation 4.11
V_{fb} is the flat band voltage
C_{ox} is the oxide capacitance
N_b is the carrier concentration in the i-channel region
$\phi_B = v_{kT} \ln\left(N_b/n_i\right)$ is the bulk potential defined in Equation 3.35

For an nTFET device with p+ source (electrons are minority carriers), the injected number of minority carrier electrons from the source is insufficient to maintain the channel inversion layer. Therefore, the MOSFET device is in the off-state at $V_{gs} = V_{th0}$. If we further increase the V_{gs} beyond V_{th0}, the channel-side conduction band E_{cc} is pulled below the source-side valence band E_{vp} and the tunneling window $\Delta\Phi$ is opened as shown in Figure 10.7b, causing current flow.

We know that the Fermi level of the i-channel region is at the center of the bandgap ($E_g/2$), and for the degenerately doped p+ source region, we can assume $E_{vp} \approx E_{fs}$. Then at $V_{gs} = V_{th}$ when the channel E_{cc} is aligned with source $E_{vp} = E_{fp}$, the energy required to pull down E_{cc} from $V_{gs} = 0$ to $V_{gs} = V_{th}$ is about $E_g/2$. Therefore, the simplified expression for the threshold voltage of an nTFET can be written as

$$V_{thn} = V_{fb} + 2\phi_B + \gamma\sqrt{2\phi_B} + \frac{E_g}{2q} \tag{10.11}$$

The same expression can be used for n-i-p structure with appropriate sign convention for the i-region pMOSFET biasing condition. An expression for V_{th} for short channel TFET devices has also been reported to model V_{th} roll-off [106]. However, experimental data show that the TFET device characteristics are independent of the length L of the intrinsic channel region for $L > L_{crit}$ (~20 nm for silicon TFETs) [61,62]. Therefore, Equation 10.11 is valid for threshold voltage modeling in most TFET devices. However, for $L < L_{crit}$ the p-i-n diode leakage current influences V_{th}, and therefore, appropriate channel length dependence in V_{th} must be used to account for the leakage currents in the short channel devices with $L < 20$ nm.

10.5.2 Drain Current Model

In order to develop a TFET I_{ds} model, we consider a TFET as a combination of an ideal *tunnel diode* in series with a *drain*-MOSFET device as shown in Figure 10.8. Therefore, the *interband tunneling* and *drift-diffusion* transport mechanisms must be considered in modeling I_{ds} for TFETs. Numerical simulation results show that the relatively large channel resistance due to the drift-diffusion causes additional potential drop and stronger lateral electric field in the channel, resulting in mobility (μ) and I_{on} degradation [107]. Thus, the modeling of channel transport in TFETs is important along with the interband tunneling. However, since the interband tunneling and channel transport mechanisms are coupled, the modeling of TFETs with two coupled transports increases the complexity of device modeling. Therefore, for the simplicity of compact TFET modeling, two separate I_{ds} models can be developed: (1) an ideal I_{ds} equation considering only the tunneling probability of the junction without the channel transport and (2) a second I_{ds} equation considering only the drift-diffusion transport in the channel-MOSFET. However, only the ideal current model can be accurately used for low-current drivability TFETs, whereas for high-current drivability devices, both the ideal and the channel transport I_{ds} equations must be used for accurate device analysis in circuit CAD.

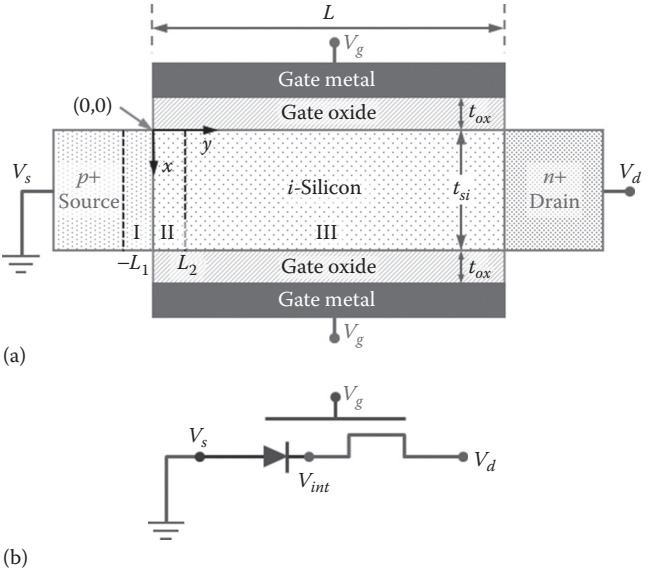

FIGURE 10.8
Schematics of a DG-nTFET for drain current modeling: (a) device structure with channel division in regions I, II, and III for current transports and (b) equivalent circuit representation of an ideal tunnel diode. L_1, L_2 are the length of the region I and II, respectively; V_{int} is the internal node; L is the channel length of the device; $V_{int} = V_{ds}$ for ideal current model and $V_{int} < V_{ds}$ for channel transport.

10.5.2.1 Ideal Drain Current Model

In the present state-of-the-art silicon TFETs with low-drive current, the channel transport is insignificant due to the comparatively large tunnel-junction resistance. Thus, for the simplicity of modeling TFETs, the channel transport can be neglected to develop an ideal TFET model by zero field approximation along the channel [105,107].

Let us consider a DG-nTFET shown in Figure 10.8a to illustrate the compact modeling techniques in TFETs. In order to derive I_{ds} model for DG-TFETs, the entire device is divided into three regions as shown in Figure 10.8a: the source junction region (I), channel junction region (II), and the channel transport region (III) [105,107]. With the zero field approximation, the quasi-Fermi potential at the boundary of regions II and III is equal to V_{ds}, and therefore, the channel transports can be neglected to develop an ideal I_{ds} model. Though a gradient of the electrostatic potential exists in region III, the quasi-Fermi potential at the *internal node* V_{int} is smaller than V_{ds}. In principle, V_{int} can be determined by ensuring current continuity between the quantum tunneling current and the drift-diffusion current.

In order to develop an ideal I_{ds} model without the channel transport, electrostatic potentials in TFETs are solved to derive the expression for tunneling current. The charges in region III are considered to model the exponential dependence of the output characteristics and the terminal capacitance properties of TFETs [105,107]. The potential solutions together with the zero electric field approximation in region III form the boundary conditions for region II.

In order to include the possible channel charge degenerations, the surface potential in region III is obtained by solving 1D Poisson's equation using Fermi-Dirac statistics [108, 109] given by

$$\frac{d^2u}{dx^2} = \left(\frac{1}{2}\frac{2q^2n_i}{\varepsilon_{si}kT}\right)\frac{F_{1/2}\left(u - v_{ch}(y) - E_g/2kT\right)}{F_{1/2}\left(-E_g/2kT\right)} \tag{10.12}$$

where:

q is the electron charge
u is the normalized potential by v_{kT}
v_{ch}(y) is the normalized quasi-Fermi channel potential at any point y along the channel
n_i is the intrinsic carrier concentration
E_g is the material bandgap
ε_{si} is the dielectric constant of region III
$F_{1/2}$ is the Fermi integral of the order 1/2

By integrating once, the vertical electric field at the surface is obtained as a function of the normalized surface potential u_s and center potential u_0, gate dielectric thickness t_{ox}, gate capacitance $C_{ox} = \varepsilon_{ox}/t_{ox}$, and $F_{3/2}$ the Fermi integral of the order 3/2

$$\left.\frac{du}{dx}\right|_{x=0} = \sqrt{\frac{2q^2 n_i}{\varepsilon_{si} kT}} \left[\frac{2F_{3/2}\left(u - v_{ch}(y) - E_g / 2kT\right)\Big|_{u0}^{u_s}}{3F_{1/2}\left(-E_g / 2kT\right)} \right] \tag{10.13}$$

The gate control equation is derived using Equation 10.13 as

$$v_g - v_{fb} - u_s = \frac{\varepsilon_{si}}{C_{ox}} \left.\frac{du}{dx}\right|_{x=0} \tag{10.14}$$

The relationship between the surface potential (u_s) and center potential (u_0) in region III required to solve Equation 10.14 is obtained by numerical device simulation using surface potentials of DG-MOSFET [110] as the initial guess for u_0 [105,107]. With the surface potential ($\phi_{s3}(y)$) solution at any point y along the channel in region III, the expressions for the electrostatic potentials $\phi_{s1}(y)$ and $\phi_{s2}(y)$ at any point y in regions I and II, respectively, are derived. It is shown that $\phi_{s1}(y)$ is a function of the effective source doping N_{seff} and L_1; $\phi_{s2}(y)$ depends on V_{gs}, work function difference between the gate and p-doped source $V_{fbs,}$ the work function difference between the gate and undoped channel V_{fbc}, built-in potential $V_{bi,s}$ of the source-channel junction, natural length of region II λ_{II}, and L_2; and $\phi_{s3}(y)$ depends on $V_{bi,s}$ and u_s [107].

The lenghts L_1 and L_2 are determined by matching the boundary conditions of regions I and II [105,107]. A tunneling distance W_T for any given energy level in the interband tunneling window (overlap between E_{cc} in region II and E_{vp} in region I) is found by deriving the classical turning points x_c in region II and x_v in region I from the derived surface potential profiles. Among all the tunneling paths, there exists a smallest tunneling distance $W_{T,min}$ with the largest tunneling probability, which will contribute to the peak generation rate of electrons at x_c and holes at x_v [111]. For interband tunneling in nTFETs at a certain potential level ϕ_I, W_T is found from the turning point x_c in region II (channel conduction band) and x_v in region I (source valence band). Then the potential level $\phi_{I,min}$ corresponding to the maximum generation rate is determined and is given by [107]

$$\phi_{I,min} = \left(V_{gs} - V_{fbs}\right) + \frac{qN_{seff}\lambda_{II}^2}{\varepsilon_{si}} - \sqrt{\left(\frac{qN_{seff}\lambda_{II}^2}{\varepsilon_{si}}\right)^2 + \left(V_{gs} - V_{fbb} - \phi_{dg}\right)^2 + \frac{qN_{seff}\lambda_{II}^2}{\varepsilon_{si}\left[V_{gs} - V_{fbc} - \left(E_g/q\right)\right]}} \tag{10.15}$$

and the minimum tunneling distance is [107]

$$W_{T,min} = L_2 - \lambda_{II} \cosh^{-1}\left(\frac{V_{gs} - V_{fbs} - \phi_{I,min}}{V_{gs} - V_{fbc} - \phi_{dg}}\right) - \sqrt{\frac{2\varepsilon_{si}}{qN_{seff}}\left(\phi_I - \frac{E_g}{q}\right)} + L_1 \tag{10.16}$$

where:

$\phi_{dg} = u_s v_{kT}$ is the surface potential of the channel region (III) DG-MOSFET

Now, from Kane's BTBT model [112], the expression for the tunneling probability is given by

$$G_T = A\frac{F^2}{\sqrt{E_g}}\exp\left(-B\frac{E_g^{3/2}}{|F|}\right) \tag{10.17}$$

where the maximum electric field across the tunneling junction is given by

$$|F| = \frac{E_g}{q}\frac{1}{W_{T,min}} \tag{10.18}$$

The peak electron generation rate is calculated by substituting Equation 10.18 into Equation 10.17 to obtain

$$G_{T,max} = A.\frac{E_g^{3/2}}{q^2}\frac{1}{W_{T,min}^2}\exp\left(-qB\sqrt{E_g}W_{T,min}\right) \tag{10.19}$$

where:

A and B are two parameters of the Kane's model [48,112]

Again, from Kane's model, we know that the generation rate of electrons decays exponentially with increasing tunneling distances. Therefore, the total tunneling current is obtained by integrating Equation 10.17 over the tunneling space $d\Omega_{tun}$ and is given by

$$I_{ds} = q\int G_T d\Omega_{tun} \tag{10.20}$$

To derive a closed-form solution of the above spatial integral of generation rates, a linearly changing tunnel distance is assumed [103]. Again, by assuming that the tunneling current is uniform across the channel thickness (a valid approximation for thin body DG-TFETs), the final I_{ds} expression can be shown as

$$I_{ds} = G_{T,max}.\left(\frac{2W.t_{si}}{B\sqrt{E_g}}\right) \tag{10.21}$$

where:

W is the channel width of TFETs

Equation 10.21 represents a simplified I_{ds} model for TFETs. However, it yields an unphysical nonzero current even at equilibrium states of TFETs.

Therefore, for physically acceptable simulation results, a correction factor is introduced as given by [107]

$$f_{fermi} = 2\left[\frac{1}{2} - \frac{1}{1+\exp\left(V_{ds}/f_n.v_{kT}\right)}\right] \tag{10.22}$$

where:
f_n is an empirical fitting parameter

Finally, the ideal I_{ds} model is given by

$$I_{ds} = G_{T,max}.\left(\frac{2W.t_{si}}{B\sqrt{E_g}}\right).f_{fermi} \tag{10.23}$$

Equation 10.23 is the ideal I_{ds} model for TFETs with $G_{T,max}$ and f_{fermi} given by Equations 10.19 and 10.22, respectively. The ideal I_{ds} is characterized by three model parameters, A, B, and f_n. When the potential $\phi_{I,min}$ given by Equation 10.15 is larger than the bandgap potential, the interband tunneling window is created and a tunneling current is observed. It can be shown that the bias-dependent S in TFETs is mainly determined by the V_{gs}-dependent tunneling distance given by Equation 10.16. The ideal I_{ds} model is valid in the operation regions with large V_{gs} due to the inclusion of channel charge in the surface potential model. Note that the I_{ds} expression in Equation 10.23 does not include channel length L. This is justified for $L > 20$ nm since the leakage current dominates in TFET devices with $L < 20$ nm as discussed earlier.

10.5.2.2 Modeling the Channel Transports Using Drain MOSFET

In contrast to low current drivability all-silicon TFETs (e.g., << 100 μA μm^{-1}), the III–V compound-based TFETs and heterojunction TFETs offer significantly high drive current (e.g., hundreds of μA μm^{-1}) [114]. In these devices, the resistance of the tunneling junction is comparable to the resistance of the channel region, and therefore, the drift-diffusion channel transport directly affects the device characteristics. Thus, for accurate modeling of high performance TFET devices, it is necessary to include the effect of channel transport in compact TFET modeling.

In order to model TFETs with coupled transports, a TFET device can be represented by an ideal TFET in series with a drift-diffusion MOSFET at the drain side of the device as shown in Figure 10.9. In this representation, a TFET includes two components that are coupled by the internal node with potential V_{int}. Thus, $V_{int} = V_d$ for the ideal TFET and $V_{int} = V_s$ for the drift-diffusion MOSFET of the DG-TFET device. At any applied biasing condition, V_{gs} is shared by both devices; however, the quasi-Fermi level V_{int} and/or electrostatic potential at the internal node is determined by setting the tunneling

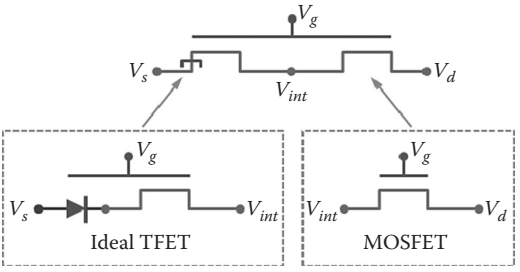

FIGURE 10.9
Schematic representation of a DG-TFET with coupled transports: The device is modeled by an ideal TFET in series with a MOSFET at the drain end of the device for modeling the channel transport; the internal node V_{int} is common to both TFET and the MOSFET and determined by current continuity at the node.

and drift-diffusion currents at the same value. From the discussion in the previous section we know that the tunneling current is a function of the surface potential in TFET region III and depends on its drain voltage ($V_d = V_{int}$) as shown in Figure 10.9. Similarly, the drift-diffusion current in a MOSFET depends on its source voltage ($V_s = V_{int}$). Thus, the current continuity at V_{int} can be achieved by iterations in a circuit CAD tool (e.g., SPICE).

The zero field approximation at V_{int} leading to $V_{int} = V_d$ simplifies the derivation of I_{ds} model as discussed in Section 10.5.2.1. However, $V_{int} = V_d$ assumption is physically invalid for modeling I_{ds} if the channel transport is considered. In this case, V_{int} is not uniquely defined since both the potential and the electric field are floating and a simple solution for Poisson's equation does not exist. Therefore, a *virtual node* method is used for modeling I_{ds} [107]. In this technique, a zero field is assumed to be still valid at V_{int} similar to the boundary condition used for the ideal TFET and a discontinuity in the lateral field is created keeping potential or quasi-Fermi level constant at the node. With this virtual node method, Equation 10.23 can be used as the component of the total I_{ds} due to the ideal TFET device shown in Figure 10.9 with its drain voltage as V_{di}. Again, V_{di} is a variable and is determined by current continuity at the internal node.

For any given biasing condition, the applied voltages V_g, V_s, and V_d and the pre-assumed quasi-Fermi potential at the internal node V_{di}, the potentials at the internal node ϕ_{int} and at the drain side ϕ_d are both derived from Equations 10.12 to 10.14 with the quasi-Fermi levels as V_{di} and V_d. Note that for the MOSFET element of the device ϕ_{int} and V_{di} are the surface potential and bias at the virtual source terminal, respectively. Then the electron charge densities at the source and drain ends of the MOSFET device are given by

$$\begin{aligned} q_{int} &= C_{ox}\left(V_{gs} - \phi_{int}\right) \\ q_d &= C_{ox}\left(V_{gs} - \phi_d\right) \end{aligned} \tag{10.24}$$

Finally, the MOSFET current is simply calculated by summarizing the drift and diffusion current components and is given by

$$I_{ds,MOS} = 2\mu \frac{W}{L_{dg}} \left[v_{kT} \left(q_{int} - q_d \right) \right] + \frac{q_{int}^2 - q_d^2}{2C_{ox}} \tag{10.25}$$

where:

μ is the electron mobility

L_{dg} is the effective channel length of the MOSFET given by

$$L_{dg} = L_g - L_2 \tag{10.26}$$

L_{dg} depends on the external bias through L_2 [105,107].

Equations 10.23 and 10.25 constitute the total drain current in a DG-TFET to model both the interband tunneling and drift-diffusion transport. The values of quasi-Fermi level V_{di} and the potential at the internal node ϕ_{int} are determined iteratively to set the ideal TFET I_{ds} in Equation 10.23 equal to the drift-diffusion I_{ds} in Equation 10.25. However, a correction factor is needed for accurate modeling of channel transport in TFETs [107].

The complete set of model parameters including channel transport models in TFETs is given by {μ, *A*, *B*, f_n}. A simple parameter extraction routine is used to extract the model parameters. The parameters, *A* and *B*, are optimized to fit the *I*–*V* characteristics in the subthreshold region of TFETs by setting a large value for μ. Then, μ is optimized to fit the *I*–*V* characteristics in the high V_{gs} region. The parameters *A* and μ determine the transition region of the transfer characteristics of TFET devices. Finally, *A* and *B* are reoptimized to fit the transconductance [107].

Though the drain-MOSFET method accurately models the effects of channel transport on TFET current and terminal charge characteristics, it requires additional iterative computations in circuit CAD and, therefore, is computationally inefficient compared to the ideal I_{ds} model described in Section 10.5.2.1. Since the drift-diffusion channel transport does not affect the terminal charge significantly, a computationally efficient simpler method can be used for modeling TFETs in circuit CAD as described in the following section [107].

10.5.2.3 Modeling the Channel Transports Using Source Resistance

The channel transport in TFETs can be modeled effectively by adding a source resistance (R_s) to the ideal TFET model as shown in Figure 10.10 [107]. R_s reduces both V_{gs} and V_{ds} simultaneously, due to the similarity in the exponential gate and drain control over the tunneling current and, therefore, effectively models the effects of channel transport in reducing the voltage drop over the tunnel junction. Since both V_{gs} and V_{ds} are reduced simultaneously, the saturation drain voltage, V_{dsat}, of TFETs does not change. R_s is, purely, a fitting parameter and is extracted along with the model parameters

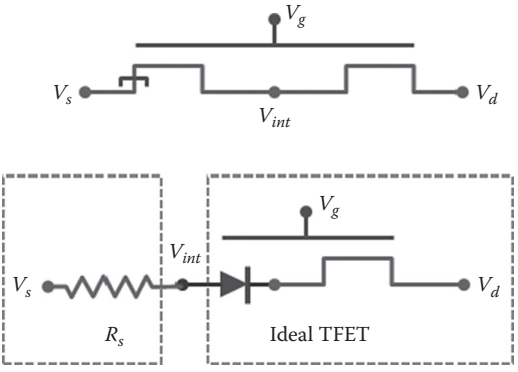

FIGURE 10.10
Schematic representation of a DG-TFET for coupled transports: The device is modeled by an ideal TFET in series with a source resistance, Rs; Rs is a fitting parameter to match the measured I–V characteristics of TFETs.

A, B, and f_n of the ideal I_{ds} model. Obviously, the accuracy of the method depends on the extraction of R_s.

The reported data show that the source-resistance method is computationally efficient compared to the drain-MOSFET method and provides acceptable simulation results for TFET devices [107].

10.6 Summary

This chapter introduces the emerging devices as the potential alternatives for beyond-CMOS devices. Among the emerging devices such as tunneling, impact ionization, ferroelectric dielectrics, and mechanical gate FETs, TFETs have recently been the subject of numerous investigations for a potential alternative to MOSFETs. Thus, in this chapter the fundamentals of TFETs are overviewed. First of all, the basic features of TFETs are discussed. Then the basic operating principle is presented to understand the basic mechanism of TFETs as the steep slope devices with S much lower than that of MOSFETs. Finally, the emerging compact TFET modeling techniques are presented.

Exercises

10.1 Consider an ideal all-silicon *n-i-p* TFET structure with *n*+ source, *intrinsic*-silicon channel, and *p*+ drain regions to explain the basic principle of pTFET operation.

a. Draw the energy band diagrams with reference to the ideal device structure for biasing conditions
   i. $V_{gs} = 0 = V_{ds}$
   ii. $V_{gs} < 0$, $V_{ds} = 0$
   iii. $V_{gs} < 0$, $V_{ds} < 0$
   Clearly label all relevant parameters;
b. Explain the operation of a pTFET device with reference to the band diagram for each of the biasing conditions in part (a).

10.2 Consider the ideal all-silicon *n-i-p* TFET structure described in exercise 10.1 to explain the interband tunneling mechanism in *p*TFET devices.

a. Draw the energy band diagrams in the off-state with $V_{gs} = 0 = V_{ds}$ and on-state with biasing condition $V_{gs} < 0$ and $V_{ds} < 0$ so that a tunneling window is created by overlapping bands at the source-channel junction. Clearly label all relevant parameters.
b. Explain the tunneling mechanism at the junction with reference to the band diagrams in part (a).
c. Sketch the transfer characteristics ($I_{ds} - V_{gs}$) of the device under the biasing conditions in part (a) with reference to the band diagrams in part (a) (similar to Figure 10.3); explain your plots.

10.3 Complete the mathematical steps to derive Equation 10.7 for subthreshold swing in TFET devices. Identify the critical parameters that can be used to optimize device performance for TFETs. Explain with examples how these parameters can be used to improve current drivability in TFETs.

10.4 Compare the carrier transport mechanisms in TFETs and MOSFETs. Explain why TFETs can offer lower S (<60 mV per decade of drain current at room temperature) than that of MOSFETs using carrier injection process and carrier statistics in each device.

10.5 Consider an all silicon *n-i-p* TFET device. Draw the energy band diagrams.

a. At the onset of threshold voltage.
b. In the on-state.

   Clearly label all relevant parameters and explain the device operation.

10.6 The carrier transport and drive current in TFETs are independent of gate length, L (i.e., length of the channel region). However, for $L < 20$ nm, the *p-i-n* diode leakage current dominates increasing the overall current flow in the device. Describe a simple technique to model this additional current in short channel TFETs for circuit CAD.

10.7 Write the complete coupled equations discussed in Section 10.5.2.2 that you would solve to model channel transport in TFETs. What are the compact model parameters and describe the methodology to extract these parameters to build compact TFET model for circuit CAD.

10.8 Are TFETs viable devices for beyond-CMOS technology? Explain your answer with examples.