Chapter

9

Models for Analog Design

In this chapter we develop models for analog design using the MOSFET. We'll break this discussion up into three sections. The first section covers long-channel MOSFET models with the assumption that the MOSFET follows the "square-law" equations derived in Ch. 6. In the second section we discuss models using modern MOSFETs with short-channel lengths (< 1 μm). Models for these short-channel MOSFETs are developed with graphs showing device characteristics, (e.g., output resistance, transconductance, etc.). Finally, at the end of the chapter, we introduce MOSFET noise modeling.

9.1 Long-Channel MOSFETs

When we do analog design we often say things like "the MOSFET looks like a current source when operating in the saturation region" or "it looks like a resistor." Before going too far, let's make sure that we understand these statements. Examine the current-voltage (IV) plot in Fig. 9.1. In this figure we've plotted the (DC) current-voltage characteristics of a resistor, a current source, and a voltage source. Often the controlling parameter in a semiconductor device is a voltage. The controlled parameter is then the device's output current (and this is why current is on the y-axis and voltage is on the x-axis in an IV plot).

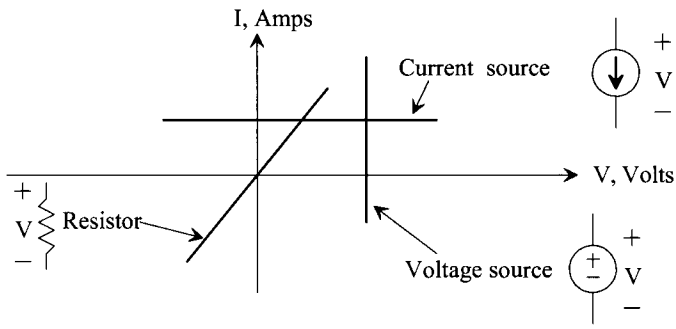


Figure 9.1 Current-voltage (IV) plots for various electrical components.

The voltage across the voltage source, for example, doesn't vary with changes in current running through it. The voltage across the resistor is linearly related to the current flowing through the resistor (Ohm's law). An important thing to note is that resistance can be calculated by taking the reciprocal of the IV plot slope. (So the voltage source in this figure has zero resistance; the current source, infinite resistance.) Also note that the x-axis corresponds to plotting the IV characteristics of an open circuit (no current with changes in voltage). The y-axis corresponds to a short (no changes in the voltage across a wire [a short], with changing current).

Example 9.1
Plot the IV characteristics for the circuit seen in Fig. 9.2.

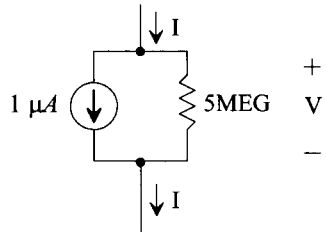


Figure 9.2 Circuit for Ex. 9.1.

Figure 9.3a shows the IV curves for each component of the circuit where we use a single quadrant of the IV plotting plane. The slope of the resistor is 200 $nA/1\ V$. The resistance value is the reciprocal of this slope (5MEG). The combined IV curve is seen in Fig. 9.3b. ■

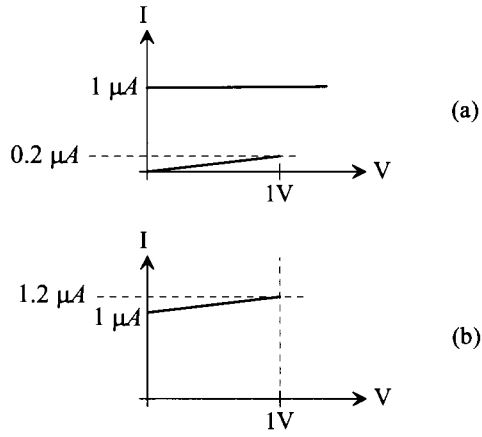


Figure 9.3 IV plots for Ex. 9.1.

Example 9.2

Figure 9.4 shows the IV curves (drain current versus drain-source voltage with constant gate source voltage) for a MOSFET. Comment on what the MOSFET looks like in the triode and saturation regions.

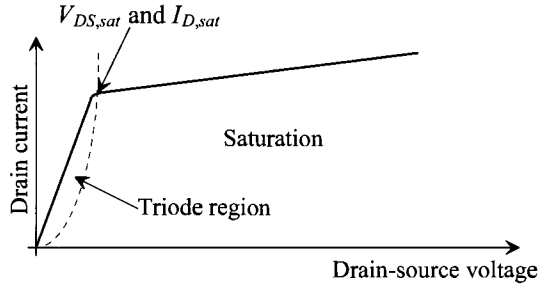


Figure 9.4 IV curves of a MOSFET.

Clearly, in the triode region (also known as the linear or ohmic region), the MOSFET behaves like a resistor. In the saturation region, the MOSFET behaves, as seen in Fig. 9.3b, like a current source in parallel with a resistor. The resistive component, whether in the triode or saturation regions, is often called the MOSFET's output resistance. ■

9.1.1 The Square-Law Equations

The drain current, I_D , is related to the gate-source voltage, V_{GS} , and the drain-source voltage, V_{DS} , using

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L}(V_{GS} - V_{THN})^2(1 + \lambda(V_{DS} - V_{DS,sat})) \qquad (9.1)$$

for $V_{DS} \geq V_{DS,sat}$ and $V_{GS} \geq V_{THN}$. As seen in Fig. 9.4, $V_{DS,sat}$ is the voltage where the MOSFET moves from the triode region to the saturation region. For long-channel MOSFETs, this can be written as

$$V_{DS,sat} = V_{GS} - V_{THN} \qquad (9.2)$$

This term is very important and will be used frequently when doing analog design. Notice that $V_{DS,sat}$ represents the amount of gate-source voltage that we have in *excess* or *over* the threshold voltage. For this reason, it is sometimes called

$$V_{DS,sat} = \text{excess gate voltage} = \text{gate overdrive voltage} \qquad (9.3)$$

Note that while **Eq. (9.2) is only valid for long-channel MOSFETs**, the voltage, $V_{DS,sat}$, simply indicates, for long- or short-channel MOSFETs, the V_{DS} at the boundary between triode and saturation. When $V_{DS} = V_{DS,sat}$, the drain current is labeled $I_{D,sat}$ or

$$I_{D,sat} = \frac{KP_n}{2} \cdot \frac{W}{L}(V_{GS} - V_{THN})^2 = \frac{KP_n}{2} \cdot \frac{W}{L}(V_{DS,sat})^2 \qquad (9.4)$$

Equation (9.1) can be rewritten as

$$I_D = I_{D,sat} + I_{D,sat}\lambda \cdot (V_{DS} - V_{DS,sat}) \tag{9.5}$$

Using the results from Exs. 9.1 and 9.2, we see that the MOSFET behaves, while in the saturation region, like a current source $I_{D,sat}$ in parallel with a resistor of value

$$r_o = \frac{1}{\lambda I_{D,sat}} \tag{9.6}$$

Figure 9.5 shows a gate-drain connected MOSFET, something we'll see often in analog design. Notice that $V_{GS} = V_{DS}$. If $V_{GS} > V_{THN}$ (a current is flowing through the device), then, for the MOSFET to operate in the saturation region, we must have $V_{DS} \geq V_{GS} - V_{THN}$ or $0 \geq -V_{THN}$ (indicating that a gate-drain-connected MOSFET with a current flowing through it is always operating in the saturation region [remember this]). We can also write the requirement for operation in the saturation region as

$$\overbrace{V_D - V_S}^{V_{DS}} \geq \overbrace{V_G - V_S}^{V_{GS}} - V_{THN} \text{ or } V_D \geq V_G - V_{THN} \tag{9.7}$$

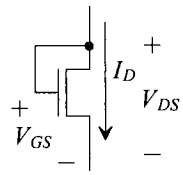


Figure 9.5 Gate-drain connected MOSFET. Also known as a diode-connected MOSFET.

PMOS Square-Law Equations

The PMOS equivalents of Eqs. (9.1) and (9.2) are (for completeness)

$$I_D = \frac{KP_p}{2} \cdot \frac{W}{L}(V_{SG} - V_{THP})^2(1 + \lambda(V_{SD} - V_{SD,sat})) \tag{9.8}$$

and

$$V_{SD,sat} = V_{SG} - V_{THP} \tag{9.9}$$

Note that all we did was swap the subscripts of the symbols used in the NMOS equations. Using this notation, the terminal currents and voltages of the MOSFET (both NMOS and PMOS) **are always positive**.

Qualitative Discussion

To develop some intuitive understanding for MOSFET operation, let's look at the circuits in Fig. 9.6. In the following discussion it is assumed that the MOSFETs are operating in the saturation region and that the terminal voltages (V_{GS} and V_{DS}) of the device do not exceed the power supply rails.

Imagine injecting a current into the drain of the NMOS device in Fig. 9.6a. What happens to the device's drain current? Answer: it goes up. What happens to the device's V_{DS}? Answer: it goes up. If we hold V_{GS} constant then, as seen in Eq. (9.1), we must see an increase in V_{DS} if I_D increases. Stealing current from the NMOS's drain (pulling more of

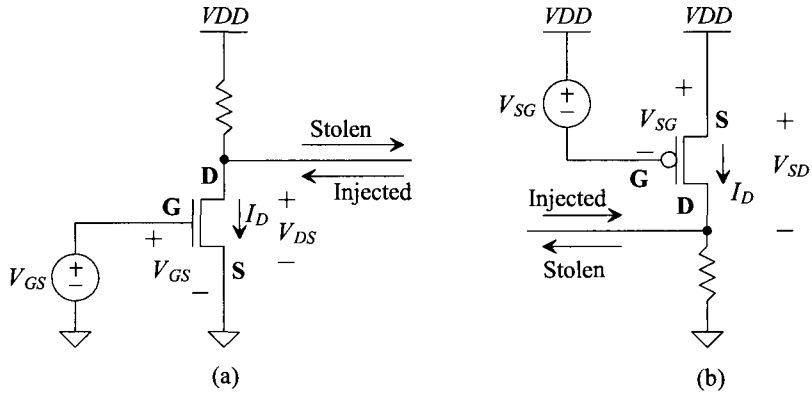


Figure 9.6 Movement of voltages and currents in a MOSFET, see text.

the current flowing down from the resistor away from the MOSFET's drain terminal) results in both the drain current and V_{DS} going down (until the device enters the triode region and ultimately turns off). Make sure that these statements are clearly understood. We will frequently sum or take the difference of currents using MOSFETs; how the voltages and currents change should be "felt" when looking at an analog design, without referring to the equations.

For the PMOS device in Fig. 9.6b, injecting a current into the drain causes the drain current to go down. In the PMOS device, drain current flows out of the drain terminal of the MOSFET. Injecting a current into the drain results in the drain current going down. When we inject this current into the PMOS drain, the source-drain voltage, V_{SD} , decreases as well (meaning that the drain voltage moves towards the power supply voltage *VDD*). Ultimately the device will shut off and the drain current will go to zero. If we steal current from the drain, the drain voltage will move towards ground (noting that $V_{SD} = VDD - V_D$) and the PMOS drain current will increase.

Question: If the channel length modulation parameter, λ, is zero and the MOSFETs stay in the saturation region, will the drain current change with drain-source voltage? Answer: no, the drain current is then independent of V_{DS}, Eq. (9.1). We won't be able to inject or steal a current from the MOSFET without either pushing the MOSFET into triode or moving the drain terminals beyond *VDD* or ground until the MOSFET breaks down. As seen in Eq. (9.1), with $\lambda = 0$, I_D is only dependent on V_{GS} as long as the MOSFET is in saturation.

Example 9.3

For the circuit in Fig. 9.7, describe qualitatively what will happen if we inject a current at the location seen in the figure of $-1\ \mu A \le I \le 1\ \mu A$. Verify your answer with SPICE. (Use the long-channel CMOS models from Ch. 6.)

This circuit, as we will see in Ch. 20, is a cascode current mirror. M1 and M3 are operating in the saturation region with a drain current of 1 μA. Neglecting body effect (the change in threshold voltage when the source and body of the MOSFET aren't at the same potential), we know $V_{GS1} = V_{GS3}$ when M1 and M3 are sized

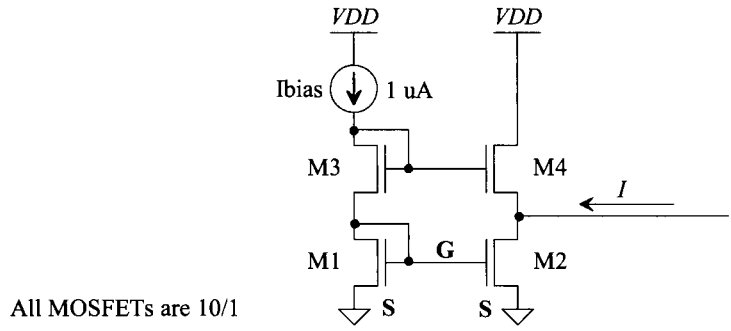


Figure 9.7 Schematic for Ex. 9.3.

the same and have the same drain currents. Because the gates and sources of M2 and M1 are physically tied together, we can write $V_{GS1} = V_{GS2} = V_{GS3} = V_{GS4}$, meaning that 1 μA flows in all MOSFETs.

For the injected current seen in the figure, a positive 1 μA indicates that current flows to the left into the drain of M2 (the source of M4). A positive current also indicates that we are injecting a current into the node. A −1 μA indicates that current flows to the right out of the node (we are stealing current from the node).

If we inject 1 μA into the drain of M2, then M2's drain voltage and M4's source voltage increase causing V_{GS4} to decrease. Since M2 wants to (meaning its V_{GS} is setting) sink a current of 1 μA, our injected current goes entirely through M2 to ground. M4 will shut off ($V_{GS4} \leq V_{THN}$).

If we steal 1 μA from the node ($I = -1$ μA), then the drain voltage of M2 moves downwards towards ground. Then M4 supplies 2 μA of current (V_{GS4} increases).

Figure 9.8 shows the SPICE simulation results. As discussed, M4 starts to shut off (its gate-source voltage falls below V_{THN}) when we inject 1 μA of current. When we steal 1 μA of current (the left side of the plot), V_{GS4} increases to supply 2 μA of current.

To look at the currents flowing in the circuit, zero-volt DC sources can be added. Then, in SPICE, the current through these added sources can be plotted. An example is seen in Fig. 9.9. Simulating the circuit in Fig. 9.7 with the added DC source, we can plot the current through M4, as seen in Fig. 9.10. As mentioned, the drain current shuts off when 1 μA is injected into the node, and it goes to 2 μA when we pull (steal) 1 μA from the node. To monitor the current flowing in M2, we can either add another zero-volt DC source or simply move the injection point to the top of the added DC voltage source in Fig. 9.9.

It's highly recommended that the reader simulate the circuit in Fig. 9.7 under various operating conditions until its operation is fully understood. ■

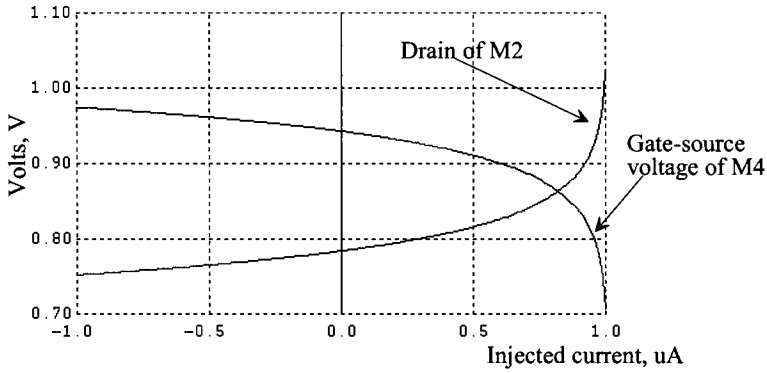


Figure 9.8 SPICE simulations verifying the discussions in Ex. 9.3.

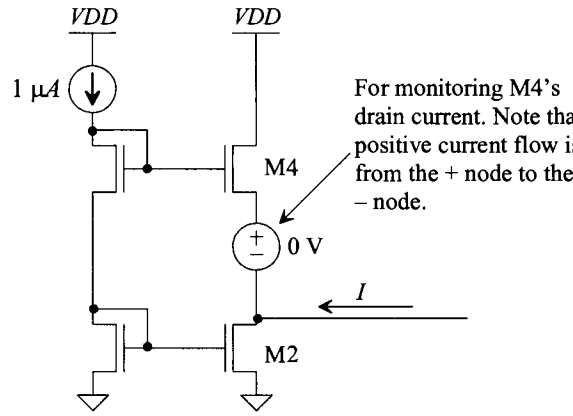


Figure 9.9 Adding zero volt sources to monitor currents in SPICE.

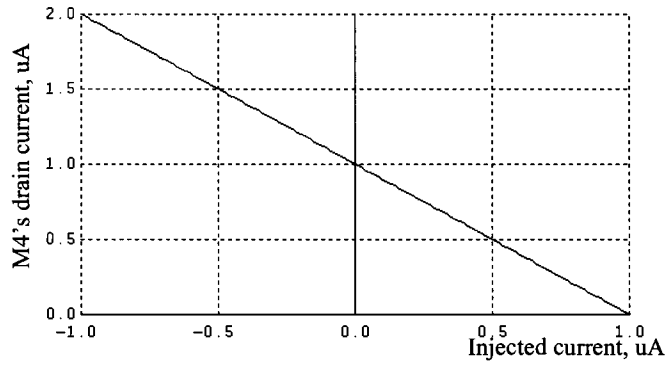


Figure 9.10 How the drain current of M4 changes with injected current.

Threshold Voltage and Body Effect

For an NMOS device, the threshold voltage increases when the source is at a higher potential than the NMOS body (the p-substrate, or ground, in this book). This change in threshold voltage is called the *body effect*. A simple example of a MOSFET operating with body effect (an increased threshold voltage) is seen in Fig. 9.7. Both M3 and M4 have a larger threshold voltage than M1 and M2.

From Ch. 6 the change in threshold voltage can be written as a function of the source to bulk potential, V_{SB}, Fig. 9.11, as

$$V_{THN}(V_{SB}) = V_{THN0} + \gamma_n\left(\sqrt{2|V_{fp}| + V_{SB}} - \sqrt{2|V_{fp}|}\right) \qquad (9.10)$$

and for the PMOS (again we simply switch the subscripts so that all voltages and currents are positive)

$$V_{THP}(V_{BS}) = V_{THP0} + \gamma_p\left(\sqrt{2|V_{fn}| + V_{BS}} - \sqrt{2|V_{fn}|}\right) \qquad (9.11)$$

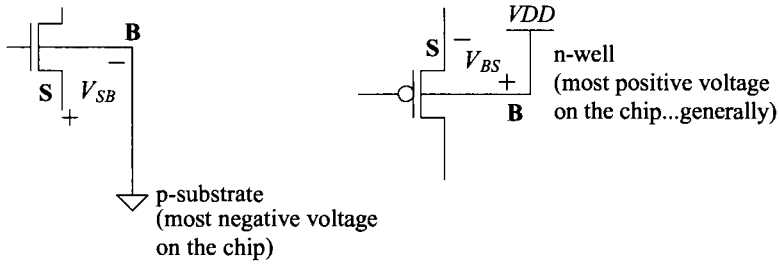


Figure 9.11 The body connection of a MOSFET.

Qualitative Discussion

It's useful to have a feeling for how the threshold voltage changes with increasing source-to-body potential. Figure 9.12 shows a plot of the threshold variation with V_{SB}. For large values of V_{SB}, the threshold voltage change isn't very significant, while for small values it is significant. The circuit seen in Fig. 9.13 is an example where we might want small variations in the threshold voltage. Because the resistor is large, the gate-source voltage will be close to the threshold voltage. If the threshold voltage didn't vary, then the drain current would be linearly related to the input voltage. This circuit is useful for voltage-to-current conversions.

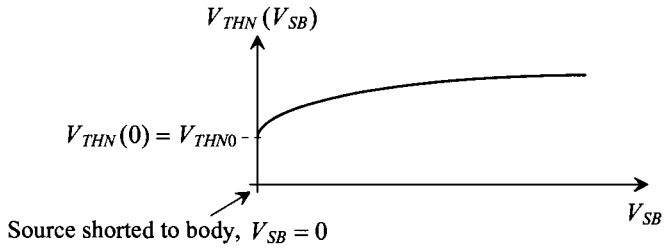


Figure 9.12 Variation in threshold voltage with source to bulk potential.

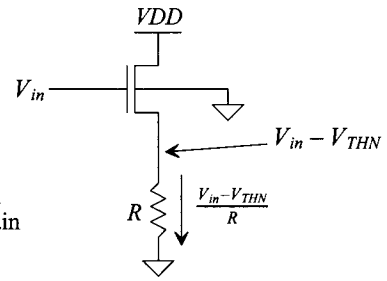


Figure 9.13 An example of a circuit where body effect is important.

Example 9.4

Simulate the operation of the voltage-to-current converter in Fig. 9.13 if the size of the MOSFET is 10/1 and the resistor is 10MEG. Use long-channel devices.

Figure 9.14a shows how the current varies through the MOSFET with V_{in} changing from 1 V to 5 V. We start at 1 V V_{in} because the current will shut off when $V_{in} < V_{THN}$, resulting in a large nonlinearity. Looking at the linearity of the current, it looks really good (straight). However, in Fig. 9.14b we take the derivative of the line in (a) to see the slope. The variation in the slope is approximately 20%. For precision design of voltage-to-current converters, the variation in the linearity of the threshold voltage can be a limiting factor. We should note that channel length modulation also contributes to nonlinearities (so increasing the length, to increase r_o, of the device can help improve the linearity).

Question: what is the ideal slope for Fig. 9.14; that is, what is the ideal value of dI/dV_{in}? Answer: $1/R$ or, in this example, $100 \times 10^{-9}\ A/V$. ■

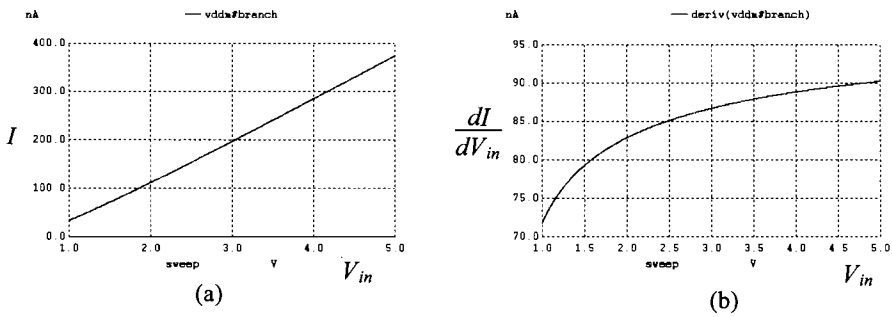


Figure 9.14 (a) Current flowing in the circuit of Fig. 9.13 and (b) its linearity.

There isn't any way to eliminate the body-effect in an n-well process where the NMOS device body is the substrate (though, if a triple well process is used, the NMOS devices can sit in their own wells). However, the PMOS devices can sit in their own wells and have separate bodies (and so we can design without body effect).

The Triode Region

The relationship between I_D, V_{GS}, and V_{DS} for an NMOS device operating in the triode region is

$$I_D = KP_n \frac{W}{L} \cdot \left((V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{9.12}$$

where $V_{GS} \geq V_{THN}$ and $V_{DS} \leq V_{DS,sat}$ $(= V_{GS} - V_{THN})$. The equivalent expression for the PMOS device is

$$I_D = KP_p \frac{W}{L} \cdot \left((V_{SG} - V_{THP}) V_{SD} - \frac{V_{SD}^2}{2} \right) \tag{9.13}$$

where $V_{SG} \geq V_{THP}$ and $V_{SD} \leq V_{SD,sat}$ $(= V_{SG} - V_{THP})$.

We said earlier, in Fig. 9.4 and the associated discussion, that the MOSFET looks like a resistor when it is operating in the triode region. To estimate the value of the resistance, we can use

$$R_{ch}^{-1} = \frac{\partial I_D}{\partial V_{DS}} = KP_n \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN}) - KP_n \cdot \frac{W}{L} \cdot V_{DS} \tag{9.14}$$

or

$$R_{ch} = \frac{1}{KP_n \cdot \frac{W}{L} \cdot (V_{DS,sat} - V_{DS})} \tag{9.15}$$

If $V_{DS,sat} >> V_{DS}$, this equation can be written as

$$R_{ch} \approx \frac{1}{KP_n \cdot \frac{W}{L} (V_{GS} - V_{THN})} \tag{9.16}$$

The Cutoff and Subthreshold Regions

For general design, we normally assume that the device is off (meaning zero drain current) when $V_{GS} < V_{THN}$ or $V_{SG} < V_{THP}$. However, it would be more correct to say that the device is operating in the subthreshold region (instead of the strong inversion region we've discussed so far in this chapter). The subthreshold current of a MOSFET operating in the active region (the amplifying region, which is similar to the saturation region for a MOSFET operating in strong inversion) is modeled using

$$I_D = I_{D0} \cdot \frac{W}{L} \cdot e^{(V_{GS} - V_{THN})/nV_T} \tag{9.17}$$

$V_{GS} \leq V_{THN}$ and $V_{DS} > 4V_T$ (remembering the thermal voltage, V_T, is kT/q or 26 mV at room temperature). The current I_{D0} is the (scaled) current that flows when $V_{GS} - V_{THN} = 0$ (the gate-source voltage is equal to the threshold voltage). Note that Eq. (9.17) shows no dependence on V_{DS}. This indicates that the MOSFET has infinite output resistance when operating in the active region (which isn't the case, and so this equation has limitations).

9.1.2 Small Signal Models

A quick note concerning symbols: throughout the book we'll represent a signal containing both AC and DC components by a lowercase letter with uppercase subscripts. AC signals are represented with both lowercase letters and subscripts, while DC signals are represented with both uppercase letters and subscripts, see Fig. 9.15. (Note that if the maximum value of v_{GS} is *VDD* in Fig. 9.15, then the MOSFET is either in the saturation region or off [$V_{GS} < V_{THN}$].)

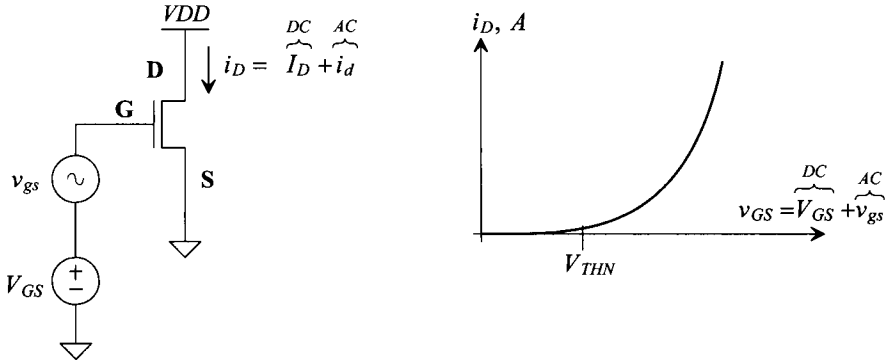


Figure 9.15 IV curves of a MOSFET in saturation.

Small-signal models are used to calculate AC gains. Figure 9.16 shows the basic idea. We adjust the DC gate-source voltage, V_{GS} , to a value that corresponds to a DC drain current I_D. At this bias point, we apply a small AC signal where $|v_{gs}| << V_{GS}$ and $|i_d| << I_D$. Because the signals are small, the change in drain current, i_d , with gate voltage, v_{gs} is essentially linear (as seen in the blown-up view in Fig. 9.16). If our AC signal amplitudes get comparable to the DC operating (or bias) points, we get high nonlinearity (which makes feedback necessary for any highly linear amplifier).

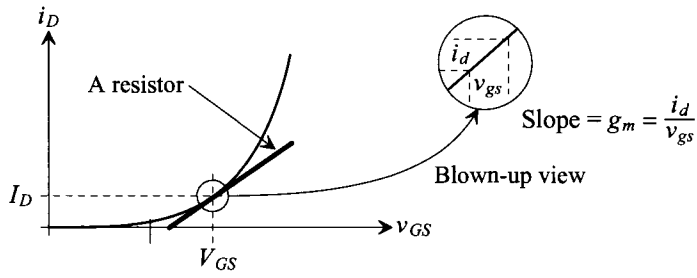


Figure 9.16 How small-signal parameters are calculated.

We often treat DC voltage sources as shorts when doing AC analysis (and current sources as opens). Looking at Fig. 9.15, we see that it's impossible for the AC signal to generate a voltage across the DC source. The voltage across the DC source is fixed with zero AC component so that the DC voltage source is an AC short.

Finally note that performing a small-signal analysis consists of the following steps:

(1) Calculating the bias point of the circuit using the DC equations from Sec. 9.1.1.

(2) Using the DC values from (1) to calculate the small-signal parameters. Small-signal AC parameters are always a function of the DC operating point.

(3) Replacing the active elements (e.g., MOSFETs) with their small-signal models. At the same time, the DC sources are removed (that is, short out all DC voltage sources and open up all DC current sources).

An AC analysis doesn't include any DC voltages or currents. For example, suppose we have an (AC) v_{gs} = 1 mV. It *doesn't make sense* to say that the MOSFET is off because $v_{gs} < V_{THN}$. To perform a small-signal analysis (to calculate small-signal parameters), the MOSFETs are in saturation or triode (meaning $V_{GS} > V_{THN}$).

Transconductance

An extremely important parameter in analog design is a device's transconductance, g_m. The g_m of a device is an AC small-signal parameter that relates the AC gate voltage to the AC drain current, that is,

$$i_d = g_m \cdot v_{gs} \tag{9.18}$$

From Figs. 9.15 and 9.16, g_m is simply the slope of the line at the intersection of the DC operating values V_{GS} and I_D. Using Eq. (9.1), without concerning ourselves with channel-length modulation, we can write

$$i_D = i_d + I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot \left(\overbrace{v_{gs} + V_{GS}}^{v_{GS}} - V_{THN} \right)^2 \tag{9.19}$$

To find the slope (g_m) of the i_D-v_{GS} curve at the fixed bias points V_{GS} and I_D (Fig. 9.16), we take the derivative of this equation with respect to the x-axis variable (v_{GS})

$$g_m = \left[\frac{\delta i_D}{\delta v_{GS}} \right]_{V_{GS} = \text{constant}}^{I_D = \text{constant}} = KP_n \cdot \frac{W}{L} \cdot (v_{gs} + V_{GS} - V_{THN}) \tag{9.20}$$

If we remember

$$\beta_n = KP_n \cdot \frac{W}{L} \text{ and } |v_{gs}| << V_{GS} \tag{9.21}$$

then we can write

$$g_m = \beta_n \left(\overbrace{V_{GS} - V_{THN}}^{V_{DS,sat}} \right) = \sqrt{2\beta_n I_D} \tag{9.22}$$

The key points are that g_m goes up as the root of the drain current and linearly with $V_{DS,sat}$.

Example 9.5
Calculate the DC and AC voltages and currents for the circuit seen in Fig. 9.17. Use the long-channel MOSFET parameters from Ch. 6.

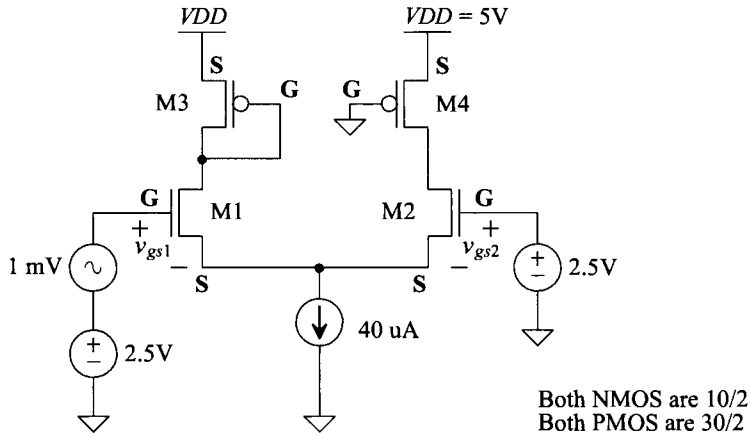


Figure 9.17 Circuit discussed in Ex. 9.5.

We begin by looking at the DC operating point. The gates of both M1 and M2 are at 2.5V. This is necessary to keep them turned on. Since the sources of M1 and M2 are physically tied together, $V_{GS1} = V_{GS2}$ and $I_{D1} = I_{D2} = 20\ \mu A$. Rewriting Eq. (9.1), neglecting channel-length modulation, results in

$$V_{GS} = \overbrace{\sqrt{\frac{2I_D}{KP_n} \cdot \frac{L}{W}}}^{V_{DS,sat}} + V_{THN} \qquad (9.23)$$

Assuming both M1 and M2 are operating in the saturation region (we'll verify this in a moment), we get

$$V_{GS1} = V_{GS2} = \sqrt{\frac{40}{120} \cdot \frac{2}{10}} + 0.8 = 1.058\ V \rightarrow V_{DS,sat} \approx 250\ mV$$

The source-to-gate voltage for M3 (knowing its drain current is 20 μA) is

$$V_{SG3} = \sqrt{\frac{2 \cdot 20}{40} \cdot \frac{2}{30}} + 0.9 = 1.158\ V \rightarrow V_{SD,sat} \approx 250\ mV$$

The drain potential of M1 and M3 is

$$V_{D1} = V_{D3} = VDD - V_{SG3} = 3.842\ V$$

From Fig. 9.5 and the associated discussion, we know that M3 is in saturation. To see if M1 is in saturation, we use Eq. (9.7)

$$V_{D1} \overset{?}{\geq} V_{G1} - V_{THN} \rightarrow 3.842 \geq 1.7\ V \text{ (yes, M1 is in saturation)}$$

Next we look at M4. M4's source-to-gate voltage is 5 V. It's very likely that it is in triode. We know, for a PMOS to be operating in the saturation region, we must have

$$\overbrace{V_{SD}}^{V_S - V_D} \geq \overbrace{V_{SG}}^{V_S - V_G} - V_{THP} \rightarrow V_D \leq V_G + V_{THP} \tag{9.24}$$

M4's gate is grounded ($V_G = 0$), so for M4 to be in saturation, $V_D \leq 0.9\ V$. Since the gate of M2 is at 2.5 V and $V_{GS2} = 1.058$, then its source is 1.442 V, which makes it impossible for M4 to be saturated. To estimate the drain-to-source voltage of M4, we use Eq. (9.13), knowing that M4's drain current is 20 μA and its gate-source voltage is 5 V

$$20 = 40 \cdot \frac{30}{2} \cdot \left((5 - 0.9) V_{SD} - \frac{V_{SD}^2}{2} \right)$$

which results in V_{SD} = 8.13 mV. The drains of M4 and M2 are then 4.992 V or essentially at *VDD*. Clearly M2 is operating in the saturation region. M4 can be thought of as a resistor with a value of (Eq. [9.16] noting $V_{SD,sat} >> V_{SD}$, that is, 4.1 V >> 8.13 mV)

$$R_{chM4} = \frac{1}{(40\ \mu A/V) \cdot \frac{30}{2} \cdot 4.1} = 407\ \Omega$$

Note that we could have estimated the resistance using $V_{SD}/I_D = 8.13m/20\mu$ = 407 Ω. Before moving on, let's do an operating point analysis for this circuit (an .op analysis). The SPICE netlist is seen below.

```
*** Example 9.5 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
** for the operating point analysis
print all
*
** for the AC analysis
*plot mag(vd13) mag(vs12) mag(vg1) mag(vd34)
*
** for the transient analysis
*plot vd13
*plot vs12
*plot vg1
.endc

.option scale=1u
.op
**.ac dec 100 1 10k
**.tran 1u 300u

VDD   VDD   0    DC   5
VG1   VG1   0    DC   2.5   AC   1m   SIN 2.5 1m 10k
VG2   VG2   0    Dc   2.5
Ibias VS12  0    DC   40u
```

```
M1    VD13  VG1   VS12  0     NMOS L=2 W=10
M2    VD24  VG2   VS12  0     NMOS L=2 W=10
M3    VD13  VD13  VDD   VDD   PMOS L=2 W=30
M4    VD24  0     VDD   VDD   PMOS L=2 W=30

.MODEL NMOS NMOS LEVEL = 3
+ TOX   = 200E-10          NSUB  = 1E17       GAMMA = 0.5
+ PHI   = 0.7              VTO   = 0.8        DELTA = 3.0
+ UO    = 650              ETA   = 3.0E-6     THETA = 0.1
+ KP    = 120E-6           VMAX  = 1E5        KAPPA = 0.3
+ RSH   = 0                NFS   = 1E12       TPG   = 1
+ XJ    = 500E-9           LD    = 100E-9
+ CGDO  = 200E-12          CGSO  = 200E-12    CGBO  = 1E-10
+ CJ    = 400E-6           PB    = 1          MJ    = 0.5
+ CJSW  = 300E-12          MJSW  = 0.5
*
.MODEL PMOS PMOS LEVEL = 3
+ TOX   = 200E-10          NSUB  = 1E17       GAMMA = 0.6
+ PHI   = 0.7              VTO   = -0.9       DELTA = 0.1
+ UO    = 250              ETA   = 0          THETA = 0.1
+ KP    = 40E-6            VMAX  = 5E4        KAPPA = 1
+ RSH   = 0                NFS   = 1E12       TPG   = -1
+ XJ    = 500E-9           LD    = 100E-9
+ CGDO  = 200E-12          CGSO  = 200E-12    CGBO  = 1E-10
+ CJ    = 400E-6           PB    = 1          MJ    = 0.5
+ CJSW  = 300E-12          MJSW  = 0.5

.end
```

A portion of the operating point analysis output is

```
vd13 = 3.854977e+00   (we hand calculated 3.842)
vd24 = 4.989641e+00   (we hand calculated 4.992)
vs12 = 1.171189e+00   (we hand calculated 1.442)
```

The only significant difference between our hand calculations and the simulation results is the potential calculated for the sources of M1/M2. The smaller value in the simulation is because we didn't include the body effect in our calculations. We used $V_{THN0} = 0.8\ V$ when the actual threshold voltage was closer to $1.1\ V$.

Let's now turn our attention towards the AC analysis. The transconductance of M1 and M2 is

$$g_{m1} = g_{m2} = \sqrt{2 \cdot KP_n \frac{W}{L} \cdot I_D} = \sqrt{2 \cdot 120\mu \cdot \frac{10}{2} \cdot 20\mu} \approx 150\ \mu A/V$$

The transconductance of M3 is

$$g_{m3} = \sqrt{2 \cdot KP_p \frac{W}{L} \cdot I_D} = \sqrt{2 \cdot 40\mu \cdot \frac{30}{2} \cdot 20\mu} \approx 150\ \mu A/V$$

M4 is operating in the triode region and so we think of it as a resistor (407 Ω). Figure 9.18 shows the simplified AC schematic of Fig. 9.17. Notice how we can replace M3 with a resistor of $1/g_{m3}$. This is because the AC voltage across M3 is $v_{sg3} = v_{sd3}$ and the AC current through it is i_d or

$$\frac{1}{g_m} = \frac{v_{sd}}{i_d} = \frac{v_{sg}}{i_d} \tag{9.25}$$

A gate-drain connected MOSFET with a current flowing through it is always in saturation, as discussed earlier, and can be thought of as a small-signal resistance of $1/g_m$ (again, remember this).

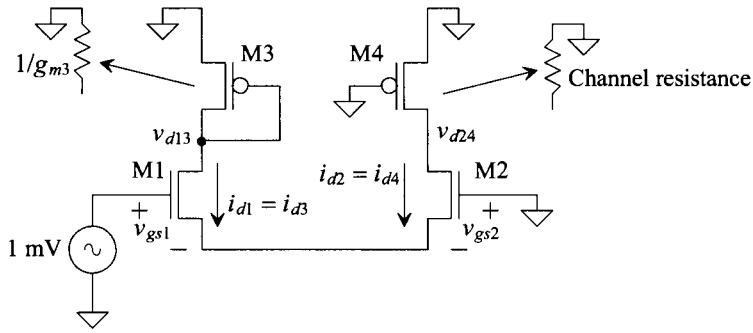


Figure 9.18 AC schematic for the circuit in Fig. 9.17.

When we talk about negative currents or voltages in an AC small-signal analysis, we are indicating that the overall AC + DC signal is decreasing. For example, we'll see in a moment that the AC small-signal drain current in M2, Fig. 9.18, is negative. This means that the current may be going from 20 μA (its DC operating point) to, say, 19.995 μA with an AC input. We would then say that the AC drain current is, i_{d2}, – 5 nA.

To analyze the circuit, we can begin by writing

$$1\ mV = v_{gs1} - v_{gs2} = \frac{i_{d1}}{g_{m1}} - \frac{i_{d2}}{g_{m2}}$$

We know that $g_{m1} = g_{m2}$ and, from Fig. 9.18,

$$i_{d1} = -i_{d2}$$

so

$$v_{gs1} = -v_{gs2} = 0.5\ mV$$

The sources of M1 and M2 are at an AC voltage of 0.5 mV. The AC drain currents are

$$i_{d1} = i_{d3} = -i_{d2} = -i_{d4} = g_{m1} \cdot v_{gs1} = (150\ \mu A/V) \cdot 0.5\ mV = 75\ nA$$

This means the overall (AC + DC) drain current of M1/M3 is

$$i_{D1} = 20\ \mu A + 0.075 \sin 2\pi f t$$

where f is the frequency of our 1 mV input signal and

$$i_{D2} = 20\ \mu A - 0.075 \sin 2\pi f t$$

noting that i_{D1} and i_{D2} must sum to the DC bias of 40 μA.

The (AC) drain voltage of M1 and M3 is

$$v_{d1} = v_{d3} = -i_{d1} \cdot \frac{1}{g_{m3}} = -\frac{75\ nA}{150\ \mu A/V} = -0.5\ mV$$

The voltages on the drains of M2 and M4 are

$$v_{d2} = v_{d4} = -i_{d4} \cdot R_{chM4} = (75\ nA) \cdot 407 = 0.03\ mV$$

We'll verify these voltages with SPICE in a moment. This lengthy example illustrates several key concepts that will be used throughout the analysis and design of analog CMOS circuits in this book. Before moving on, make sure that the concepts are clear and well understood (SPICE can be very helpful for this).

Question: How would we look at the SPICE simulated currents (AC and DC) flowing in the MOSFETs in Fig. 9.17? Answer: add zero-volt voltage sources as seen in Fig. 9.9 and the associated discussion. ■

AC Analysis

We can perform a small-signal analysis using a SPICE ".ac" statement. Just like in our hand calculations, SPICE first calculates the operating point using the DC sources (no AC sources are present in the circuit). Then SPICE replaces the active devices with their small-signal equivalent circuits (no DC sources in the circuit, now just the AC sources). The key point here is that SPICE assumes the user knows that the AC components should be much smaller than the DC components. If we were to simulate, using an AC analysis, the operation of the circuit in Fig. 9.17, but used a 1,000 V AC input instead of a 1 mV AC input, SPICE would simply scale all of the outputs (the simulation won't tell the user that the AC input is too big).

The possible syntax for an .ac analysis statement is

```
.AC DEC ND FSTART FSTOP
.AC OCT NO FSTART FSTOP
.AC LIN NP FSTART FSTOP
```

where DEC stands for decade (our x-axis in an .ac analysis is frequency) and ND is the number of points per decade (OCT stands for octave and LIN stands for linear). FSTART and FSTOP are the starting and ending frequencies for the small-signal AC analysis.

We can do a SPICE AC analysis for the circuit in Fig. 9.17 by changing the .op analysis used in the netlist to an AC analysis control statement

```
.ac dec 100 1 10k
```

where we've picked a frequency range of 1 Hz to 10k Hz with 100 points calculated per decade. (The first decade is 1 to 10 Hz, the second, 10 Hz to 100 Hz, etc. If we had used a start frequency of 2 Hz, then the first decade would be 2 Hz to 20 Hz, the second would be 20 Hz to 200 Hz, noting that increasing by a decade is multiplying by 10 and decreasing by a decade is dividing by 10.) The input signal (the gate of M1) is

```
VG1   VG1   0     DC   2.5   AC   1m   SIN 2.5 1m 10k
```

The operating point analysis ignores the AC voltage of 1 mV and the sinusoid specification (a sine wave with a DC offset of 2.5 V, a peak amplitude of 1 mV, and a frequency of 10 kHz). The AC analysis uses the DC value to calculate the operating point and the AC value to calculate the small-signal AC voltages and currents. We'll discuss the SIN portion in a moment when we talk about transient analysis. The simulation results are seen in Fig. 9.19. The values should be compared to the values calculated in Ex. 9.5. The only (small) difference is the voltage calculated at the sources of M1 and M2. We calculated 0.5 mV, while SPICE gives 0.42 mV. This is due to the body effect transconductance, g_{mb}, which is discussed on the next page.

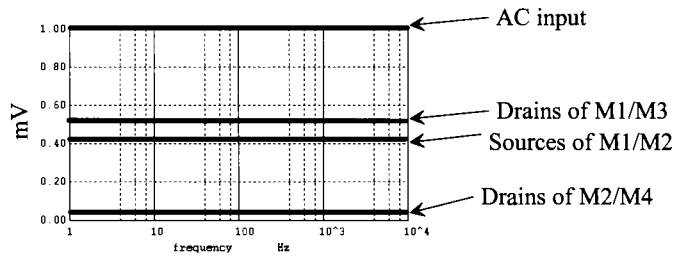


Figure 9.19 AC simulation results for the circuit in Fig. 9.17.

Transient Analysis

The AC analysis is frequently used to look at the frequency response of a circuit. However, as we have just discussed, it will not show large signal nonlinearity. A transient analysis, however, will show large signal nonlinearity (the x-axis is time just like the x-axis on an oscilloscope display). The control statement for a transient analysis is

```
.TRAN TSTEP TSTOP <TSTART <TMAX> <UIC>
```

where TSTEP is the step size (say 1/1,000) of the stop time TSTOP. TSTART is an optional parameter to specify a later starting time. The simulation always starts at 0 seconds. However, in some simulations there are start-up transient signals that we are not interested in. To avoid saving this uninteresting data in our output file (to reduce the output file size), we can specify a start-up time later than 0. In this book we won't use this option. The TMAX parameter specifies a maximum step size for the simulation. If, for example, a sine wave is plotted and it looks *jagged* (meaning that our step size is too coarse), we would use a smaller step size (TMAX) in the simulation to smooth it out. UIC indicates, "Use Initial Conditions." If UIC isn't present in a simulation, SPICE ignores all initial conditions. A sample transient control statement is

```
.TRAN  1n 1000n 0 1n UIC
```

To simulate the circuit in Fig. 9.17 using a transient analysis, we use the input signal source of

```
VG1   VG1   0     DC    2.5    AC    1m    SIN 2.5 1m 10k
```

In a transient analysis, SPICE always ignores the AC component. It ignores the DC component as well if pulse, sinusoid, or some other signal is specified. Note that the SIN specification **has nothing to do with AC analysis**. For the transient simulation of the

circuit in Fig. 9.17, we use a sinusoid with a DC offset of 2.5 V, a peak amplitude of 1mV, and a frequency of 10 kHz (picked arbitrarily for this simulation). The simulation results showing the drain potential of M1 and M3 are seen in Fig. 9.20.

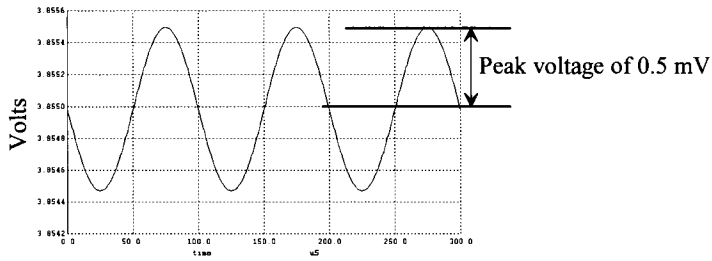


Figure 9.20 Transient simulation showing the drain voltages of M1 and M3 from Fig. 9.17.

Body Effect Transconductance, g_{mb}

Figure 9.21 shows the setup to determine how the drain current varies with source-to-bulk potential V_{SB}. If we raise the potential of the source, we eventually run into the point where the source potential is less than a V_{THN} below the gate potential, and the MOSFET shuts off.

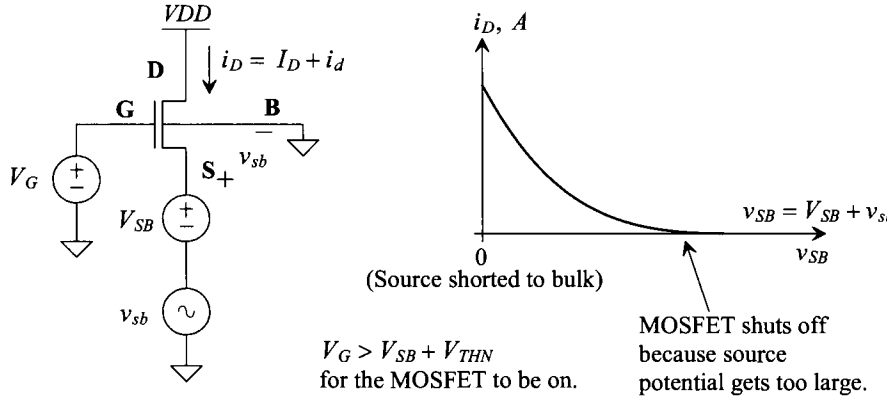


Figure 9.21 How the drain current changes with body-effect.

Remembering that the body-effect is the variation of the threshold voltage with V_{SB}, we can write

$$g_{mb} = \left[\frac{\partial i_D}{\partial v_{SB}}\right]_{V_{SB}\,=\,\text{constant}}^{I_D\,=\,\text{constant}} = \frac{\partial}{\partial v_{SB}}\left[\frac{KP_n}{2}\cdot\frac{W}{L}(V_{GS}-V_{THN})^2\right]_{V_{SB}\,=\,\text{constan}}^{I_D\,=\,\text{constant}} \qquad (9.26)$$

or

$$g_{mb} = \overbrace{KP_n \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})}^{g_m} \cdot \left(-\frac{\partial V_{THN}}{\partial v_{SB}}\right) \tag{9.27}$$

or (noting there is a variation in v_{GS} with v_{SB} but this is simply the forward g_m).

$$g_{mb} = g_m \cdot \eta \tag{9.28}$$

The factor η describes how the threshold voltage changes with V_{SB} and generally ranges from 0 (no body effect) to 0.5. The minus sign in Eq. (9.27) simply indicates that the AC drain current contributions from changes in the threshold voltage with V_{SB} (body effect) flow in the opposite direction of the contributions from the forward transconductance, g_m. Figure 9.22 shows the AC small-signal model of the MOSFET with both small-signal transconductances included.

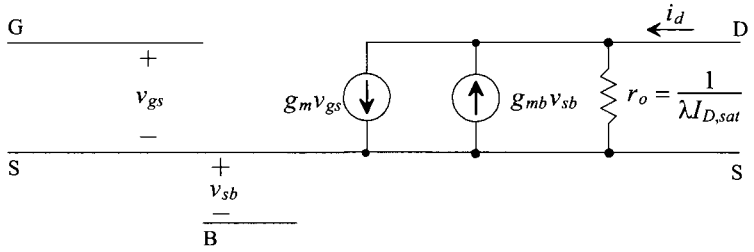


Figure 9.22 Small-signal MOSFET with both transconductances.

Output Resistance

We've already calculated the output resistance of a MOSFET operating in the saturation region in Eq. (9.6) (added to Fig. 9.22). Let's calculate this value again using the circuit seen in Fig. 9.23. We can write

$$r_o^{-1} = \left[\frac{\partial i_D}{\partial v_{DS}}\right]_{\substack{I_D = \text{constant} \\ V_{DS} = \text{constant}}} = \frac{\partial}{\partial v_{DS}}\left(\frac{KP_n}{2} \cdot \frac{W}{L}(V_{GS} - V_{THN})^2\left(1 + \lambda\left(\overbrace{v_{ds} + V_{DS}}^{v_{DS}} - V_{DS,sat}\right)\right)\right) \tag{9.29}$$

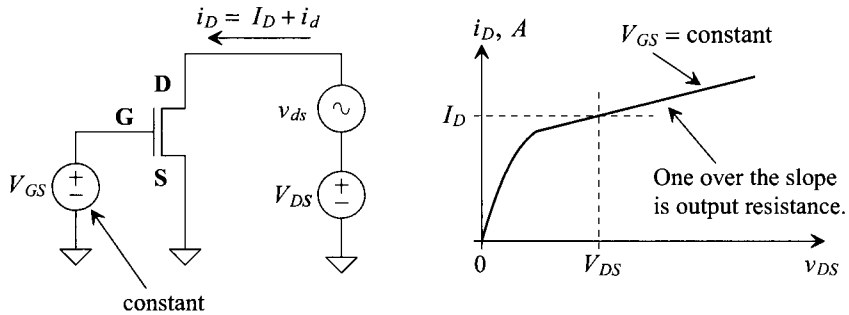


Figure 9.23 How the drain current changes with drain-to-source voltage.

or, once again,

$$r_o = \frac{1}{\lambda I_{D,sat}} \tag{9.30}$$

Example 9.6

Determine λ, using simulations, for the MOSFETs in Ex. 9.5.

The V_{GS} (NMOS) and V_{SG} (PMOS) of the MOSFETs in Ex. 9.5 are 1.05 V and 1.15 V, respectively (roughly for 20 μA of bias current). Figure 9.24 shows the IV plots for the MOSFETs and the reciprocal of the derivative of the drain current (which gives us the output resistance). Because the NMOS threshold voltage is 0.8 V and the PMOS threshold voltage is 0.9 V, both MOSFETs have a $V_{DS,sat}$ of 250 mV and a channel length of 2. The channel-length modulation parameter is calculated using

$$\lambda_n = \frac{1}{I_{D,sat} \cdot r_o} = \frac{1}{20\mu \cdot 5MEG} = 0.01\ V^{-1}$$

and

$$\lambda_p = \frac{1}{20\mu \cdot 4MEG} = 0.0125\ V^{-1}$$

noting that the values are approximations. Also note that the output resistance is very dependent on drain-to-source voltage. ■

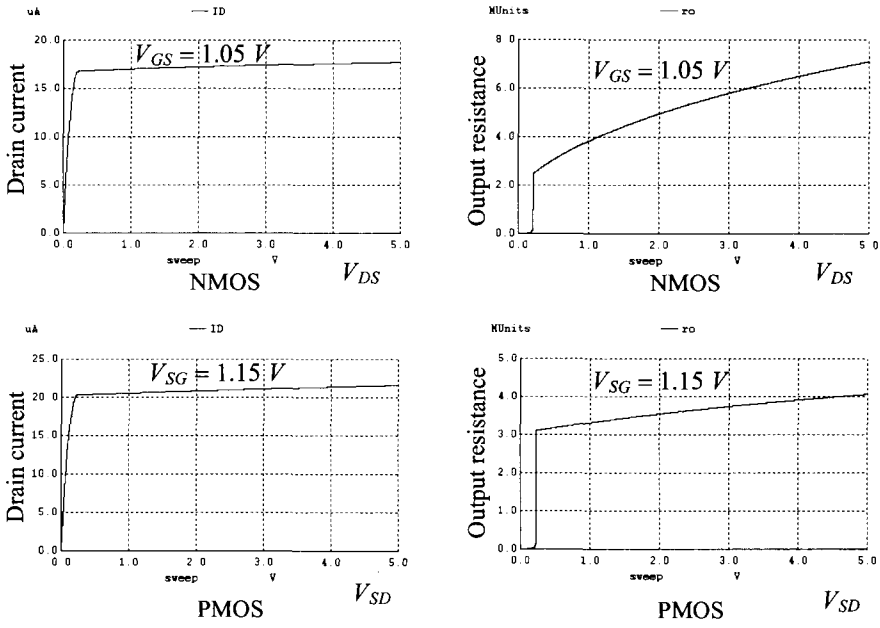


Figure 9.24 Using simulations to determine lambda.

It's of interest to determine how output resistance changes with channel length and $V_{DS,sat}$. Remember

$$I_{D,sat} = \frac{KP_N}{2} \cdot \frac{W}{L} \cdot V_{DS,sat}^2 \tag{9.31}$$

and, from Ch. 6,

$$\lambda \propto \frac{1}{L} \tag{9.32}$$

so we can write

$$r_o \propto \frac{L^2}{V_{DS,sat}^2} \tag{9.33}$$

If the length of the MOSFET is increased, for fixed V_{GS} (equivalent to saying for fixed $V_{DS,sat}$, since $V_{DS,sat} = V_{GS} - V_{THN}$), then the drain current decreases and the output resistance increases. If the length is held constant, then decreasing $V_{DS,sat}$ causes the drain current to decrease and the output resistance to increase. We might think that, to get large output resistance, all we have to do is use a very long-length device. However, as we'll show next, this causes the inherent speed of the MOSFETs to decrease.

MOSFET Transition Frequency, f_T

Examine the circuit in Fig. 9.25. The drain of the MOSFET is at AC ground (shorted through the DC drain-source voltage). This causes, from the gate terminal, C_{gs} and C_{gd}, to appear as though they are in parallel. We can then write

$$v_{gs} = \frac{i_g}{j\omega \cdot (C_{gs} + C_{gd})} \tag{9.34}$$

Knowing $i_d = g_m \cdot v_{gs}$, we can write the current gain of the MOSFET as

$$\left| \frac{i_d}{i_g} \right| = \frac{g_m}{2\pi f \cdot (C_{gs} + C_{gd})} \tag{9.35}$$

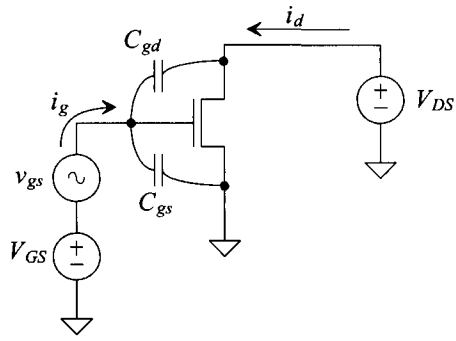


Figure 9.25 Determining the transition frequency of an NMOS transistor.

If we call the frequency where the current gain of the MOSFET is one, Fig. 9.26, the transition frequency, f_T (the transistor transitions from an amplifier to an attenuator) and we remember that $C_{gs}\left(=\frac{2}{3}WLC'_{ox}\right) >> C_{gd}$, then we can write (see Eq. [9.22])

$$f_T \approx \frac{g_m}{2\pi C_{gs}} = \frac{3KP_n \cdot (V_{GS} - V_{THN})}{4\pi \cdot L^2 C'_{ox}} = \frac{3\mu_n}{4\pi} \cdot \frac{V_{DS,sat}}{L^2} \qquad (9.36)$$

This equation is *fundamentally important.* To get high speed, we need to use minimum channel lengths and design with a large $V_{DS,sat}$. However, as seen in Eq. (9.33), using minimum lengths results in lower output resistances (and, as we'll see later, lower gain). What this indicates is a constant gain-bandwidth product (higher speed resulting in lower gain). In using a large $V_{DS,sat}$, the MOSFETs enter the triode region earlier (resulting in reduced output swing in amplifiers or mirrors). Note that the f_T for the PMOS device is inherently smaller than that of the NMOS device due to the lower value of hole mobility.

For short-channel devices, the mobility is no longer constant but starts to decrease (velocity saturation as discussed in Ch. 6) with decreasing length (increasing electric field between the drain and channel). Because of this, we treat the term μ_n/L as a relatively constant value and rewrite Eq. (9.36) as

$$f_T \propto \frac{V_{DS,sat}}{L} \text{ (Short-channel devices)} \qquad (9.37)$$

Again, for high-speed, we need to use the smallest possible channel length and large $V_{DS,sat}$.

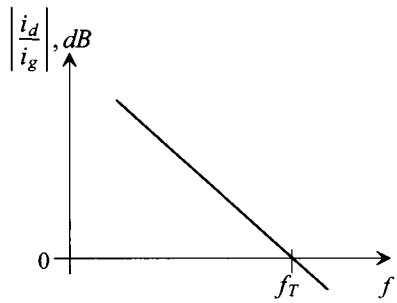


Figure 9.26 The transition frequency of a MOSFET.

General Device Sizes for Analog Design

Based on Eqs. (9.33) and (9.36), we can make some general statements about selecting device L, W, and $V_{DS,sat}$. For general analog design, use an L of 2–5 times minimum (in this book L_{min} = 1, since we scale the MOSFET sizes by either 1 μm [long-channel MOSFETs] or 50 nm [short-channel MOSFETs] in the SPICE netlists or layout). We'll use an L, for analog design, of 2 as a good trade-off between speed and gain.

For general design, use a $V_{DS,sat}$ of 5% of *VDD*. For our long-channel MOSFETs (*VDD* = 5 V), we'll use a $V_{DS,sat}$ of 250 mV, while for the short-channel process (*VDD* = 1V), we'll use 50 mV. Table 9.1 shows the parameters for general analog design using the long-channel process discussed in this chapter.

Table 9.1 Typical parameters for analog design using the *long-channel* CMOS process discussed in this book. Note that the parameters may change with temperature or drain-to-source voltage (e.g., Fig. 9.24).

Long-channel MOSFET parameters for general analog design *VDD* = 5 V and a scale factor of **1 μm** (*scale* = 1e–6)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias current, I_D	20 μA	20 μA	Approximate
W/L	10/2	30/2	Selected based on I_D and $V_{DS,sat}$
$V_{DS,sat}$ and $V_{SD,sat}$	250 mV	250 mV	For sizes listed
V_{GS} and V_{SG}	1.05 V	1.15 V	No body effect
V_{THN} and V_{THP}	800 mV	900 mV	Typical
$\partial V_{THN,P}/\partial T$	−1 mV/C°	−1.4 mV/C°	Change with temperature
KP_n and KP_p	120 μA/V^2	40 μA/V^2	t_{ox} = 200 Å
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	1.75 fF/μm^2	1.75 fF/μm^2	$C_{ox} = C'_{ox}WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	35 fF	105 fF	PMOS is three times wider
C_{gsn} and C_{sgp}	23.3 fF	70 fF	$C_{gs} = \frac{2}{3}C_{ox}$
C_{gdn} and C_{dgp}	2 fF	6 fF	$C_{gd} = CGDO \cdot W \cdot scale$
g_{mn} and g_{mp}	150 μA/V	150 μA/V	At I_D = 20 μA
r_{on} and r_{op}	5 MΩ	4 MΩ	Approximate at I_D = 20 μA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	750 V/V	600 V/V	Open circuit gain
λ_n and λ_p	0.01 V^{-1}	0.0125 V^{-1}	At L = 2
f_{Tn} and f_{Tp}	900 MHz	300 MHz	For L =2, f_T goes up if L = 1

Subthreshold g_m and V_{THN}

Before leaving the topic of small-signal models, let's derive the forward transconductance of the MOSFET operating in the subthreshold region. Using Eqs. (9.17) and (9.20), we can write

$$g_m = \left[\frac{\delta i_D}{\delta v_{GS}}\right]_{V_{GS}=\text{constant}}^{I_D=\text{constant}} = I_{D0} \cdot \frac{W}{L} \cdot e^{\left(\overbrace{V_{GS}+v_{gs}}^{v_{GS}} - V_{THN}\right)/nV_T} \cdot \left(\frac{1}{nV_T}\right) \quad (9.38)$$

If, (as always for a small-signal analysis) $v_{gs} << V_{GS}$, then

$$g_m = \frac{I_D}{nV_T} \quad (9.39)$$

The transconductance increases linearly with bias current when operating in the subthreshold region (compare to Eq. (9.22)). Unfortunately, the speed (f_T) of MOSFETs operating in this region is considerably slower. The small currents charging the device's own capacitances limit the speeds to, in general, < MHz. As CMOS technology scales downwards, the inherent speeds increase. This, together with the need for lower power, increases the number of designs operating in, or near, the subthreshold region.

As I_D (V_{GS}) increases, the MOSFET moves from operating in the subthreshold region, $g_m = I_D/nV_T$ (g_m is exponentially dependent on V_{GS}), to moderate inversion, and then to the strong inversion region, $g_m = \sqrt{2I_D\beta_n} = \beta_n(V_{GS} - V_{THN})$ (g_m is linearly dependent on V_{GS}). As seen in Eq. (9.16), using small V_{DS} results in a channel resistance, R_{ch} , of $1/g_m$ (assuming that the MOSFET is operating in the *triode* region). Fig. 9.27a shows a plot of I_D against V_{GS} for a MOSFET in the short-channel process discussed later in the chapter. The threshold voltage in (a) is estimated by linearly extrapolating back to the x-axis (again from Eq. [9.16] the slope is R_{ch}^{-1}). In (b) we take the derivative of (a) to get the g_m of the device. Knowing $g_m = \beta_n(V_{GS} - V_{THN})$ (for a MOSFET operating in the *saturation* region), we can linearly extrapolate back to the x-axis to estimate when g_m goes to zero (to get V_{THN}). The two methods give different results (there are other methods as well, such as taking the derivative of g_m with respect to V_{GS} and looking at the V_{GS} [= V_{THN}] when this second derivative of I_D becomes constant). Because, even for small V_{DS} (> a couple of kT/q), the MOSFET will be operating in the saturation region when $V_{GS} \approx V_{THN}$ we'll use method (b).

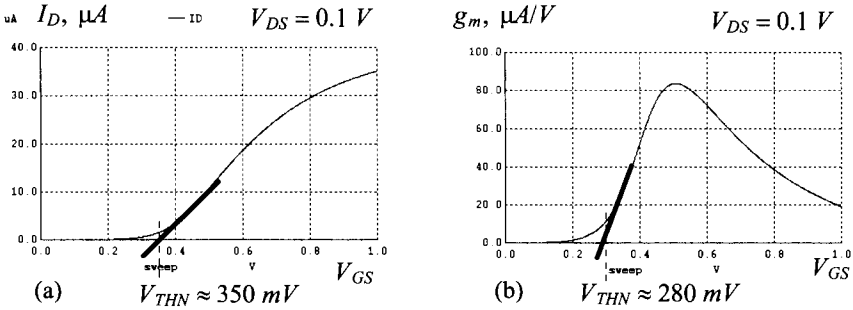


Figure 9.27 (a) Drain current plotted against gate-source voltage with small Vds and (b) transconductance plotted against gate-source voltage.

9.1.3 Temperature Effects

In this section we look at how the drain current of a MOSFET operating in the saturation region changes with temperature. Looking at the long-channel expression for the drain current

$$I_{DS,sat} = \frac{\mu_n \cdot \varepsilon_{ox}}{2t_{ox}} \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \tag{9.40}$$

(where we've written KP_n as $\mu_n\varepsilon_{ox}/t_{ox}$), the variables that change with temperature are the mobility and the threshold voltage.

Threshold Variation with Temperature

From Ch. 6, Eq. (6.17), we can write

$$V_{THN} = -V_{ms} - 2V_{fp} + \frac{Q'_{b0} - Q'_{ss}}{C'_{ox}} \tag{9.41}$$

noting Q'_{ss} is a constant and $Q'_{b0} = \sqrt{2qN_A\varepsilon_{si}|-2V_{fp}|}$. Knowing

$$V_{fp} = -\frac{kT}{q}\ln\frac{N_A}{n_i} \text{ and } V_{ms} = V_G - V_{fp} = \frac{kT}{q}\ln\frac{N_{D,poly}}{n_i} - V_{fp} \tag{9.42}$$

the change in the threshold voltage with temperature is

$$\frac{\partial V_{THN}}{\partial T} = -\frac{k}{q} \cdot \ln \frac{N_{D,poly}}{N_A} + \frac{Q'_{b0}}{C'_{ox} \cdot 2T} \approx -\frac{k}{q} \cdot \ln \frac{N_{D,poly}}{N_A} \tag{9.43}$$

The term k/q is the change in the thermal voltage with temperature, that is,

$$\frac{\partial V_T}{\partial T} = \frac{\partial}{\partial T}\left(\frac{kT}{q}\right) = \frac{k}{q} = 0.085\ mV/C^\circ \tag{9.44}$$

(keeping in mind that we don't confuse the temperature behavior of the thermal voltage, V_T, with the behavior of the threshold voltage, V_{THN}). If $N_{D,poly} = 10^{20}$ and $N_A = 10^{15}$ (a ballpark value for a long-channel MOSFET), then

$$\frac{\partial V_{THN}}{\partial T} \approx -1\ mV/C^\circ \tag{9.45}$$

If $N_A = 10^{17}$ (N_A scales upwards as the channel length of the CMOS technology decreases, see Table 6.3 in Ch. 6), then

$$\frac{\partial V_{THN}}{\partial T} \approx -0.6\ mV/C^\circ \tag{9.46}$$

noting that the threshold voltage decreases with increasing temperature, while the thermal voltage increases with increasing temperature. The temperature coefficient of the threshold voltage is defined as

$$TCV_{THN} = \frac{1}{V_{THN}} \cdot \frac{\partial V_{THN}}{\partial T} \tag{9.47}$$

so that the threshold voltage can be written as a function of temperature as

$$V_{THN}(T) = V_{THN}(T_0) \cdot (1 + TCV_{THN} \cdot (T - T_0)) \tag{9.48}$$

where the threshold voltage is measured at the temperature T_0, Fig. 9.28. The units for temperature can be Kelvin or Celsius because of the difference used in this equation. For our long-channel process with V_{THN} = 0.8 V, the temperature coefficient is −1,250 ppm/C°. For a short-channel process with V_{THN} = 0.28 V, we get a temperature coefficient of −2,143 ppm/C°. For a 100-degree increase in temperature, our short-channel threshold voltage decreases by 60 mV, resulting in a larger I_{off} (a factor of 10 larger if the subthreshold slope is the ideal 60 mV/decade at room temperature).

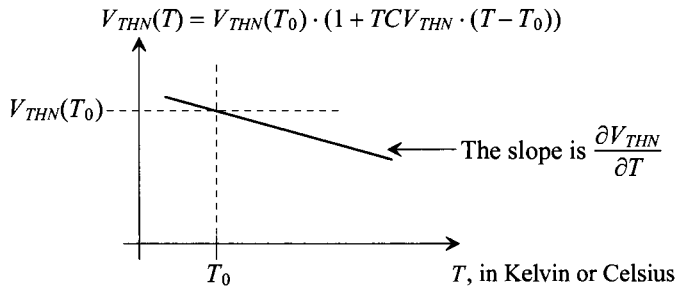


Figure 9.28 Temperature dependence of the threshold voltage.

Mobility Variation with Temperature

The reduction in mobility with increasing temperature is modeled using

$$\mu(T) = \mu(T_0) \cdot \left(\frac{T_0}{T}\right)^{1.5} \tag{9.49}$$

and so it follows that the reduction in the transconductance parameter with increasing temperature is

$$KP(T) = KP(T_0) \cdot \left(\frac{T_0}{T}\right)^{1.5} \tag{9.50}$$

where, once again, the mobility is measured at temperature T_0. Note that both T and T_0 have units of Kelvin. The change in the MOSFET transconductance parameter, KP, with temperature around T_0 is

$$\left[\frac{\partial KP(T)}{\partial T}\right]_{T_0=\text{ constant}} = KP(T_0) \cdot (-1.5)\left(\frac{T_0}{T}\right)^{2.5} \cdot \frac{1}{T_0} \tag{9.51}$$

The temperature coefficient of the transconductance parameter around the temperature T_0 is then

$$\frac{1}{KP(T)} \cdot \frac{\partial KP(T)}{\partial T} = -\frac{1.5}{T} \tag{9.52}$$

The transconductance parameter at a particular temperature close to T_0 is given by

$$KP(T) = KP(T_0) \cdot \left(1 - 1.5 \cdot \frac{T - T_0}{T}\right) \tag{9.53}$$

As temperature increases, the mobility and KP decrease. Note that our derivation used the change in the temperature (the slope of the line) around the measured temperature T_0 (just like we used for small-signal analysis). Equations (9.52) and (9.53) work well for hand calculations. However, for wide temperature changes, we'll need to use simulations (which can include the nonlinear variations in the mobility). Note, again, that unlike Eq. (9.48) where a difference in temperatures is present, and so either Kelvin or Celsius can be used, we must use Kelvin when using Eq. (9.53).

Drain Current Change with Temperature

We now know that as temperature goes up, the threshold voltage and mobility go down. A decrease in mobility, see Eq. (9.40), causes the drain current to go down. At the same time, a decrease in threshold voltage causes the drain current to go up. At low V_{GS}, the changes in V_{THN} dominate and the drain current increases with increasing temperature. At higher V_{GS}, the mobility dominates and the drain current decreases with increasing temperature. When the effects cancel, the drain current doesn't change with temperature, Fig. 9.29. For a long-channel device like the one seen in Fig. 9.29, again, $\partial V_{THN}/\partial T = -1\ mV/C°$.

Figure 9.30a shows how the drain current changes with temperature in a short-channel CMOS technology. Again, we see where the effects of the mobility changing with temperature cancel the effects of the threshold voltage changing with temperature. Looking at Fig. 9.30b, we see that, for a constant current of 10 μA, V_{GS} changes at a rate of $\approx -0.6\ mV/C°$ ($= \partial V_{THN}/\partial T$ because the V_{GS} is small).

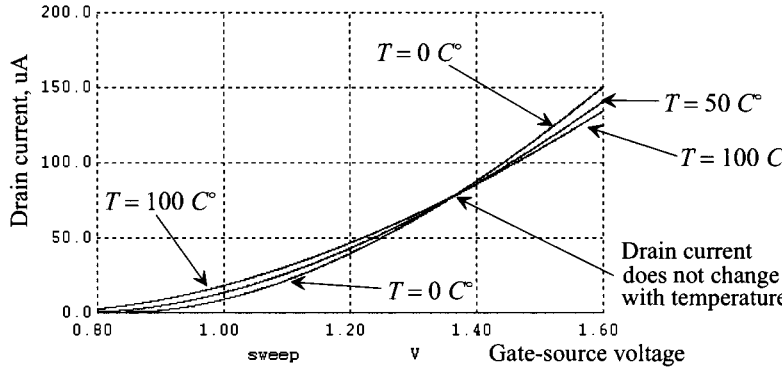
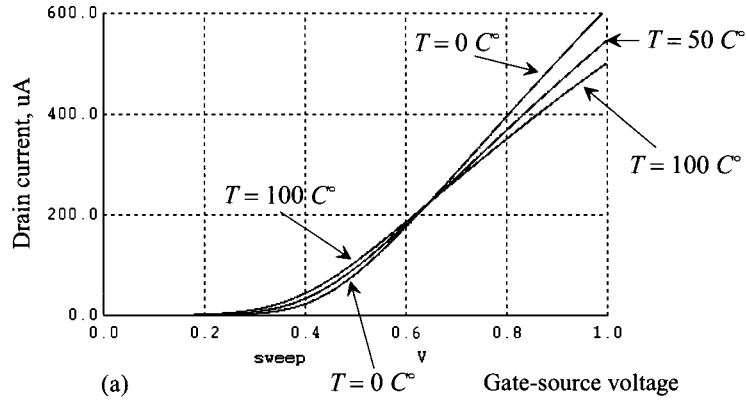
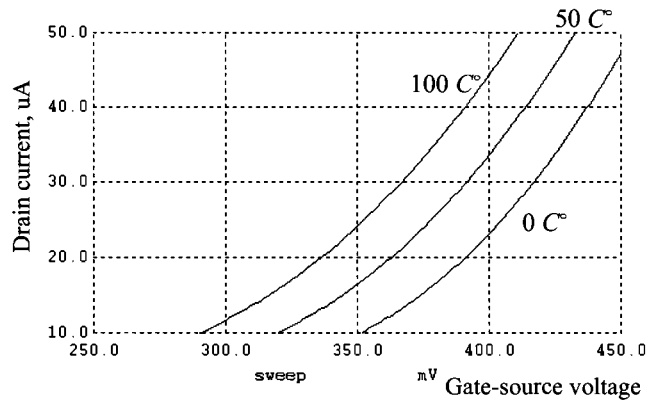


Figure 9.29 Long-channel drain current change with temperature.





(b) Zoomed-in view of (a).

Figure 9.30 Short-channel drain current change with temperature.

9.2 Short-Channel MOSFETs

The last section covered the fundamental models used for MOSFETs in analog design. In this section we use these results to help with our selection of device sizes and biasing currents to meet certain design requirements: speed, power, output or input swing, etc. Our approach is to develop plots of device parameters based on simulations that can be used when designing with short-channel MOSFETs. The CMOS process technology that we use in this section has a minimum length of 50 nm and a *VDD* of 1 V.

9.2.1 General Design (A Starting Point)

We labeled the V_{DS} where the MOSFET enters the saturation region, for a fixed V_{GS} and for either long- or short-channel MOSFETs, $V_{DS,sat}$ (Fig. 9.4). For long-channel MOSFETs this voltage was determined using Eq. (9.2), that is, $V_{GS} - V_{THN}$. However, for short-channel devices this relationship ($V_{DS,sat} = V_{GS} - V_{THN}$) isn't meaningful. For these devices, we'll call the difference between V_{GS} and V_{THN} the *gate overdrive voltage*

$$V_{ovn} = V_{GS} - V_{THN} \neq V_{DS,sat} \tag{9.54}$$

As we saw in Fig. 9.27 the threshold voltage for this 50 nm process is 280 mV. We said earlier that for general analog design we set the overdrive voltage to roughly 5% of *VDD*. We might use, as a starting point,

$$V_{ovn} = 70\ mV \rightarrow V_{GS} = 350\ mV$$

For higher speed we increase V_{ovn} at the price of reduced output swing (a higher V_{DS} is needed to move the MOSFET into saturation). Using the overdrive voltage, we can rewrite, perhaps more correctly now, Eq. (9.37) as

$$f_T = \frac{g_m}{2\pi C_{gs}} \propto \frac{V_{ovn}}{L} \tag{9.55}$$

Now we must select the biasing current and the width/length of the MOSFETs. As mentioned earlier, we use 2–5 times minimum length for general design (we use minimum length for high-speed design). As we did with the long-channel process, let's use twice minimum length (L = 2 or, with the scale factor, L = 100 nm) to get started as a good trade-off between speed and gain. To select the bias current and width, let's remember the on current for a short-channel MOSFET, from Ch. 6, is

$$i_D = v_{sat} \cdot C'_{ox} \cdot W \cdot (v_{GS} - V_{THN} - V_{DS,sat}) \tag{9.56}$$

The transconductance, following the same procedure used earlier, for a short-channel MOSFET is then

$$g_m = \left[\frac{\partial i_D}{\partial v_{GS}}\right]_{V_{GS}\ =\ \text{constant}}^{I_D\ =\ \text{constant}} = v_{sat} \cdot C'_{ox} \cdot W \tag{9.57}$$

The g_m of a short-channel device depends only on the MOSFET's width if the velocity of the carriers saturates (is a constant). Fortunately, effects such as velocity overshoot **cause g_m to increase with increases in V_{GS} or V_{DS}.** The width of the MOSFET is selected to ensure the MOSFET has enough current drive for a particular load (for a more detailed discussion see Sec. 26.1). Here we'll select a bias current of 10 μA and a g_m of 150 μA/V. As a first cut, let's use V_{ovn} = 70 mV, W = 50, and L = 2 (selected based on simulations).

Figure 9.31 shows the IV curves for a 50/2 (actual size of 2.5μm/100nm device) with a V_{GS} of 350 mV. The current shows significant variation as V_{DS} changes. Knowing I_D does change with V_{DS}, we'll still simply say the drain current is 10 μA (as an approximation).

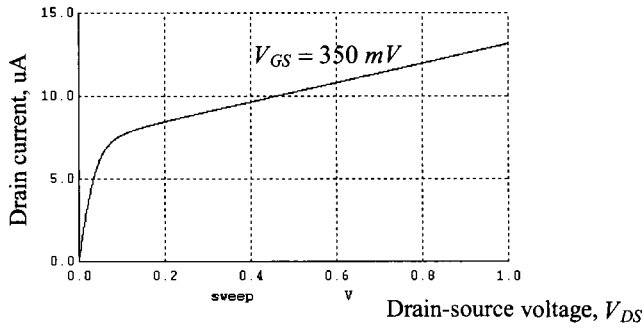


Figure 9.31 IV curves for a 50/2 NMOS with VGS = 350 mV.

Output Resistance

Figure 9.32 shows the output resistance of this 50/2 NMOS device. We get r_o by taking the reciprocal of the drain current's derivative in Fig. 9.31. To determine $V_{DS,sat}$, we can look at the point where the output resistance starts to increase. Here this is approximately 50 mV (= $V_{DS,sat}$). However, notice that if we use larger V_{DS}, we get considerably higher output resistances. This is an **important point** when we design current mirrors in Ch. 20. The lambda can be estimated using Figs. 9.31 and 9.32 as 0.6 V^{-1}.

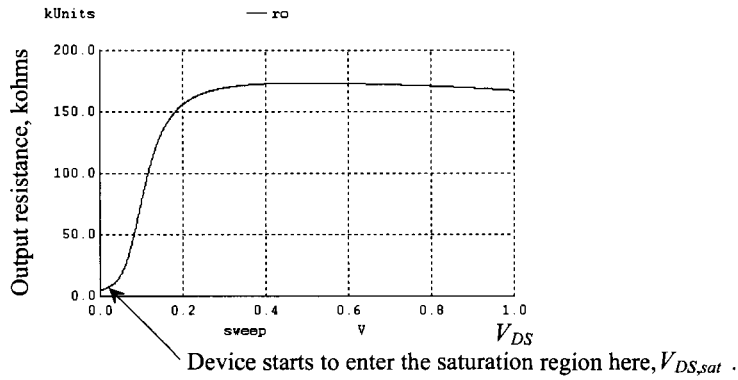


Figure 9.32 Output resistance of the MOSFET in Fig. 9.31 against V_{DS} .

Forward Transconductance

The forward transconductance, g_m , is plotted against V_{GS} in Fig. 9.33. At our V_{GS} of 350 mV (gate overdrive, V_{ovn}, of 70 mV), we get, as designed for, a g_m of 150 μA/*V*. The open circuit gain is $g_m r_o$ and is only 25. This is *considerably lower* than the open circuit gains seen in Table 9.1 for the long-channel devices and results in design "challenges" when designing with such small devices. Also notice that the g_m does change with V_{GS} , unlike

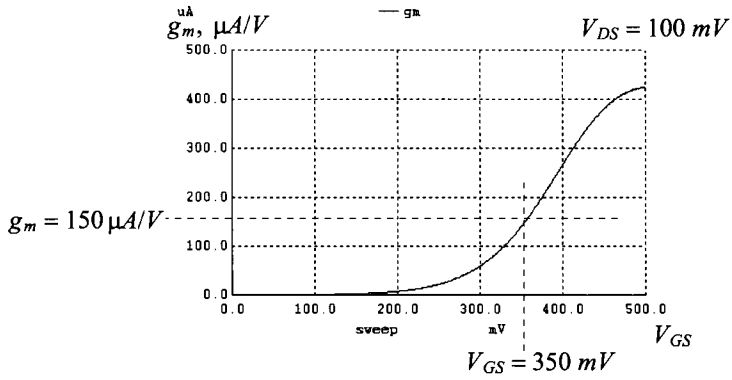


Figure 9.33 How transconductance changes with gate-source bias.

what was indicated in Eq. (9.57). This is because the saturation velocity isn't exactly constant and depends on both V_{GS} and V_{DS}.

Transition Frequency

From Fig. 9.34 we see that the transition frequency of the 50/2 NMOS is approximately 6 GHz. While the equations show that increasing the gate overdrive increases f_T, it can be educational to change the V_{GS} in the netlist and look at how the speed (f_T) changes.

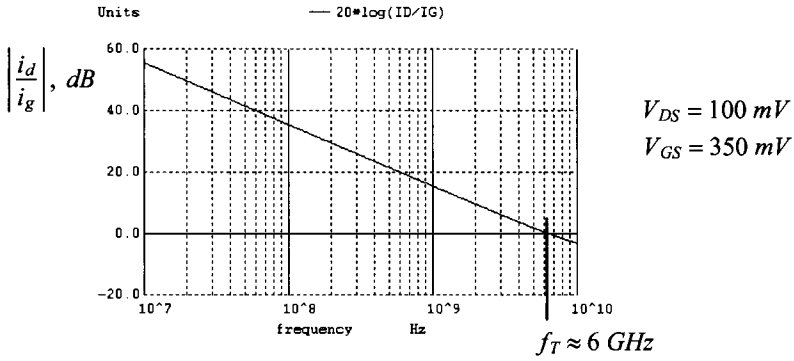


Figure 9.34 MOSFET transition frequency.

Table 9.2 shows the typical parameters for the sizes and biasing current we've used in this section. These values are a good starting point for general design. However, if the design must be either high-speed or low-power, the biasing current, device sizes, and thus overdrive voltages **will be** different from what's listed. They'll also be different with shifts in process, voltage, and temperature (PVT).

Finally, we generated the PMOS data from simulation netlists that are available at cmosedu.com. These simulation netlists are invaluable for quickly regenerating the data in Table 9.2 for different device sizes and overdrive voltages.

Table 9.2 Typical parameters for analog design using the *short-channel* CMOS process discussed in this book. These parameters are valid only for the device sizes and currents listed.

Short-channel MOSFET parameters for general analog design *VDD* = 1 V and a scale factor of **50 nm** (*scale* = 50e–9)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias current, I_D	10 μA	10 μA	Approximate, see Fig. 9.31
W/*L*	50/2	100/2	Selected based on I_D and V_{ov}
Actual *W*/*L*	2.5μm/100nm	5μm/100nm	L_{min} is 50 nm
$V_{DS,sat}$ and $V_{SD,sat}$ V_{ovn} and V_{ovp}	50 mV 70 mV	50 mV 70 mV	However, see Fig. 9.32 and the associated discussion
V_{GS} and V_{SG}	350 mV	350 mV	No body effect
V_{THN} and V_{THP}	280 mV	280 mV	Typical
$\partial V_{THN,P}/\partial T$	– 0.6 mV/C°	– 0.6 mV/C°	Change with temperature
v_{satn} and v_{satp}	110 x 10^3 m/s	90 x 10^3 m/s	From the BSIM4 model
t_{ox}	14 Å	14 Å	Tunnel gate current, 5 A/cm^2
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	25*f*F/μm^2	25*f*F/μm^2	$C_{ox} = C'_{ox}WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	6.25*f*F	12.5*f*F	PMOS is two times wider
C_{gsn} and C_{sgp}	4.17*f*F	8.34*f*F	$C_{gs} = \frac{2}{3}C_{ox}$
C_{gdn} and C_{dgp}	1.56*f*F	3.7*f*F	$C_{gd} = CGDO \cdot W \cdot scale$
g_{mn} and g_{mp}	150 μA/V	150 μA/V	At I_D = 10 μA
r_{on} and r_{op}	167 kΩ	333 kΩ	Approximate at I_D = 10 μA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	25 V/V	50 V/V	!!Open circuit gain!!
λ_n and λ_p	0.6 V^{-1}	0.3 V^{-1}	$L = 2$
f_{Tn} and f_{Tp}	6000 MHz	3000 MHz	Approximate at $L = 2$

9.2.2 Specific Design (A Discussion)

A figure-of-merit (FOM) that is useful when comparing designs with different *W*/*L*s and bias currents is the gain-f_T product (GFT) of an amplifier. The GFT of a MOSFET can be written as the product of the open-circuit gain and f_T, that is,

$$\text{GFT} = g_m r_o \cdot f_T \tag{9.58}$$

For a *long-channel* process we can write this equation (see Eqs. [9.22], [9.30], [9.32], and [9.36]) knowing $C_{gs} = \frac{2}{3}C'_{ox}WL$ as

$$\text{GFT} = g_m r_o \cdot f_T = \frac{g_m^2}{2\pi C_{gs}} \cdot \frac{1}{\lambda I_D} = \frac{3\mu_n}{2\pi \cdot L^2 \lambda} \propto \frac{\mu_n}{L} \tag{9.59}$$

Notice that this expression is *independent of drain current.* It is based entirely on the channel length and mobility of the MOSFET. This result is important because it shows that if the gain goes up, the speed (f_T) goes down. Not understanding this equation will

result in *wasted time* when trying to increase both the gain and bandwidth of an amplifier. Note that for a *short-channel* process the GFT is *dependent on mobility alone* since the f_T of the MOSFET is proportional to L, Eq. (9.55), not L^2, Eq. (9.36) (discussion below).

We know from Eq. (9.36) that increasing the drain current (or increasing V_{GS}) results in an increase in speed. But the cost for the higher speed is a reduction in the open-circuit gain. This gain can be written, for a device operating in strong inversion, as

$$g_m r_o = \frac{\sqrt{2KP_n \frac{W}{L} I_D}}{\lambda I_D} = \frac{\sqrt{2KP_n \frac{W}{L}}}{\lambda} \cdot \frac{1}{\sqrt{I_D}} \tag{9.60}$$

showing that gain decreases with increasing drain current, Fig. 9.35. We can also write, with the help of Eq. (9.32),

$$g_m r_o = \frac{KP_n \frac{W}{L}(V_{GS} - V_{THN})}{\lambda \cdot \frac{KP_n}{2} \frac{W}{L}(V_{GS} - V_{THN})^2} = \frac{2}{\lambda (V_{GS} - V_{THN})} \propto \frac{L}{V_{ovn}} \tag{9.61}$$

showing that open-circuit gain increases with increasing L or decreasing V_{GS}. When operating in the *subthreshold region* (weak inversion), we can write

$$g_m r_o = \frac{I_D}{nV_T} \cdot \frac{1}{\lambda I_D} = \frac{1}{nV_T \lambda} \tag{9.62}$$

showing that the gain is independent of drain current when the long-channel MOSFET is operating in the subthreshold region, again see Fig. 9.35.

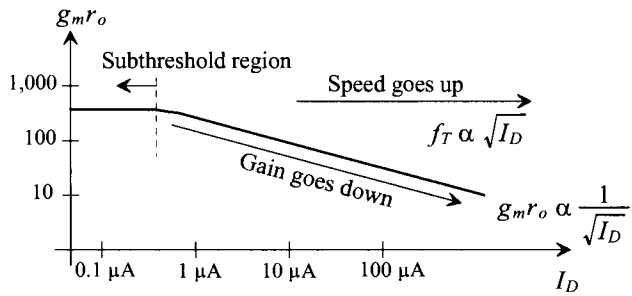


Figure 9.35 Gain falling off with bias current.

While these results were derived using long-channel models, we can use the outcomes for design in a short-channel process. For high-speed we want to use higher biasing currents and thus overdrive voltages. As the speed of the design increases, the gain falls (but, as we'll see, not at the same rate). As an example, if we decrease the width of the NMOS device used to generate Table 9.2 from 50 to 20 (using the same gate-source voltage of 350 mV), we would expect I_D to fall, f_T to remain unchanged (the device is narrower so its capacitance decreases but so does the g_m), r_o to increase, and g_m to decrease. The GFT shouldn't change much by simply reducing the width of the device. First, from Table 9.2 the GFT is

$$\overbrace{g_m r_o}^{\text{open circuit gain} = 25} \cdot f_T = 150 \frac{\mu A}{V} \cdot 167\ k\Omega \cdot 6\ GHz = 150\ GHz$$

Next, with the decrease in the device's width to 20, we get (with the help of the simulations that generated Figs. 9.31–9.34): $I_D = 4\ \mu A$ (V_{ovn} is still 70 mV), $r_o = 435\ k\Omega$, $g_m = 55\ \mu A/V$, and $f_T = 6\ GHz$. The GFT with the device width of 20 is

$$g_m r_o \cdot f_T = \overbrace{55\frac{\mu A}{V} \cdot 435\ k\Omega}^{\text{open circuit gain} = 24} \cdot 6\ GHz = 144\ GHz$$

practically no difference. If we now increase the gate-source voltage to 450 mV (almost half of *VDD*) so that the overdrive goes from 70 mV to 170 mV while using a 50/2 NMOS, we would expect the f_T to increase, g_m to increase, I_D to increase, and r_o to decrease. Again, with the help of the simulations that generated Figs. 9.31–9.34, $I_D = 45\ \mu A$ (V_{ovn} is now 170 mV), $r_o = 55\ k\Omega$, $g_m = 390\ \mu A/V$, and $f_T = 10\ GHz$. The GFT with the increased V_{ovn} is

$$g_m r_o \cdot f_T = \overbrace{390\frac{\mu A}{V} \cdot 55\ k\Omega}^{\text{open circuit gain} = 21.5} \cdot 10\ GHz = 215\ GHz$$

Using the long-channel equations, Eq. (9.59), we would expect little change (again) since the GFT doesn't depend on the overdrive voltage. However, the mobility in a short channel process does change with V_{ovn} (see g_m and velocity overshoot discussions on pages 151 and 297). By using higher gate overdrives, in a short-channel process, we can improve the GFT (and speed) of our circuits at the cost of power and overhead (the devices will triode at a higher V_{DS}) with small degradation to the gain.

Based on large GFT it might appear that it's better to design using a long-channel (older) CMOS technology rather than a short-channel (nanometer) process. The GFT, for example, of the NMOS device in Table 9.1 is 675 GHz while it's only 150 GHz for the NMOS device in Table 9.2. In addition, the open circuit gains of short-channel MOSFETs are considerably lower than long-channel MOSFETs. The smaller device, however, is better for high-speed design because its f_T is higher (it still behaves like an amplifier at high frequencies). In summary, for high-speed designs use a small process while for low-frequency designs use older CMOS (if there is a choice).

9.3 MOSFET Noise Modeling

In this section we cover modeling MOSFET noise using SPICE. It is assumed that the reader is familiar with the material presented in Ch. 8, that is, the spectral characteristics and origins of thermal and flicker noise.

Drain Current Noise Model

The noise generators in MOSFETs are due to thermal and flicker noise. The thermal noise due to the channel resistance, modeled in the saturation region using a resistor of $\frac{3}{2} \cdot \frac{1}{g_m}$ (subsitute Eq. [6.46], without the area dependence, into [6.27] and integrate) and R_{CH} in the triode region, is given, in the saturation region, by a power spectral density, PSD, of

$$I_R^2(f) = \frac{4kT}{\frac{3}{2} \cdot \frac{1}{g_m}} = \frac{8kT}{3} \cdot g_m \tag{9.63}$$

This noise current source is placed across the drain and source of the MOSFET (so the output current is the sum of the desired and undesired [noise] components).

Flicker noise (one-over-f, that is, $1/f$) results from the trapping of charges at the oxide/semiconductor interface. As indicated in Ch. 8, flicker noise is present whenever a direct current flows in a discontinuous material. The electrons jump from one location to the next while sometimes being randomly trapped and released. This trapping gives rise to a flickering in the drain current. Since the carrier lifetime in silicon is on the order of tens of microseconds (relatively long), the resulting current fluctuations are concentrated at lower frequencies. Flicker noise can be modeled in SPICE (with NLEV = 0, the default) by a PSD of

$$I_{1/f}^2(f) = \frac{KF \cdot I_D^{AF}}{f \cdot (C'_{ox} \cdot L)^2} \tag{9.64}$$

where KF is the flicker noise coefficient, a typical value is 10^{-28} $A^{2-AF}(F/m)^2$, I_D is the DC drain current, AF is the flicker noise exponent, a value ranging from 0.5 to 2 (generally very close to 1), and f is the frequency variable we integrate over. Setting NLEV = 1 in SPICE changes the L^2 term in the denominator to LW (the area of the MOSFET), that is,

$$I_{1/f}^2(f) = \frac{KF \cdot I_D^{AF}}{f \cdot (C'_{ox})^2 LW} \tag{9.65}$$

Figure 9.36 shows measured data comparing a straight-line fit to the PSD generated using this noise model. The device used to collect this data is 10 μm wide and 2.8 μm long. Note that the noise PSD was averaged 20 times and still looks jagged. The 1/f noise spectrums we drew in Ch. 8, e.g., Fig. 8.31, show smooth PSDs. We only get smooth spectrums after much averaging (it is, after all, noise).

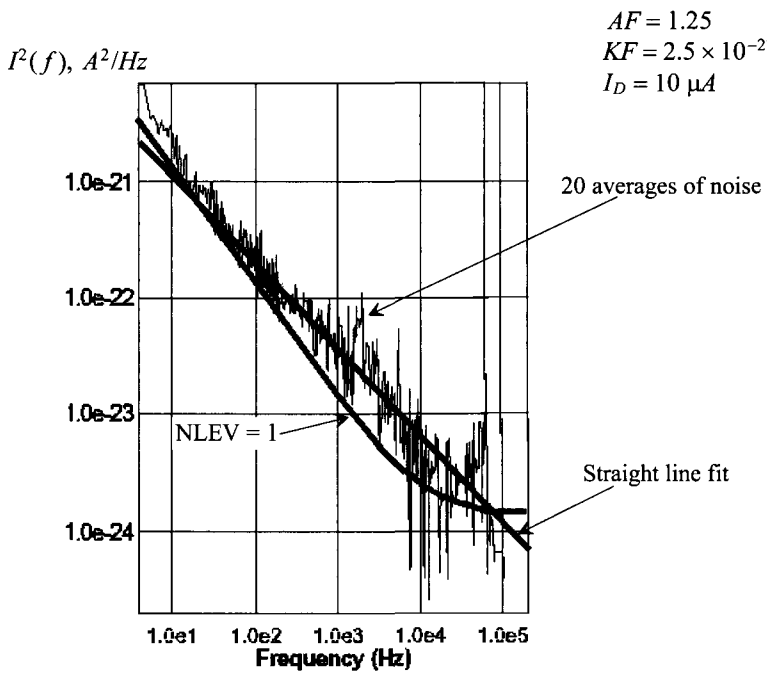


Figure 9.36 Measured MOSFET flicker noise spectrum.

The total PSD of MOSFET drain current noise (the sum of the flicker and thermal noise contributions) is given by

$$I_M^2(f) = I_{1/f}^2(f) + I_R^2(f) = \frac{KF \cdot I_D^{AF}}{f \cdot (C'_{ox})^2 LW} + \frac{8kT}{3} \cdot g_m \qquad (9.66)$$

Remembering noise is always measured on the output of a circuit and referred back to the input of a circuit so that it can be compared to the input signal, we can write (knowing $i_d = g_m v_{gs}$) the MOSFET's input-referred noise PSD as

$$V_{inoise}^2(f) = \frac{KF \cdot I_D^{AF}}{f \cdot (C'_{ox})^2 LW \cdot g_m^2} + \frac{8kT}{3g_m} \qquad (9.67)$$

Figure 9.37 shows how the noise models are added to the schematic representation of the MOSFET. Notice that increasing the MOSFET's forward transconductance, g_m, reduces the input-referred thermal noise. If the g_m is increased by making the device wider (that is, it is not increased by simply raising the drain current), then the $1/f$ noise decreases as well. Note, as discussed in Ch. 8, that looking at the (size of the) output noise alone gives no indication of the noise performance of the amplifier or circuit. The input-referred noise should be compared to the input signal for an indication of noise performance. (A notable exception to this is a circuit that doesn't have an input signal like a current mirror. In these types of circuits we *do* care about reducing the size of the output noise.)

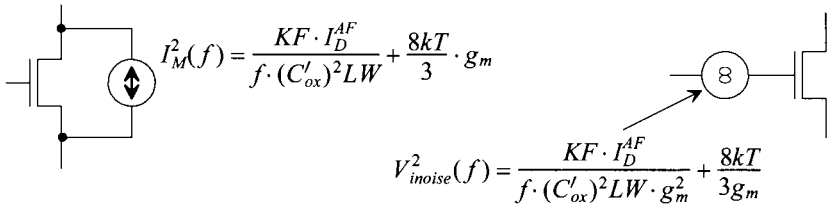


Figure 9.37 (a) Modeling MOSFET noise current and (b) input-referred noise voltage.

Finally, we might ask if it is better to use a PMOS or NMOS device for low-noise design? In the older CMOS technologies, say 350 nm and earlier technology nodes, n-type polysilicon was used to form the gates of both NMOS and PMOS devices (single workfunction gates, see page 191). This keeps the PMOS device's channel from forming at the surface directly under the gate oxide. Instead a *buried channel* is formed in the device. By avoiding conduction at the oxide/semiconductor surface we also avoid the trapping and random release of carriers that is a major component of the MOSFET's drain current flicker noise. The result is the PMOS devices in the older CMOS processes have considerably better noise performance than the NMOS devices. In modern CMOS n-type polysilicon is used to form the gate of the NMOS device and p-type polysilicon is used for the gate of the PMOS (dual workfunction gates and why the polysilicon must be silicided, that is, so the connection between the p-type and n-type polysilicon isn't rectifying). The result is that both devices utilize a surface channel so the benefit of using PMOS devices is gone. The larger g_m of the NMOS makes it the preferable device for low noise design (however, this is process dependent).

ADDITIONAL READING

Textbooks Covering Small-Signal Analysis

[1] R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design*, 4th ed., McGraw-Hill Publishers, 2011. ISBN 978-0-07-338045-2.

[2] R. Spencer and M. Ghausi, *Introduction to Electronic Circuit Design*, Prentice-Hall Publishers, 2003. ISBN 0-201-36183-3.

[3] D. J. Comer and D. T. Comer, *Fundamentals of Electronic Circuit Design*, John Wiley and Sons, 2002. ISBN 0-471-41016-0.

[4] D. A. Neamen, *Electronic Circuit Analysis and Design*, McGraw-Hill Publishers, 2001. ISBN 0-072-45194-7.

[5] A. R. Hambley, *Electronics*, Prentice-Hall Publishers, 2nd ed, 2000. ISBN 0-136-91982-0.

[6] M. H. Rashid, *Microelectronic Circuits: Analysis and Design*, Brookes-Cole Publishing, 1998. ISBN 0-534-95174-0.

[7] A. Sedra and K. Smith, *Microelectronic Circuits*, Oxford University Press, 4th ed., 1998. ISBN 0-195-11663-1.

[8] R. T. Howe and C. G. Sodini, *Microelectronics: An Integrated Approach*, Prentice-Hall Publishers, 1997. ISBN 0-135-88518-3.

[9] N. Malik, *Electronic Circuits: Analysis, Simulation, and Design*, Prentice-Hall Publishers, 1995. ISBN 0-023-74910-5.

[10] M. N. Horenstein, *Microelectronic Circuits and Devices*, Prentice-Hall Publishers, 2nd ed., 1990. ISBN 0-135-83170-9.

[11] M. S. Roden, G. L. Carpenter, and C. J. Savant, *Electronic Design: Circuits and Systems*, Pearson Benjamin Cummings Publishers, 2nd ed, 1990.

[12] J. Millman and A. Grabel, *Microelectronics*, McGraw-Hill Publishers, 2nd ed. 1987. ISBN 0-070-42330-X.

Textbooks Covering Noise Analysis

[13] F. Bonani and G. Ghione, *Noise in Semiconductor Devices: Modeling and Simulation*, Springer-Verlag Publishers, 2002. ISBN 3-540-66583-8.

[14] C. D. Motchenbacher and J. A. Connelly, *Low-Noise Electronic System Design*, John Wiley and Sons, 1993. ISBN 0-471-57742-1.

[15] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, John Wiley and Sons, 1980. ISBN 0-471-03018-X.

A Good Paper on the Origins of Flicker Noise

[16] Reimbold, G., "Modified 1/f Trapping Noise Theory and Experiments in MOS Transistors Biased from Weak to Strong Inversion - Influence of Interface States," *IEEE Transactions on Electron Devices*, vol. ED-31, no. 9, pp. 1190–1198, September, 1984.

PROBLEMS

For the following problems use the long-channel process information given in Table 9.1 for KP, V_{TH}, and C'_{ox}, unless otherwise indicated.

9.1 Calculate and simulate the values of I_D and V_{GS} in the following circuit.

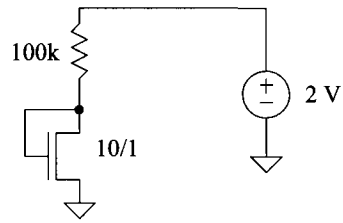


Figure 9.38 Circuit used in Problem 9.1

9.2 Repeat Problem 9.1 if the MOSFET size is changed to 10/10.

9.3 Calculate and simulate the values of I_D and V_{SG} in the following circuit.

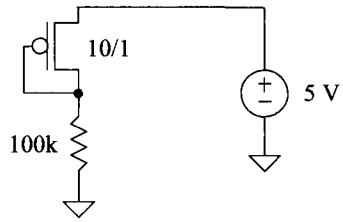


Figure 9.39 Circuit used in Problem 9.3

9.4 Repeat Problem 9.3 if the MOSFET size is changed to 10/10.

9.5 Calculate I_D, V_{DS}, and estimate the small-signal resistance looking into the drain of the MOSFET in the following circuit.

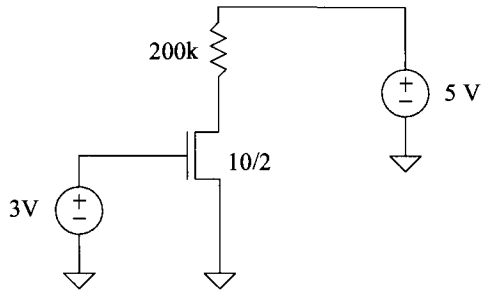


Figure 9.40 Circuit used in Problem 9.5

9.6 To determine the value of a small-signal resistance in a simulation, the circuit seen in Fig. 9.41 is used. The ratio of the test voltage, v_T, to the current that flows in the source, i_T, that is, v_T/i_T, is the small signal resistance. Using this circuit determine, with SPICE, the value of the resistance looking into the drain of the circuit in Fig. 9.40. How does the 200k resistor affect i_T in the simulation?

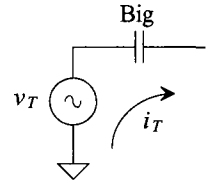


Figure 9.41 Using a test voltage to determine a resistance in a simulation.

9.7 Explain qualitatively what happens to V_{GS4} and V_{DS4} in Fig. 9.42 as the bias current is increased.

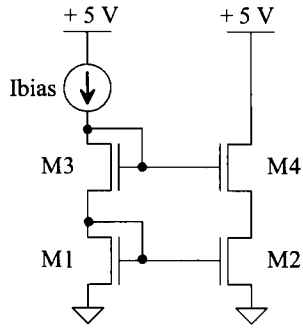


Figure 9.42 Schematic for Problem 9.7.

9.8 Describe qualitatively what happens if we steal or inject a current at the point indicated in Fig. 9.43. How does this affect the operation of M1 and M2? Verify your answer with SPICE.

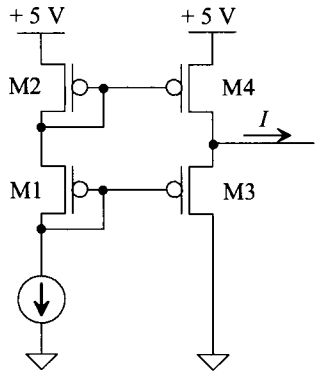


Figure 9.43 Schematic for Problem 9.8.

9.9 Using simulations, generate the plot seen in Fig. 9.12 for both NMOS and PMOS devices.

9.10 Design a circuit that will linearly convert an input voltage that ranges from 0 to 4V into a current that ranges from roughly 50 μA to 0. Simulate the operation of the design showing the linearity of the voltage-to-current conversion. How does the MOSFET's length affect the linearity?

9.11 Using a PMOS device, discuss and show with simulations how it can be used to implement a 10k resistor. Are there any limitations to the voltage across the PMOS resistor? Explain.

9.12 Using SPICE (and ensuring the MOSFET is operating in the saturation region with sufficient V_{DS}), generate the i_D versus v_{GS} curve seen in Fig. 9.15. Using SPICE take the derivative of i_D (e.g., "plot deriv(ID)") to get the device's g_m (versus V_{GS}). How does the result compare to Eq. (9.22)? Does the level 3 model used in the simulation show a continuous change from subthreshold to strong inversion?

9.13 Estimate the AC, i_d , drain current that flows in the circuit seen in Fig. 9.44. Verify your answer with SPICE in using both transient and AC simulations.

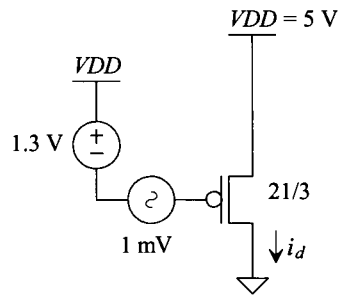


Figure 9.44 Schematic for Problem 9.13.

9.14 Calculate the DC and AC voltages and currents for the circuit seen in Fig. 9.45. Verify your answers with a SPICE AC analysis simulation.

9.15 Repeat Problem 9.14 if the bias current is reduced to 20 μA.

9.16 Using SPICE (and zero volt sources), verify the drain currents calculated in Ex. 9.5. Show both your AC analysis and transient analysis simulation results.

9.17 Using SPICE, generate the i_D versus v_{SB} curve seen in Fig. 9.21.

9.18 Repeat Ex. 9.6 if the widths and lengths of the PMOS and NMOS devices are multiplied by 10 (that is the NMOS is now 100/20 and the PMOS is now 300/20). How does the drain current change?

9.19 Compare the f_T of a 10/2 NMOS to a 100/20 NMOS. Verify your hand calculations using simulations.

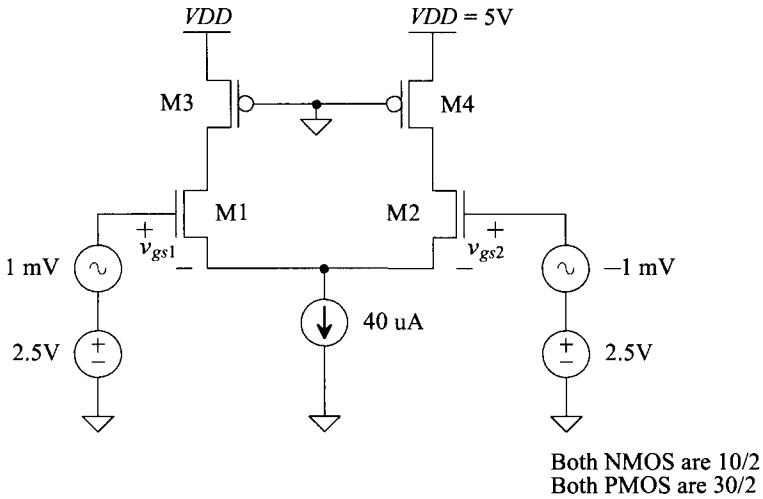


Figure 9.45 Circuit used in Problem 9.14.

9.20 Equation (9.39) is used to calculate the forward transconductance of a MOSFET operating in the subthreshold region. Is it possible to have subthreshold operation when I_D is 100 μA? If so, how?

9.21 Using the simulations that generated Fig. 9.27, estimate the threshold voltage for 50/5 PMOS and NMOS devices (both in the short-channel CMOS process).

9.22 Show the details leading to Eq. (9.43). Show, as an example, that the approximation is valid if $Q'_{b0}/C'_{ox} = 30\,mV$. (Remember: temperature is in Kelvin.)

9.23 For the circuits seen in Fig. 9.46, estimate both the output voltage at room temperature and how it will change with temperature. Verify your answer with SPICE. Use the short-channel CMOS process.

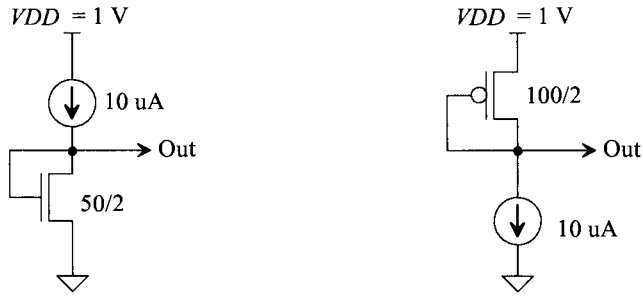


Figure 9.46 Circuits for Problem 9.23.

9.24 Verify, using simulations, the result given in Eq. (9.59), that is, that the GFT of a long-channel process is independent of biasing conditions. Make sure that the MOSFET is biased away from the subthreshold and triode regions.

9.25 When Eq. (9.36) was derived it was assumed that $C_{gs} >> C_{gd}$. Looking at the data in Table 9.2, is this a good assumption? Compare the hand-calculated value of f_T to the simulation results in Table 9.2.

9.26 Using the short-channel parameters in Table 9.2, calculate the drain voltage of M1 and its drain current (both AC and DC components) for the circuit seen in Fig. 9.47.

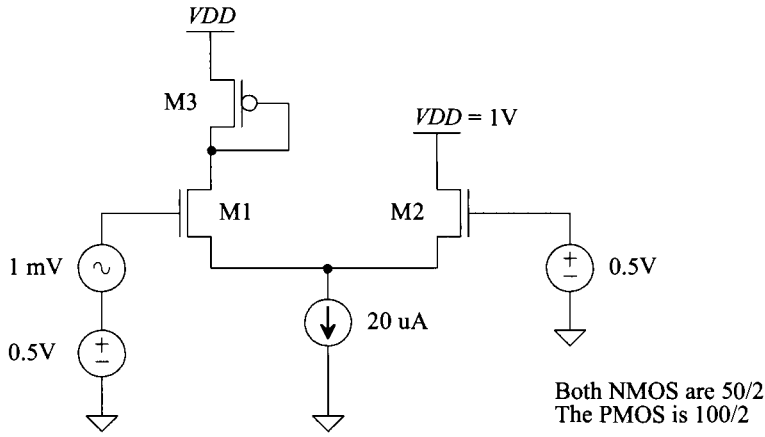


Figure 9.47 Circuit used in Problem 9.26.

9.27 What is the PSD of a MOSFET's thermal noise when it is operating in the triode region?

9.28 Looking at Eq. (9.66), we see that decreasing the MOSFET's g_m reduces the MOSFET's drain current noise PSD. If the MOSFET is to be used as an amplifier where the input signal is on the MOSFET's gate, is reducing g_m a good idea? Why or why not?

9.29 Show how the thermal noise resistance of the channel seen in Eq. (9.63) is derived for the MOSFET operating in the saturation region.