Chapter

11

The Inverter

The CMOS inverter is a basic building block for digital circuit design. As Fig. 11.1 shows, the inverter performs the logic operation of A to $\overline{A}$. When the input to the inverter is connected to ground, the output is pulled to *VDD* through the PMOS device M2 (and M1 shuts off). When the input terminal is connected to *VDD*, the output is pulled to ground through the NMOS device M1 (and M2 shuts off). The CMOS inverter has several important characteristics that are addressed in this chapter: for example, its output voltage swings from *VDD* to ground unlike other logic families that never quite reach the supply levels. Also, the static power dissipation of the CMOS inverter is practically zero, the inverter can be sized to give equal sourcing and sinking capabilities, and the logic switching threshold can be set by changing the size of the device.

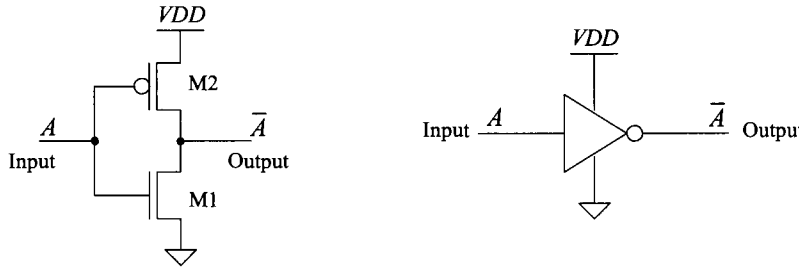

Figure 11.1 The CMOS inverter, schematic, and logic symbol.

11.1 DC Characteristics

Consider the inverter shown in Fig. 11.2 and the associated transfer characteristic plot. In region 1 of the transfer characteristics, the input voltage is sufficiently low (typically less than the threshold voltage of M1), so that M1 is off and M2 is on ($V_{SG} >> V_{THP}$). As V_{in} is increased, both M2 and M1 turn on (region 2). Increasing V_{in} further causes M2 to turn off and M1 to fully turn on, as shown in region 3.

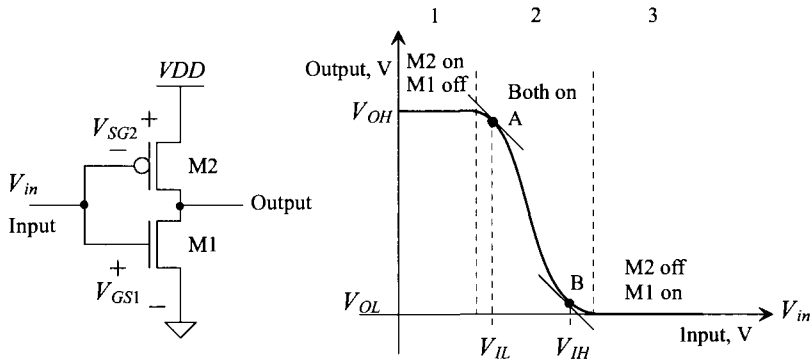

Figure 11.2 The CMOS inverter transfer characteristics.

The maximum output "high" voltage is labeled V_{OH} and the minimum output "low" voltage, V_{OL}. Points A and B on this curve are defined by the slope of the transfer curves equaling –1. Input voltages less than or equal to the voltage V_{IL}, defined by point A, are considered a logic low on the input of the inverter. Input voltages greater than or equal to the voltage V_{IH}, defined by point B, are considered a logic high on the input of the inverter. Input voltages between V_{IL} and V_{IH} do not define a valid logic voltage level. Ideally, the difference in V_{IL} and V_{IH} is zero; however, this is never the case in real logic circuits.

Example 11.1

Using SPICE, plot the transfer characteristics for the inverter seen in Fig. 11.3 in both the long- and short-channel CMOS processes used in this book. From the plot, determine V_{IH}, V_{IL}, V_{OH}, and V_{OL}.

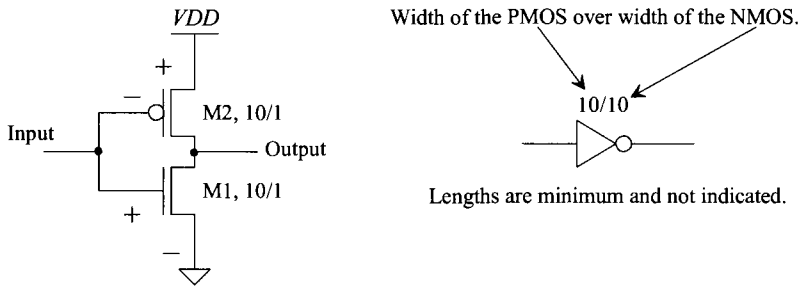

Figure 11.3 Inverter used in Ex. 11.1.

The inverter *voltage transfer curves* (VTCs) are shown in Fig. 11.4. Notice how the *VDD* used for the long-channel process is 5 V, while the *VDD* used in the short-channel, process is 1 V. The output high voltage, V_{OH}, is *VDD* and the output low voltage, V_{OL}, is ground (for both inverters). For the inverter using the

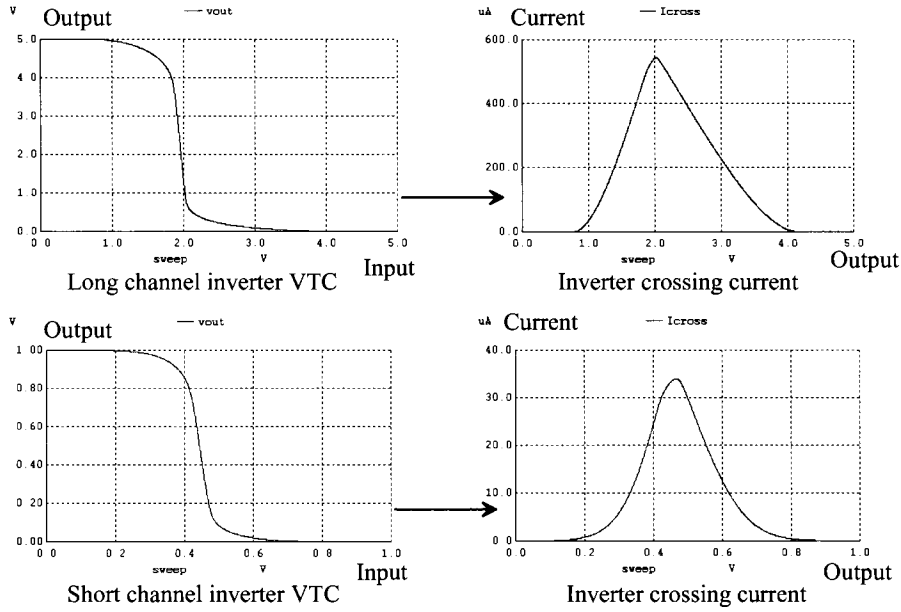

Figure 11.4 Voltage transfer curves (VTCs) for a long and a short channel inverter.

long-channel process, V_{IL} is approximately 1.8 V while, when using the short-channel process, V_{IL} is approximately 400 mV. For V_{IH} we get 2.1 V and 500 mV for the long- and short-channel processes, respectively.

Note that in Fig. 11.4 we also plotted the crossing current (the inverter's output voltage crossing between a logic 1 and a logic 0). This is the current that flows when the inverter is operating in region 2 in Fig. 11.2 (the inverter's input transitioning from a high to a low or from a low to a high). If the inverter's input transitions quickly, the amount of charge pulled from *VDD* (the amount of time the inverter is operating in region 2) is small. However, if the inverter's input logic signal transitions slowly or the logic levels don't swing all the way to the power supply rails (like what we get with the pass gates discussed in the last chapter, see Fig. 10.19), it's possible for a significant current to flow through the inverter (important!) ■

Noise Margins

The noise margins of a digital gate or circuit indicate how well the gate will perform under noisy conditions. The noise margin for the high logic levels is given by

$$NM_H = V_{OH} - V_{IH} \tag{11.1}$$

and the noise margin for the low logic levels is given by

$$NM_L = V_{IL} - V_{OL} \tag{11.2}$$

For $VDD = 1$ V, the ideal noise margins are 500 mV; that is, $NM_L = NM_H = VDD/2$.

Inverter Switching Point

Consider the transfer characteristics of the basic inverter as shown in Fig. 11.5. Point C corresponds to the point on the curve when the input voltage is equal to the output voltage. At this point, the input (or output) voltage is called the *inverter switching point voltage*, V_{SP}, and both MOSFETs in the inverter are in the saturation region. Since the drain current in each MOSFET must be equal, the following is true:

$$\frac{\beta_n}{2}(V_{SP} - V_{THN})^2 = \frac{\beta_p}{2}(VDD - V_{SP} - V_{THP})^2 \tag{11.3}$$

Solving for V_{SP} gives

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{THN} + (VDD - V_{THP})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \tag{11.4}$$

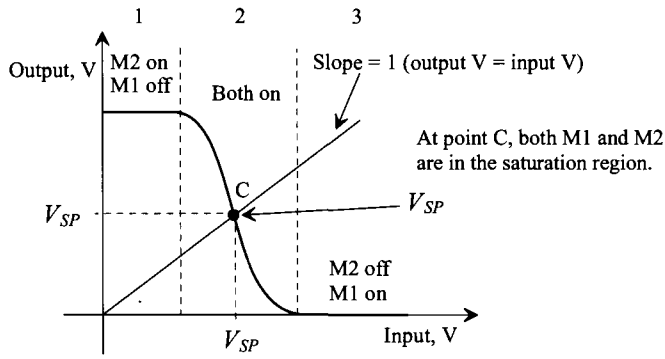

Figure 11.5 Transfer characteristics of the inverter showing the switching point.

Ideal Inverter VTC and Noise Margins

The ideal voltage transfer curves for an inverter are seen in Fig. 11.6. The ideal switching point voltage, V_{SP}, is *VDD*/2. As seen in Eqs. (11.1) and (11.2), this makes the noise margins equal to ensure the best performance (a noise margin, say the logic low level, isn't improved at the cost of the other margin). When looking at Fig. 11.6, notice that, unlike what is seen in Fig. 11.5, the inverter never operates where both MOSFETs are on. The input to the inverter is recognized as either a 1 or a 0.

Example 11.2

Estimate β_n and β_p so that the switching point voltage of a CMOS inverter designed in the long-channel CMOS process is 2.5 V (= *VDD*/2).

Solving Eq. (11.4) with V_{SP} = 2.5 V for the ratio β_n/β_p gives a value of approximately unity. That is,

$$\beta_n = \beta_p = KP_n \frac{W_1}{L_1} = KP_p \frac{W_2}{L_2}$$

Since $KP_n = 3KP_p$, the width of the PMOS device must be three times the width of the NMOS, assuming equal-length MOSFETs. For $V_{SP} = 2.5$ V, this requires

$$W_2 = 3W_1$$

which is also the requirement for making $R_n = R_p$. This is an important practical result. It shows how the electron and hole mobilities are related to both the effective switching resistances and the switching point voltage. As seen in Table 10.2, we often increase the widths of the PMOS devices to try to center V_{SP} and equate the propagation delays (the pull-up resistance, R_p , is the same as the pull-down resistance R_n). ■

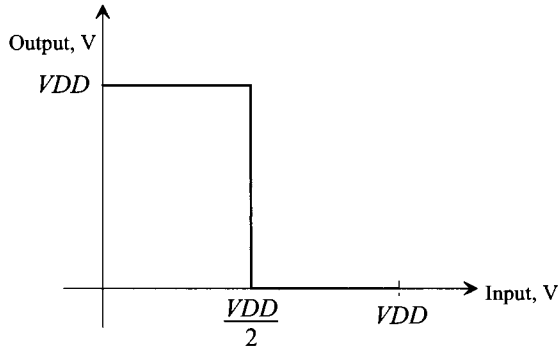

Figure 11.6 Ideal VTCs for the inverter.

Example 11.3

Show, using SPICE, that the inverter seen in Fig. 11.7 and implemented in the short-channel CMOS process has a switching point voltage close to the ideal value of *VDD*/2. Comment on the sizes of the devices.

The simulation results are seen (also) in Fig. 11.7. Because we've sized the width of the PMOS to twice the width of the NMOS (see Table 10.2), the switching point is close to the ideal value of *VDD*/2. We know that short-channel devices don't follow the square-law models and so we can't use Eq. [11.4] to calculate the V_{SP} in our 50 nm process. We can, however, get a good estimate using the effective switching resistances as seen in the figure (a voltage divider). When $R_p = R_n$, the switching point voltage is close to ideal. By changing the widths of the devices, we can adjust the switching point voltage. In other words, for a short-channel CMOS process we can use

$$V_{SP} = VDD \cdot \frac{R_n}{R_n + R_p} \tag{11.5}$$

to estimate V_{SP}. This equation does have limitations. For example, if $R_n >> R_p$, then this equation indicates V_{SP} is *VDD*. However, we know that V_{SP} has to be

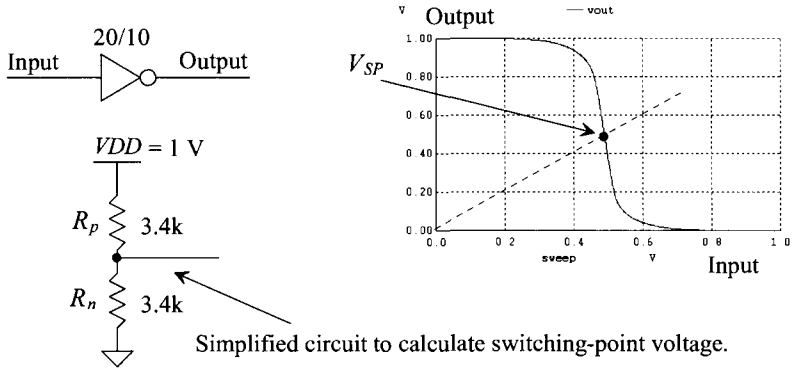

Figure 11.7 Switching point voltage for an inverter in the short-channel process.

greater than V_{THN} and less than $VDD - V_{THP}$ (make sure that this is understood). ■

Example 11.4

Show, using SPICE and the long-channel process, the transfer curves for the CMOS inverter with transconductance ratios β_n/β_p of 3, 1, and 1/3. Explain what changing the inverter ratio does to the transfer characteristics.

The simulation results are seen in Fig. 11.8. For all three DC sweeps the MOSFET's lengths are 1. For the case when $\beta_n/\beta_p = 1$, the $W_n = 10$ and $W_p = 30$. For the case when $\beta_n/\beta_p = 3$, the $W_n = 10$ and $W_p = 10$, etc. Increasing the strength of the NMOS (increasing the NMOS's width, which decreases R_n) causes the switching point voltage to decrease. We also get a decrease in V_{SP} by decreasing the strength of the PMOS device (which increases R_p). ■

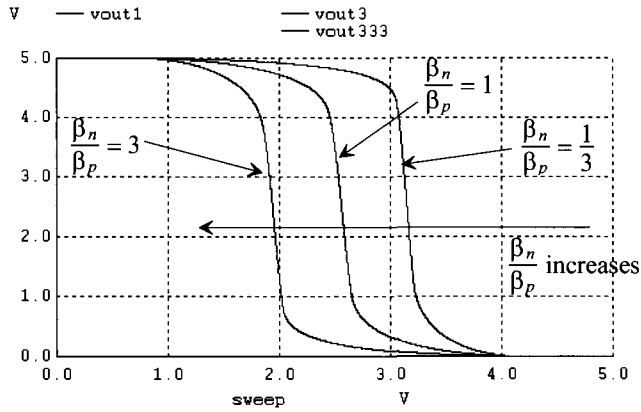

Figure 11.8 Sizing the inverter changes the switching point voltages.

11.2 Switching Characteristics

The switching behavior of the inverter can be generalized by examining the parasitic capacitances and resistances associated with the inverter. Consider the inverter shown in Fig. 11.9 with its equivalent digital model. Although the model is shown with both switches open, in practice one of the switches is closed, keeping the output connected to *VDD* or ground. The effective input capacitance of the inverter is

$$C_{in} = \frac{3}{2}(C_{ox1} + C_{ox2}) = C_{inn} + C_{inp} \tag{11.6}$$

The effective output capacitance of the inverter is simply

$$C_{out} = C_{ox1} + C_{ox2} = C_{outn} + C_{outp} \tag{11.7}$$

The intrinsic propagation delays of the inverter are

$$t_{PLH} = 0.7 \cdot R_{p2} \cdot C_{out} \text{ and } t_{PHL} = 0.7 \cdot R_{n1} \cdot C_{out} \tag{11.8}$$

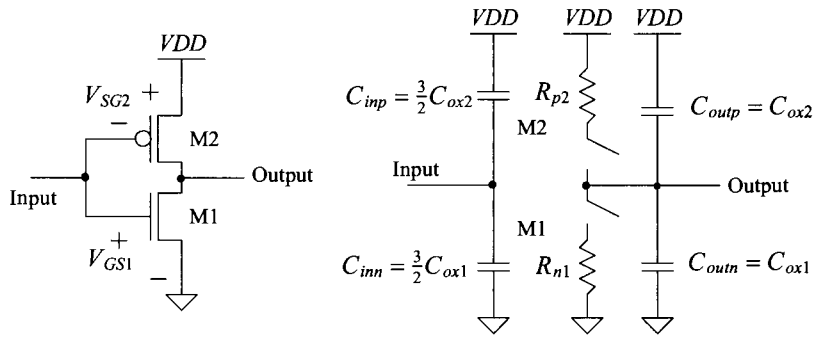

Figure 11.9 The CMOS inverter switching characteristics using the digital model.

Example 11.5

Estimate and simulate the intrinsic propagation delays of the inverter seen in Fig. 11.7. Estimate the inverter's input capacitance.

From the data in Table 10.2 and Eqs. (11.6) to (11.8), we can write

$$t_{PHL} = t_{PLH} = 0.7 \cdot 3.4k \cdot (0.625 + 1.25)\,fF = 4.5\,ps$$

The simulation results are seen in Fig. 11.10. The intrinisic delays are considerably larger than this calculation (around 20 ps).

Using Eq. (11.6), the inverter's input capacitance is

$$C_{in} = \frac{3}{2}(0.625 + 1.25)\,fF = 2.8\,fF$$

Sizing up the width of the PMOS so that its effective resistance is equal to R_n has the unwanted effect of increasing the inverter's input capacitance. ■

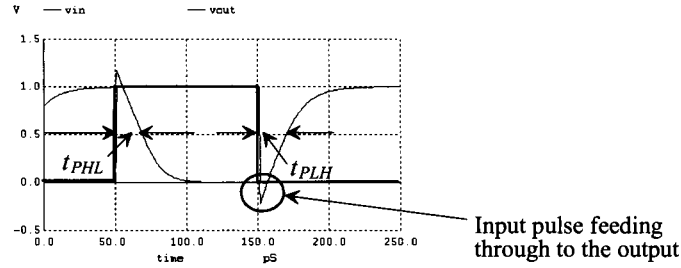

Figure 11.10 The intrinsic propagation delays of an inverter.

The propagation delays for an inverter driving a capacitive load are

$$t_{PLH} = 0.7 \cdot R_{p2} \cdot C_{tot} = 0.7 \cdot R_{p2} \cdot (C_{out} + C_{load}) \tag{11.9}$$

and

$$t_{PHL} = 0.7 \cdot R_{n1} \cdot C_{tot} = 0.7 \cdot R_{n1} \cdot (C_{out} + C_{load}) \tag{11.10}$$

where C_{tot} is the total capacitance on the output of the inverter, that is, the sum of the output capacitance of the inverter, any capacitance of interconnecting lines, and the input capacitance of the following gate(s).

Example 11.6

Estimate and simulate the propagation delays for the circuit seen in Fig. 11.11. Use the 50 nm CMOS process.

Because the load capacitance is much larger than the output capacitance of the inverter, we can rewrite

$$t_{PLH} = 0.7 \cdot R_{p2} \cdot C_{tot} \approx 0.7 \cdot R_{p2} \cdot C_{load} = 120\,ps$$

and

$$t_{PHL} = 0.7 \cdot R_{n1} \cdot C_{tot} \approx 0.7 \cdot R_{n1} \cdot C_{load} = 120\,ps$$

The simulation results are seen in Fig. 11.11. Notice that we are treating the MOSFETs used in the digital circuits as resistors and calculating the delays with a simple product of these resistors with the load capacitance. ■

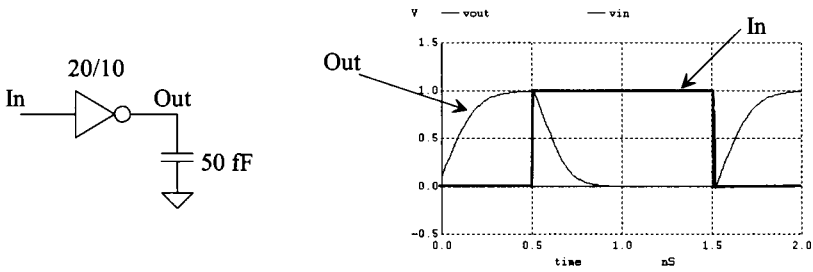

Figure 11.11 The delay associated with an inverter driving a 50 fF load.

The Ring Oscillator

The odd number of inverters in the circuit shown in Fig. 11.12 forms a closed loop with positive feedback and is called a ring oscillator. The oscillation frequency is given by

$$f_{osc} = \frac{1}{n \cdot (t_{PHL} + t_{PLH})} \tag{11.11}$$

assuming that the inverters are identical and n is the number (odd) of inverters in the ring oscillator. Since the ring oscillator is self-starting, it is often added to a test portion of a wafer to indicate the speed of a particular process run. The sum of the high-to-low and low-to-high delays is used to calculate the period of the oscillation because each inverter switches twice during a single oscillation period.

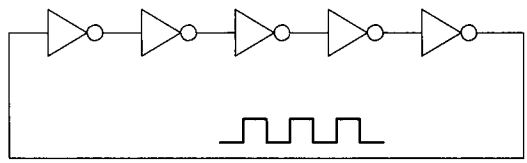

Figure 11.12 A five-stage ring oscillator.

When identical inverters are used the capacitance on the inverter's input/output is the sum of an inverter's input capacitance with the inverter's output capacitance, see Fig. 11.9, or

$$C_{tot} = \overbrace{C_{oxp} + C_{oxn}}^{C_{out}} + \overbrace{\frac{3}{2} \cdot (C_{oxp} + C_{oxn})}^{C_{in}} = \frac{5}{2} \cdot (C_{oxp} + C_{oxn}) \tag{11.12}$$

where, again, $C_{oxp} = C'_{ox} \cdot W_p \cdot L_p \cdot (scale)^2$ and $C_{oxn} = C'_{ox} \cdot W_n \cdot L_n \cdot (scale)^2$. The delay is then calculated using

$$t_{PHL} + t_{PLH} = 0.7 \cdot (R_n + R_p) \cdot C_{tot} \tag{11.13}$$

Dynamic Power Dissipation

Consider the CMOS inverter driving a capacitive load shown in Fig. 11.13. Each time the inverter changes states, it must either supply a charge to C_{tot} or sink the charge stored on C_{tot} to ground. If a square pulse is applied to the input of the inverter with a period T and frequency, f_{clk}, the average amount of current that the inverter must pull from *VDD*, recalling that current is being supplied from *VDD* only when the PMOS device is on, is

$$I_{avg} = \frac{Q_{Ctot}}{T} = \frac{VDD \cdot C_{tot}}{T} \tag{11.14}$$

The average dynamic power dissipated by the inverter is

$$P_{avg} = VDD \cdot I_{avg} = \frac{C_{tot} \cdot VDD^2}{T} = C_{tot} \cdot VDD^2 \cdot f_{clk} \tag{11.15}$$

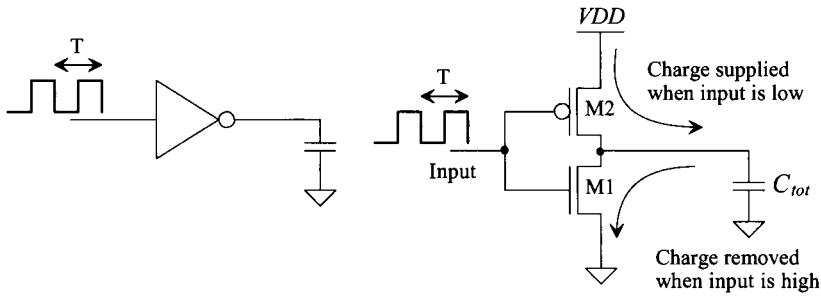

Figure 11.13 Dynamic power dissipation of the CMOS inverter.

Notice that the power dissipation is a function of the clock frequency, power supply voltage, and load capacitance. A great deal of effort is put into reducing the power dissipation in CMOS circuits. One of the major advantages of dynamic logic (Ch. 14) is its lower power dissipation.

To characterize the speed of a digital process, a term called the power delay product *(PDP)* is often used. The *PDP,* measured in Joules, is defined by

$$PDP = P_{avg} \cdot (t_{PHL} + t_{PLH}) \tag{11.16}$$

These terms can be determined from a ring oscillator. The *PDP* is frequently used to compare different technologies or device sizes; for example, a GaAs process can be compared with a 50 nm CMOS process. Although the GaAs process may have a lower propagation delay, the power dissipation may be larger and result in a larger *PDP.*

Example 11.7

Estimate the oscillation frequency of an 11-stage ring oscillator in the 50 nm process using the inverter seen in Fig. 11.7 (see Table 10.2). Verify the estimate with simulations.

Using the data in Table 10.2 and Eqs. (11.11) – (11.13), we can write

$$C_{tot} = \frac{5}{2} \cdot (1.25 + 0.625)\,fF = 4.7\,fF$$

and

$$t_{PHL} + t_{PLH} = 0.7 \cdot (3.4k + 3.4k) \cdot 4.7\,fF = 22\,ps$$

For an 11-stage ring oscillator, we get an oscillation frequency of

$$f_{osc} = \frac{1}{11 \cdot (22\,ps)} = 4.1\ GHz$$

The simulation results are seen in Fig. 11.14. The simulated oscillation frequency is close to 1.25 GHz or considerably different from our hand calculations (as will be the case when delays are close to the intrinsic values). The average power, P_{avg}, dissipated by a single inverter in this ring oscillator, using Eq. (11.15), is estimated as 19.6 μW. The PDP for the 50 nm process is then 431×10^{-18} *J*. ■

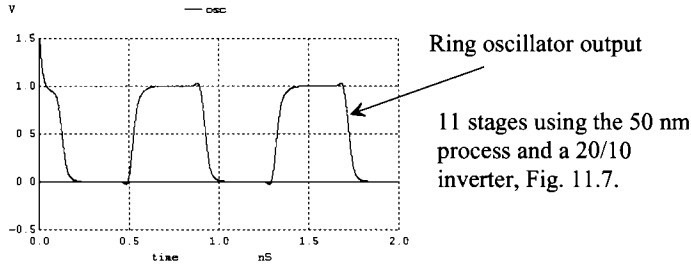

Figure 11.14 Oscillation frequency for the ring oscillator described in Ex. 11.7.

11.3 Layout of the Inverter

If care is not taken when laying out CMOS circuits, the parasitic devices present can cause a condition known as latch-up. Once latch-up occurs, the inverter output will not change with the input; that is, the output may be stuck in a logic state. To correct this problem, the power must be removed. Latch-up is especially troubling in output driver circuits.

Latch-Up

Figure 11.15 illustrates two methods of laying out an inverter. Notice how the cell's inputs and outputs are on metal2, while the power and ground conductors are routed on metal1 in the standard cell frame (see Fig. 4.15 and the associated discussion). The cross-sectional view in Fig. 11.16 shows both the NMOS and PMOS devices that make up an inverter (and associated parasistics). Notice that in Fig. 11.10, the input pulse feeds through the gate-drain capacitance of the MOSFETs to the output of the inverter. This causes the output to change in the same direction as the input before the inverter starts to switch. This feedthrough and the parasitic bipolar transistors can cause the latch-up.

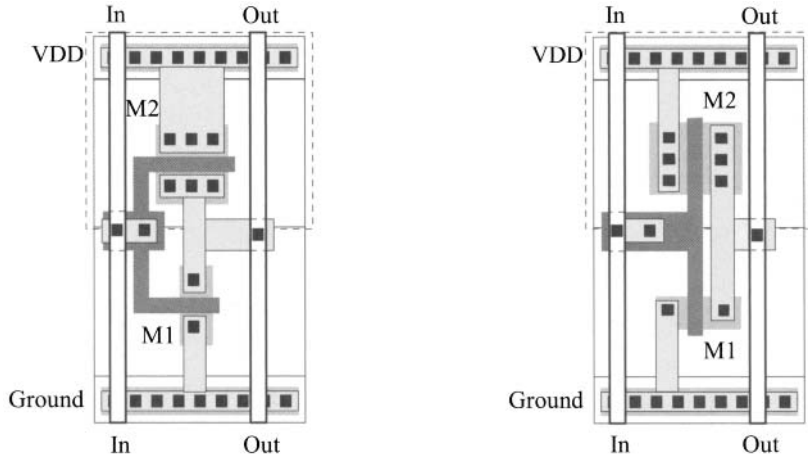

Figure 11.15 Layout styles for inverters.

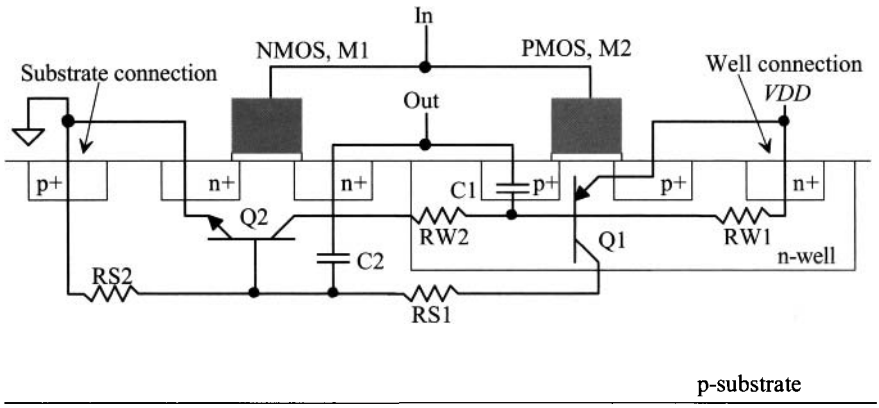

Figure 11.16 Cross-sectional view of an inverter showing parasitic bipolar transistors and resistors.

In Fig. 11.16, the emitter, base, and collector of transistor Q1 are the source of the PMOS, n-well, and substrate, respectively. Transistor Q2's collector, base, and emitter are the n-well, substrate, and source of the NMOS transistor. Resistors RW1 and RW2 represent the effects of the resistance of the n-well, and resistors RS1 and RS2 represent the resistance of the substrate. The capacitors C1 and C2 represent the drain implant depletion capacitance, that is, the capacitance between the drains of the transistors and the n-well (for C1) and substrate (for C2). The parasitic circuit resulting from the inverter layout is shown in Fig. 11.17.

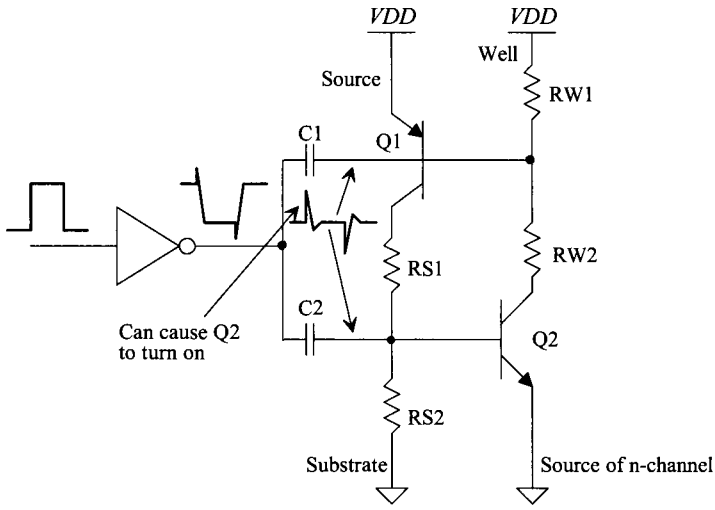

Figure 11.17 Schematic used to describe latch-up.

If the output of the inverter switches fast enough, the pulse fed through C2 (for positive-going inputs) can cause the base-emitter junction of Q2 to become forward biased. This then causes the current through RW2 and RW1 to increase, turning on Q1. When Q1 is turned on, the current through RS1 and RS2 increases, causing Q2 to turn on harder. This positive feedback will eventually cause Q2 and Q1 to turn on fully and remain that way until the power is removed and reapplied. A similar argument can be given for negative-going inputs feeding through C1, *VDD* bouncing upwards, or ground bouncing downwards.

Several techniques reduce the latch-up problem. One technique is to slow the rise and fall times of the logic gates, reducing the amount of signal fed through C1 and C2. Reducing the areas of M1 and M2's drains lowers the size of the depletion capacitance and the amount of signal fed through. Probably the best method of reducing latch-up effects is to reduce the parasitic resistances RW1 and RS2. If these resistances are zero, Q1 and Q2 never turn on. The value of these resistances, as seen in Fig. 11.16, is a strong function of the distance between the well and substrate contacts. Simply put, the closer these contacts are to the MOSFETs used in the inverter, the less likely it is that the inverter will latch up. These contacts should be plentiful as well as close. Placing substrate and well contacts between the PMOS and NMOS devices provides a low-resistance connection to *VDD* and ground, significantly helping to reduce latchup (see Fig. 11.18 for a simple layout example). Placing n+ and p+ areas between or around circuits reduces the amount of signal reaching a given circuit from another circuit. These implants are sometimes called guard rings (see Fig. 5.5). Notice that poly cannot be used to connect the gates of the MOSFETs, since poly over the n+ or p+ will be interpreted as a MOSFET. Therefore, metal2 is used to connect the MOSFETs together. The cost of reducing the possibility of latch-up is a more complicated layout in a larger area.

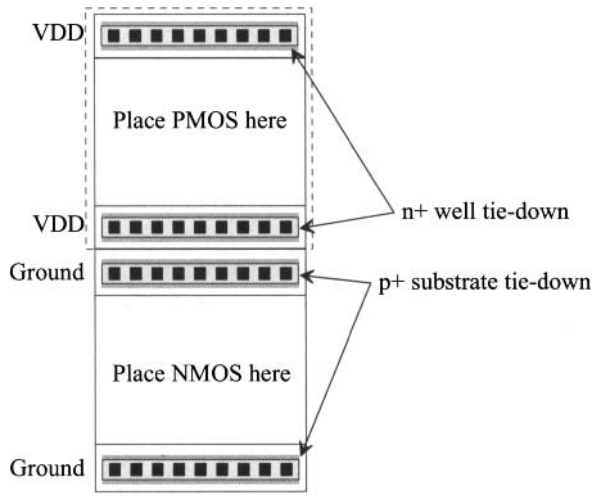

Figure 11.18 Adding an extra implant between NMOS and PMOS to reduce latch-up.

11.4 Sizing for Large Capacitive Loads

Designing a circuit to drive large capacitive loads with minimum delay is important when driving off-chip loads. As we saw in Ex. 11.6, a large load capacitance can drastically affect the delay through an inverter. Remembering our discussion in Sec. 10.3, we see that using a standard scope probe to measure an output signal can result in delays that are microseconds in length. In order to avoid this situation, we add a buffer circuit (a string of inverters) between the on-chip logic and the bonding pads. In this section we discuss how to design (select the widths of the MOSFETs) for low delays.

Buffer Topology

Consider the inverter string (a buffer) driving a load capacitance, labeled C_{load} and shown in Fig. 11.19. Moving towards the load in a cascade of the N inverters, each inverter larger than the previous by a factor A (that is, the width of each MOSFET is multiplied by A), a minimum delay can be obtained as long as A and N are picked correctly. Each inverter's input capacitance is larger than the previous inverter's input capacitance by a factor of A,

$$C_{in2} = A \cdot C_{in1} \text{ and } C_{in3} = A \cdot C_{in2} = A^2 \cdot C_{in1}, \text{ etc.} \tag{11.17}$$

The effective switching resistances are also divided by a factor of A, resulting in the same delay for each stage of the buffer,

$$R_{n,p2} = \frac{R_{n,p1}}{A} \text{ and } R_{n,p3} = \frac{R_{n,p2}}{A} = \frac{R_{n,p1}}{A^2} \tag{11.18}$$

In other words, the effective switching resistance of the NMOS in the third inverter is $1/A^2$ smaller than the effective switching resistance of the NMOS in the first inverter.

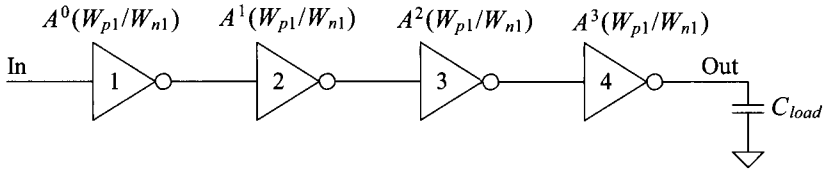

Figure 11.19 Cascade of inverters used to drive a large load capacitance.

If the load capacitance equals the input capacitance of the last inverter multiplied by A (so that the load capacitance has a value equal to the input capacitance of the next inverter if an additional inverter were used), then

$$\text{Input C of the final inverter} = C_{in1} \cdot A^N = C_{load} \tag{11.19}$$

or

$$A = \left[\frac{C_{load}}{C_{in1}}\right]^{\frac{1}{N}} \tag{11.20}$$

Again, the delays of each stage in the buffer are equal. The total delay of the inverter string is given by

$$(t_{PHL}+t_{PLH})_{total}=\underbrace{0.7\cdot(R_{n1}+R_{p1})(C_{out1}+AC_{in1})}_{\text{First-stage delay}}+\underbrace{0.7\cdot\frac{(R_{n1}+R_{p1})}{A}\cdot(AC_{out1}+A^2C_{in1})\ldots}_{\text{Second-stage delay}} \tag{11.21}$$

Because as the inverters are increased in size by A, their capacitances, both input and output, increase by A, while their resistances decrease by a factor A. This equation can be rewritten as

$$(t_{PHL}+t_{PLH})_{total}=0.7\cdot\sum_{k=1}^{N}(R_{n1}+R_{p1})(C_{out1}+AC_{in1})=0.7\cdot N(R_{n1}+R_{p1})(C_{out1}+AC_{in1}) \tag{11.22}$$

or with the help of Eq. (11.20):

$$(t_{PHL}+t_{PLH})_{total}=0.7\cdot N(R_{n1}+R_{p1})\cdot\left(C_{out1}+\left(\frac{C_{load}}{C_{in1}}\right)^{\frac{1}{N}}\cdot C_{in1}\right) \tag{11.23}$$

The minimum delay can be found by taking the derivative of this equation with respect to N, setting the result equal to zero, and solving for N. Taking the derivative of Eq. (11.23) with respect to N gives

$$0.7\cdot\left((R_{n1}+R_{p1})C_{out1}+(R_{n1}+R_{p1})C_{in1}\left(\left(\frac{C_{load}}{C_{in1}}\right)^{\frac{1}{N}}+N\cdot\left(\frac{C_{load}}{C_{in1}}\right)^{\frac{1}{N}}\frac{\ln(C_{load}/C_{in1})}{-N^2}\right)\right)=0 \tag{11.24}$$

The first term in this equation is the intrinsic delay of the first inverter in our cascade of inverters. *This first stage represents, generally, the on-chip logic gate and* ***is not part*** *of the buffer.* The first inverter is included in the calculations to represent the limited drive of the on-chip logic. If we assume that this delay is small, solving for N gives

$$N=\ln\frac{C_{load}}{C_{in1}} \tag{11.25}$$

Equations (11.25) and (11.20) are used in the buffer design to drive a large capacitance. Note that the larger the first inverter, the fewer the number of inverters needed to drive a given capacitive load.

Example 11.8

Estimate t_{PHL} + t_{PLH} for the inverter shown in Fig. 11.11 driving a load capacitance of 20 pF. Design a buffer to drive the load capacitance with a minimum delay.

The total propagation delay of the unbuffered inverter, Fig. 11.11, is given by

$$t_{PHL}+t_{PLH}=0.7\cdot(3.4k+3.4k)\cdot(20\,pF)=95\,ns\,!$$

Designing a buffer begins with determining C_{in1}. For our 20/10 inverter in the 50 nm process, the C_{in1} (see Table 10.2) is $\frac{3}{2}(1.25+0.625)\,fF=2.81\,fF$ and C_{out1} is $1.875\,fF$. To determine the number of inverters, we use

$$N=\ln\left(\frac{20\,pF}{2.81\,fF}\right)=8.87\rightarrow\ 9\text{ stages}$$

To maintain the same logic, that is, an inversion of the input signal, we use seven inverters. In practice, the difference in delay between eight and nine inverters is negligible. If we did not want a logic inversion, we would use eight stages. The area factor is then

$$A = \left[\frac{20\,pF}{2.81\,fF}\right]^{\frac{1}{8.87}} = 2.718 = e$$

noting that for the *minimum delay* in all cases the widths are increased by e.

The total delay, using Eq. (11.23), is then

$$(t_{PHL} + t_{PLH})_{total} = 0.7 \cdot 9 \cdot (3.4k + 3.4k)(1.875\,fF + 2.718 \cdot 2.81\,fF) = 407\,ps$$

or over 200 times faster. Since the PMOS width is twice the width of the NMOS, the propagation delay times, t_{PHL} and t_{PLH}, are equal, or

$$t_{PHL} = t_{PLH} = \frac{(t_{PHL} + t_{PLH})_{total}}{2N} = 22.5\,ps$$

A schematic of the design is shown in Fig. 11.20. ■

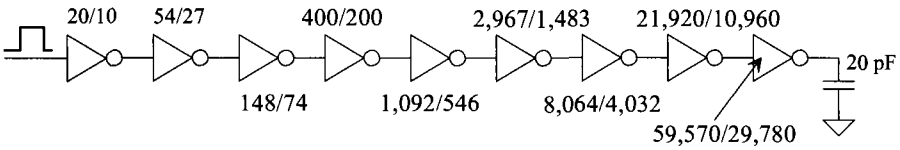

Figure 11.20 Buffer designed in Ex. 11.8. Attains the minimum delay but the buffer is not practical.

It should be clear that, although this technique results in the least delay in driving the 20 pF load, the MOSFETs needed are very large. In many applications, the very minimum delay through a buffer is not required. The value of A (ideally e) can be considerably larger and have little impact on the delay of the buffer (reducing the number of stages and their widths). Consider the following.

Example 11.9

Redesign the buffer of Ex. 11.8 with an A of 8. Compare the delay of the modified (practical) buffer to the delay of the ideal buffer calculated in Ex. 11.8.

We can rewrite Eq. (11.20) as

$$N \cdot \ln A = \ln \frac{C_{load}}{C_{in1}}$$

The natural logarithm of 8 is roughly 2 so we can solve for the number of stages using

$$N = \frac{1}{2} \cdot \ln \frac{C_{load}}{C_{in1}} = 4.43$$

To maintain the logic inversion, we'll use five stages. The delay is (roughly, because we are using 5 instead of 4.43) calculated as

$$(t_{PHL} + t_{PLH})_{total} = 0.7 \cdot 5 \cdot (3.4k + 3.4k)(1.875\,fF + 8 \cdot 2.81\,fF) = 580\,ps$$

(not too much larger than the 407 ps calculated in Ex. 11.7). The resulting buffer is shown in Fig. 11.21. ■

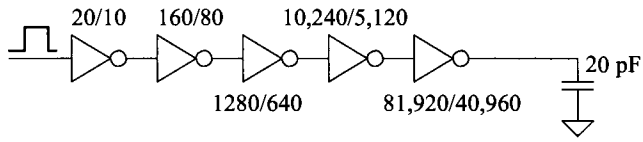

Figure 11.21 Buffer designed in Ex. 11.9.

Distributed Drivers

Consider the driver circuit shown in Fig. 11.22a containing 11 inverters. If all of the inverters shown in the figure are the same size, the delay from the input to the output is

$$t_{PHL} + t_{PLH} = 0.7 \cdot (R_n + R_p)(C_{out} + 10C_{in}) \qquad (11.26)$$

Now consider the circuit shown in Fig. 11.22b with 13 inverters. Again, assuming all of the inverters are the same size, the delay from the input to the output is

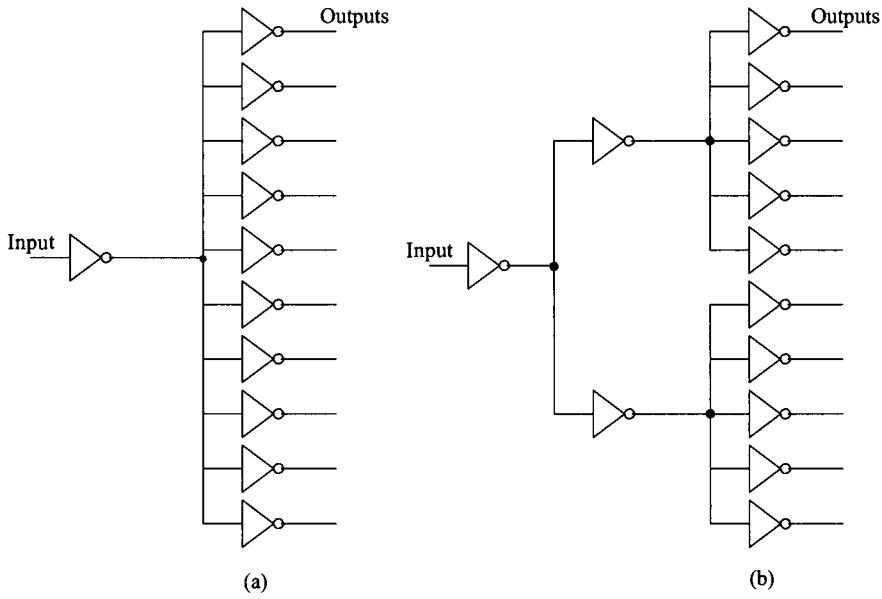

Figure 11.22 Distributed drivers.

$$t_{PHL} + t_{PLH} = 0.7 \cdot (R_n + R_p)[(C_{out} + 2C_{in}) + (C_{out} + 5C_{in})] = 0.7 \cdot (R_n + R_p)[2C_{out} + 7C_{in}] \tag{11.27}$$

which is less delay than the circuit with 11 inverters. Distributing the signal into different paths can reduce the propagation delays. Using the results from the last section, we can get minimum overall delay when the delays through each layer of logic are equal. This occurs when $A = e$ (each inverter drives 2.718 other inverters) and Eq. (11.25) is used to select the (number of) layers of logic. The load capacitance is equal to the number of outputs multiplied by the capacitance on each output. In practice, again as we saw in the last section, the change in delays isn't too significant, as long as one logic gate (one path) isn't loaded too much (compare actual numbers in Eqs. [11.26] and [11.27]).

At this point we can ask the question, "Why not make the first inverter in the circuits of Fig. 11.22 really large (small R_n and R_p) so that it has small effective resistances for driving the ten inverters quickly?" The answer is simply that as we increase the size of an inverter, we also increase its input capacitance. In SPICE simulations, we use ideal voltage sources to drive the first gate in our circuit. In practice, this inverter is driven from another gate somewhere on the chip. Increasing the size will slow the propagation delay-time of the gate driving this inverter.

Driving Long Lines

Often when designing large systems, a signal may need to be driven across the chip. In some cases, for example, in dynamic random-access memory (DRAM), the signal must be transmitted over a line that has a large parasitic resistance and capacitance. We need to develop a method of determining the delay through this line using hand calculations. This will lend insight to the design and help to determine exactly how to design the driver (or drivers).

Consider the driver circuit shown in Fig. 11.23. The inverter is driving an RC transmission line with resistance/unit length, r, capacitance/unit length, c, and unit length, l. We can estimate the delay from the input to voltage across the capacitor by adding the delays. This is given by

$$t_{PHL} + t_{PLH} = 0.7 \cdot [(R_n + R_p)(C_{out} + c \cdot l + C_{load}) + 2 \cdot (r \cdot l)(C_{load})] + 2 \cdot 0.35 \cdot rcl^2 \tag{11.28}$$

where the first term in this equation is the delay associated with the inverter driving the total capacitance at its output to ground. The second term is the delay associated with driving a capacitive load through the line's resistance, while the last term is an estimate of

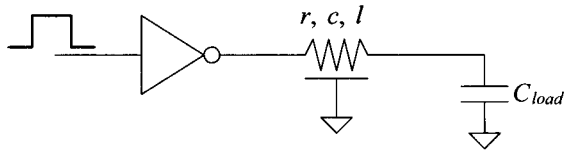

Figure 11.23 Driving an RC transmission line.

the delay through the RC line. The most common method of reducing the delay through the line is to place buffer stages at different locations along the line. This effectively breaks the line up and can lower the overall delay. If C_{load} is a major contributor to the delay, a buffer can be inserted between the RC line and C_{load} to reduce the delay.

11.5 Other Inverter Configurations

Three other inverter configurations are shown in Fig. 11.24. The inverter shown in Fig. 11.24a is an NMOS-only inverter, useful in avoiding latch-up. There's no PMOS device so there's no parasitic bipolar junction transistors. The inverters shown in Fig. 11.24b and c use a PMOS load, which is, in general, most useful in logic gates with a large number of inputs (more on this in the next chapter). In general, the selection of the MOSFET sizes in (a) and (b) follows the 4-to-1 rule; that is, the resistance (R_n or R_p) of the load is made four times larger than the resistance of M1. The resistance of the PMOS in (c) can be made eight times the resistance of the NMOS. Because $R_p > R_n$, the t_{PLH} will always be greater than the t_{PHL}. In other words, the switching times will be asymmetric.

For all inverter configurations in Fig. 11.24, a logic 1 input signal results in a DC current flowing in both MOSFETs. Making sure that this DC current isn't too large is an important design concern when sizing the MOSFETs. The output logic low will never reach 0 V in these inverters (V_{OL} doesn't reach ground), and thus the noise margins are poorer than the basic CMOS inverter of Fig. 11.1. The output high level of the inverter of Fig. 11.24c will reach *VDD*, while the other inverter's output high level will be a threshold voltage drop below *VDD*. It might be concluded that the power dissipation of the inverters shown in Fig. 11.24 is greater than the basic CMOS inverter. However, since the input capacitance of these inverters is less than the basic CMOS inverter and the output voltage swing is reduced, the inverter with the greatest power dissipation is determined by the operating frequency. At high operating frequencies, the basic CMOS inverter dissipates the most power. At DC or low frequencies, the inverter configurations seen in Fig. 11.24 dissipate more power.

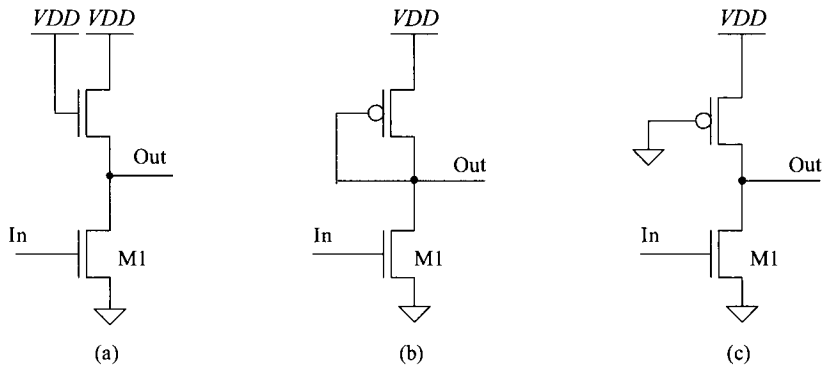

Figure 11.24 Other inverter configurations.

NMOS-Only Output Drivers

Because of the susceptibility of the basic CMOS inverter to latch-up, output drivers consisting of only NMOS devices are used. Figure 11.25 shows the basic "NMOS super buffer." When the input signal is low, M1 and M4 are off while M2 and M3 are on. The output is pulled to ground through M2. A high on the input to the buffer causes M1 and M4 to turn on pulling the output to $VDD - V_{THN}$, assuming that the input high-signal amplitude is *VDD*.

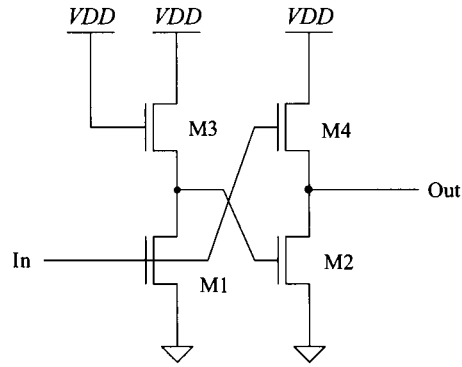

Figure 11.25 NMOS super buffer.

The reduced output voltage of the NMOS-only output buffer can be improved using the circuit of Fig. 11.26. The inverter driving the gate of M2 uses an on-chip generated DC voltage of *VDD* + *Vadd* (where *Vadd* is large enough to ensure that M2 turns fully on and the output is driven to *VDD*). Thus, the output swings from 0 to *VDD* similar to the CMOS output buffer. Note that with the addition of an enabling logic gate, the gates of M1 and M2 can be held at ground, forcing the output into the high-impedance (Hi-Z) state. (Note: Figure 18.40 shows two dynamic NMOS-only output drivers.)

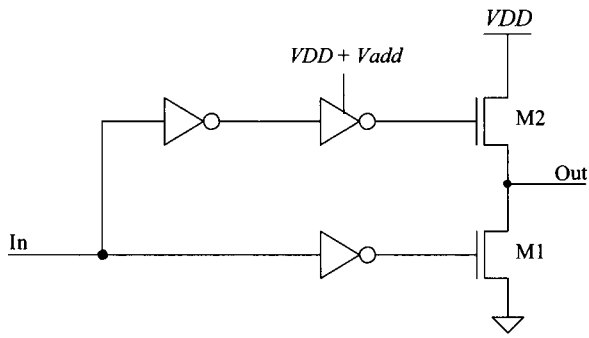

Figure 11.26 Output buffer using a pumped voltage.

Inverters with Tri-State Outputs

Two configurations used in the design of an inverter with tri-state outputs are shown in Fig. 11.27. A high on the S input allows the circuit to operate normally, that is, as an inverter. A low on the S input forces the output into the Hi-Z, or high-impedance state. These circuits are useful when data is shared on a communication bus. The logic symbol for the tri-state inverter is shown in Fig. 11.27c. Note that the circuit in (a) dissipates power even when the the select signal, S , is a low, while the circuit in (b) does not. However, the circuit in (a) has faster switching times because the effective resistance seen at the output to ground or *VDD* is lower (the NMOS and PMOS devices are in parallel).

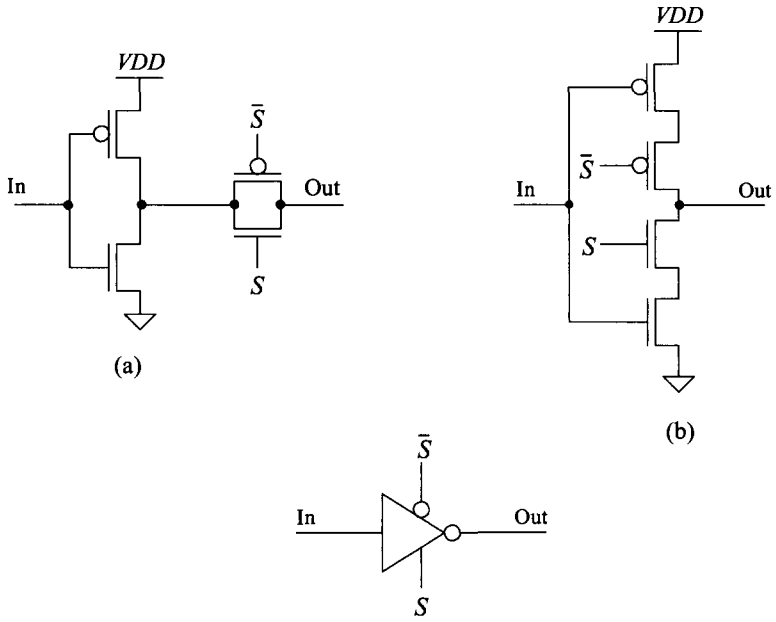

Figure 11.27 Circuits and logic symbol for the tri-state inverter.

Additional Examples

Additional delay calculations using inverters (and other CMOS circuit building blocks) can be found in Sec. 13.4.

ADDITIONAL READING

[1] K. Bernstein, K. M. Carrig, C. M. Durham, P. R. Hansen, D. Hogenmiller, E. J. Nowak, and N. J. Rohrer, *High Speed CMOS Design Styles*, Springer, 1999. ISBN 978-0792382201.

[2] J. P. Uyemura, *Introduction to VLSI Circuits and Systems*, John Wiley and Sons Publishers, 2002. ISBN 0-471-12704-3.

[3] M. I. Elmasry, *Digital MOS Integrated Circuits II,* IEEE Press, 1992. ISBN 0-87942-275-0, IEEE order number: PC0269-1.

[4] R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI-Design Techniques for Analog and Digital Circuits,* McGraw-Hill Publishing Co., 1990. ISBN 0-07-023253-9.

PROBLEMS

Use the 50 nm CMOS process for the following problems unless otherwise stated.

11.1 Estimate the noise margins for the inverters used to generate Fig. 11.4.

11.2 Design and simulate the DC characteristics of an inverter with V_{SP} approximately equal to V_{THN}. Estimate the resulting noise margins for the design.

11.3 Show that the switching point of three inverters in series is dominated by the V_{SP} of the first inverter.

11.4 Repeat Ex. 11.6 using a PMOS device with a width of 10.

11.5 Repeat Ex. 11.6 using the long-channel process with a 30/10 inverter.

11.6 Estimate the oscillation frequency of a 11-stage ring oscillator using inverters 30/10 inverters in the long-channel CMOS process. Compare your hand calculations to simulation results.

11.7 Using the long-channel process, design a buffer with minimum delay (A = 2.718) to insert between a 30/10 inverter and a 50 pF load capacitance. Simulate the operation of the design.

11.8 Repeat Problem 11.7 using an area factor, A, of 8.

11.9 Derive an equation for the switching point voltage, similar to the derivation of Eq. (11.4), for the NMOS inverter seen in Fig. 11.24a.

11.10 Repeat Problem 11.9 for the inverter in Fig. 11.24c. Note that the PMOS transistor is operating in the triode region when the input/output are at V_{SP}.