Chapter

18

Special Purpose CMOS Circuits

In this chapter we discuss some special-purpose CMOS circuits. We begin with the Schmitt trigger, a circuit useful in generating clean pulses from a noisy input signal or in the design of oscillator circuits. Next, we discuss multivibrator circuits, both astable and monostable types. This is followed by a discussion concerning input buffer design. Good receiver circuits (input buffers) in CMOS chips are required in any high-speed, board-level design to change the distorted signals transmitted between chips (because of the imperfections in the interconnecting signal paths) into well-defined digital signals with the correct pulse widths and amplitudes. Finally, we end this chapter with a discussion of on-chip voltage generators.

18.1 The Schmitt Trigger

The schematic symbol of the Schmitt trigger is shown in Fig. 18.1 along with typical transfer curves. We should note the similarity to the inverter transfer characteristics with the exception of a steeper transition region (and hysteresis). Curve A in Fig. 18.1 corresponds to the output of the Schmitt trigger changing from a low to a high, while curve B corresponds to the output changing from a high to a low. The hysteresis present in the transfer curves is what sets the Schmitt trigger apart from the basic inverter.

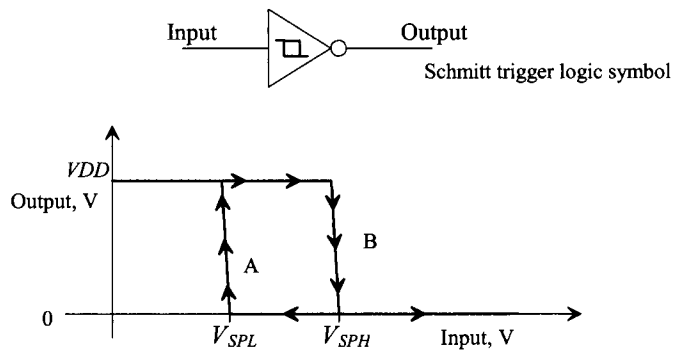

Figure 18.1 Transfer characteristics of a Schmitt trigger.

Figure 18.2 shows a possible input to a Schmitt trigger and the resulting output. When the output is high and the input exceeds V_{SPH}, the output switches low. However, the input voltage must go below V_{SPL} before the output can switch high again. Note that we get normal inverter operation when $V_{SPH} = V_{SPL}$. The hysteresis of the Schmitt trigger is defined by

$$V_H = V_{SPH} - V_{SPL} \tag{18.1}$$

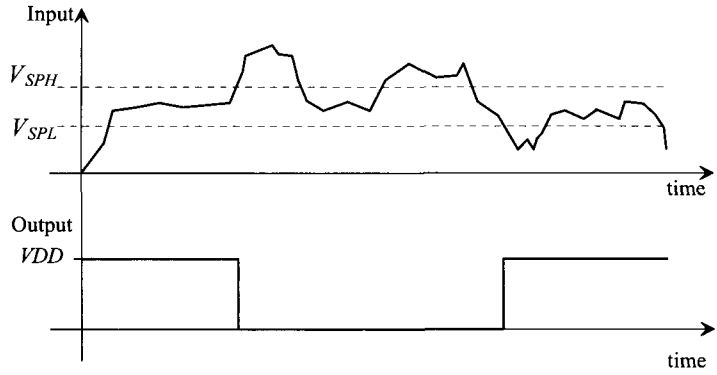

Figure 18.2 Input, top trace, and output of a Schmitt trigger.

18.1.1 Design of the Schmitt Trigger

The basic schematic of the Schmitt trigger is shown in Fig. 18.3. We can divide the circuit into two parts, depending on whether the output is high or low. If the output is low, then M6 is on and M3 is off and we are concerned with the p-channel portion when calculating the switching point voltages, while if the output is high, M3 is on and M6 is off and we are concerned with the n-channel portion. Also, if the output is high, M4 and M5 are on, providing a DC path to *VDD*.

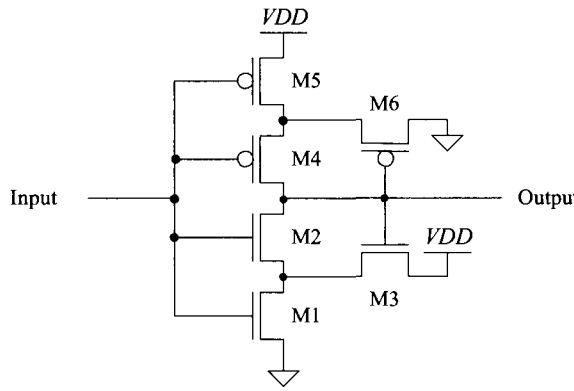

Figure 18.3 Schematic of the Schmitt trigger.

Let's begin our analysis of this circuit, assuming that the output is high (= *VDD*) and the input is low (= 0 V). Figure 18.4 shows the bottom portion of the Schmitt trigger used in calculating the upper switching point voltage, V_{SPH}. MOSFETs M1 and M2 are off, with V_{in} = 0 V while M3 is on. The source of M3 floats to $VDD - V_{THN}$, or approximately 4 V for *VDD* = 5 V. We can label this potential V_x, as shown in the figure.

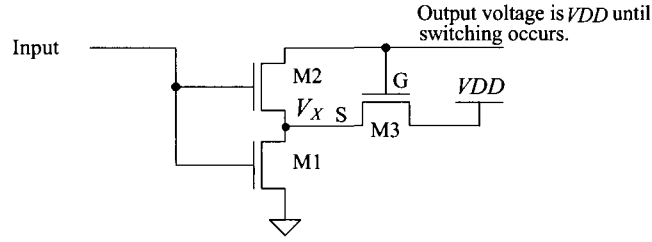

Figure 18.4 Portion of the Schmitt trigger schematic used to calculate upper switching point voltage.

With V_{in} less than the threshold voltage of M1, V_X remains at $VDD - V_{THN3}$. As V_{in} is increased further, M1 begins to turn on and the voltage, V_X, starts to fall toward ground. The high switching point voltage is defined when

$$V_{in} = V_{SPH} = V_{THN2} + V_X \tag{18.2}$$

or when M2 starts to turn on. As M2 starts to turn on, the output starts to move toward ground, causing M3 to start turning off. This in turn causes V_X to fall further, turning M2 on even more. This continues until M3 is totally off and M2 and M1 are on. This positive feedback causes the switching point voltage to be very well defined.

When Eq. (18.2) is valid, the currents flowing in M1 and M3 are essentially the same. Equating these currents gives

$$\frac{\beta_1}{2}(V_{SPH} - V_{THN})^2 = \frac{\beta_3}{2}(VDD - V_X - V_{THN3})^2 \tag{18.3}$$

Since the sources of M2 and M3 are tied together, $V_{THN2} = V_{THN3}$, the increase in the threshold voltages from the body effect is the same for each MOSFET. The combination of Eqs. (18.2) and (18.3) yields

$$\frac{\beta_1}{\beta_3} = \frac{W_1 L_3}{L_1 W_3} = \left[\frac{VDD - V_{SPH}}{V_{SPH} - V_{THN}}\right]^2 \tag{18.4}$$

The threshold voltage of M1, given by V_{THN} in this equation, is the zero body bias threshold voltage (= 0.8 V in our long-channel CMOS process and 0.25 V in the short-channel process). Given a specific upper switching point voltage, the ratio of the MOSFET transconductors is determined by solving this equation. A general design rule for selecting the size of M2, that is, β_2, is to require that

$$\beta_2 \geq \beta_1 \text{ or } \beta_3 \tag{18.5}$$

since M2 is used as a switch.

A similar analysis can be used to determine the lower switching point voltage, V_{SPL}, resulting in the following design equation:

$$\frac{\beta_5}{\beta_6} = \frac{W_5 L_6}{L_5 W_6} = \left[\frac{V_{SPL}}{VDD - V_{SPL} - V_{THP}}\right]^2 \tag{18.6}$$

The following example illustrates the design procedure for a Schmitt trigger.

Example 18.1

Design and simulate a Schmitt trigger using the short-channel CMOS process with $V_{SPL} = 400$ mV and $V_{SPH} = 700$ mV.

We begin by solving Eqs. (18.4) and (18.6) for the transconductance ratios. For the upper switching point voltage,

$$\frac{W_1 L_3}{W_3 L_1} = \left[\frac{1-0.7}{0.7-0.25}\right]^2 = 0.444 \rightarrow L_1 = L_3 = 1 \text{ and } W_1 = 10, W_3 = 22.5$$

and for the lower switching point voltage,

$$\frac{W_5 L_6}{W_6 L_5} = \left[\frac{0.4}{1-0.4-0.25}\right]^2 = 1.3 \rightarrow L_5 = L_6 = 1 \text{ and } W_6 = 20, W_5 = 26$$

M2 is set to 10/1 and M4 is set to 20/1. Simulation results are seen in Fig. 18.5. This figure reveals the benefit of using a Schmitt trigger, namely, it allows slow moving inputs to be made into good solid logic high and low values. In a practical circuit, connecting the ramp-shaped input seen in Fig. 18.5 to an inverter would produce oscillations in the inverter's output (because of noise on the ramp). ■

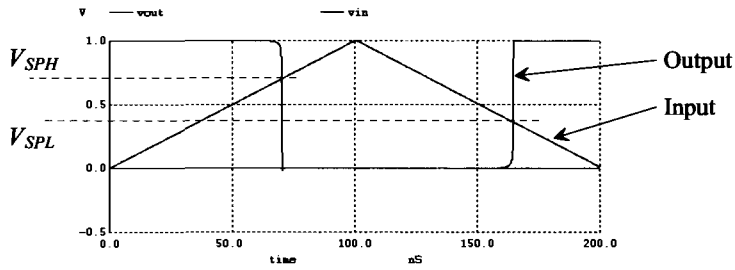

Figure 18.5 The input and output of the Schmitt trigger designed in Ex. 18.1.

Switching Characteristics

The propagation delays of the Schmitt trigger can be calculated in much the same way as the inverter of Ch. 11. Defining equivalent digital resistances for M1, M2, M4, and M5 as R_{n1}, R_{n2}, R_{p4}, and R_{p5}, respectively, gives a high-to-low propagation delay-time, neglecting the Schmitt trigger output capacitance, of

$$t_{PHL} = 0.7 \cdot (R_{n1} + R_{n2}) \cdot C_{load} \tag{18.7}$$

and

$$t_{PLH} = 0.7 \cdot (R_{p4} + R_{p5}) \cdot C_{load} \tag{18.8}$$

18.1.2 Applications of the Schmitt Trigger

Consider the waveform shown in Fig. 18.6. A pulse with ringing is a common voltage waveform encountered in buses or lines interconnecting systems. If this voltage is applied directly to a logic gate or inverter input with a V_{SP} of 0.5 V, the output of the gate will vary with the period of the ringing on top of the pulse. Using a Schmitt trigger with properly designed switching points can eliminate this problem.

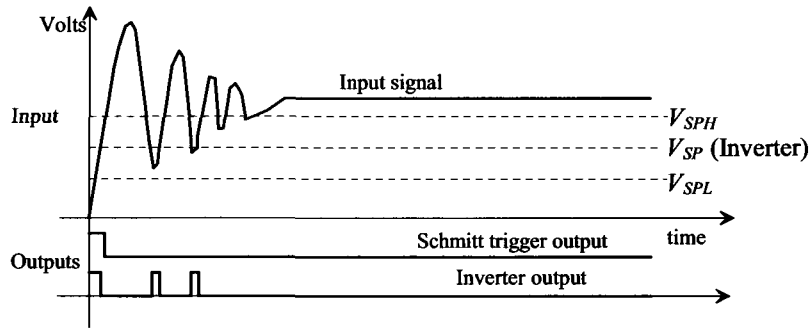

Figure 18.6 Applying a Schmitt trigger to clean up an interconnecting signal.

The Schmitt trigger can also be used as an oscillator (Fig. 18.7). The delay-time in charging and discharging the capacitor sets the oscillation frequency. At the moment in time when the output of the Schmitt trigger switches low, the voltage across the capacitor is V_{SPH}. The capacitor will start to discharge toward ground. The voltage across the capacitor is given by

$$V_c(t) = V_{SPH} \cdot e^{-t/RC} \tag{18.9}$$

At the time when $V_c(t) = V_{SPL}$, the output of the Schmitt trigger changes state. This time is given by solving Eq. (18.9) by

$$t_1 = RC \cdot \ln \frac{V_{SPH}}{V_{SPL}} \tag{18.10}$$

A similar analysis for the case when the capacitor is charged from V_{SPL} to V_{SPH} gives

$$V_c(t) = V_{SPL} + (VDD - V_{SPL})\left(1 - e^{\frac{-t}{RC}}\right) \tag{18.11}$$

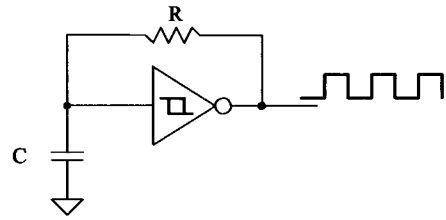

Figure 18.7 Oscillator design using a Schmitt trigger.

and

$$t_2 = RC \cdot \ln \frac{VDD - V_{SPL}}{VDD - V_{SPH}} \tag{18.12}$$

The oscillation frequency, neglecting the intrinsic delay of the Schmitt trigger, is given by

$$f_{osc} = \frac{1}{t_1 + t_2} \tag{18.13}$$

The capacitance used in these equations is the sum of the input capacitance of the Schmitt trigger and any external capacitance.

An alternative oscillator using the Schmitt trigger is shown in Fig. 18.8. Here the MOSFETs M1 and M4 behave as current sources (see Ch. 20) mirroring the current in M5 and M6. When the output of the oscillator is low, M3 is on and M2 is off. This allows the constant current from M4 to charge C. When the voltage across C reaches V_{SPH}, the output of the Schmitt trigger swings low. This causes the output of the oscillator to go high and allows the constant current from M1 to discharge C. When C is discharged down to V_{SPL}, the Schmitt trigger changes states. This series of events continues, generating the square wave output.

If we label the drain currents of M1 and M4 as I_{D1} and I_{D4}, we can estimate the time it takes the capacitor to charge from V_{SPL} to V_{SPH} as

$$t_1 = C \cdot \frac{V_{SPH} - V_{SPL}}{I_{D4}} \tag{18.14}$$

and the time it takes to charge from V_{SPH} to V_{SPL} is

$$t_2 = C \cdot \frac{V_{SPH} - V_{SPL}}{I_{D1}} \tag{18.15}$$

The period of the oscillation frequency is, as before, the sum of t_1 and t_2.

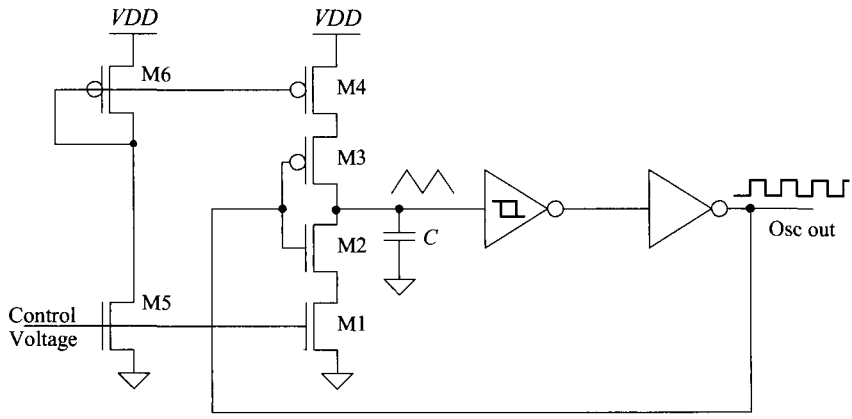

Figure 18.8 Voltage-controlled oscillator using Schmitt trigger and current sources. MOSFETs M2 and M3 are used as switches.

This type of oscillator is termed a voltage-controlled oscillator (VCO) since the output frequency can be controlled by an external voltage. The currents I_{D1} and I_{D4}, (Fig. 18.8) are directly controlled by the control voltage. As we will see in Ch. 20, the current in M5 is mirrored in M1, M4, and M6, with an appropriate scaling factor dependent on the size of the transistors.

18.2 Multivibrator Circuits

Multivibrator circuits (Fig. 18.9) are circuits that employ positive feedback. The name "multivibrator" is a vestige from early-time electronics development (prior to the ubiquitous term "digital") where the circuits' outputs vibrate between two states. There are three types of multivibrators: astable, bistable, and monostable. Astable multivibrator circuits are unstable in either output (high or low) state. The oscillators that we have discussed are examples of astable multivibrators. The bistable multivibrator is stable in either the high or low state. Flip-flops and latches are examples of the bistable multivibrator. Monostable multivibrators are stable in a single state. Monostable multivibrators are also called one-shots. In this section we discuss the monostable and astable multivibrators. We distinguish the material in this section from the other material in the book by using resistor-capacitor time constants to set time intervals.

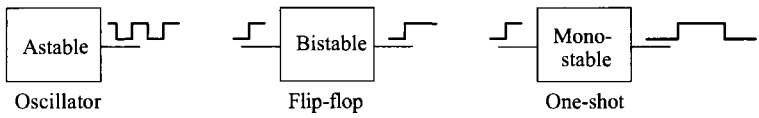

Figure 18.9 Multivibrator circuits.

18.2.1 The Monostable Multivibrator

A CMOS implementation of the monostable multivibrator is shown in Fig. 18.10. Under normal conditions, V_{in} is low and the output of the NOR gate, V_1, is high. The voltage V_2 is pulled high through the resistor, and the output of the inverter, V_3, is a low. Upon application of a trigger pulse, that is, V_{in} going high, both V_1 and V_2 drop to zero volts and the output of the inverter, which is also the output of the monostable, goes high. This output is fed back to the input of the NOR gate holding V_1 at ground potential.

After triggering, the potential V_2 will start to increase because C is charged through R. The potential across the capacitor after triggering takes place is given by

$$V_c(t) = V_2(t) - \overbrace{V_1(t)}^{=0} = VDD \cdot (1 - e^{\frac{-t}{RC}}) \tag{18.16}$$

If we assume that the V_{SP} of the inverter is $VDD/2$, then the time it takes for the capacitor to charge to V_{SP} is given by

$$t = RC \cdot \ln \frac{VDD}{VDD - V_{SP}} = RC \cdot \ln(2) \approx 0.7RC \tag{18.17}$$

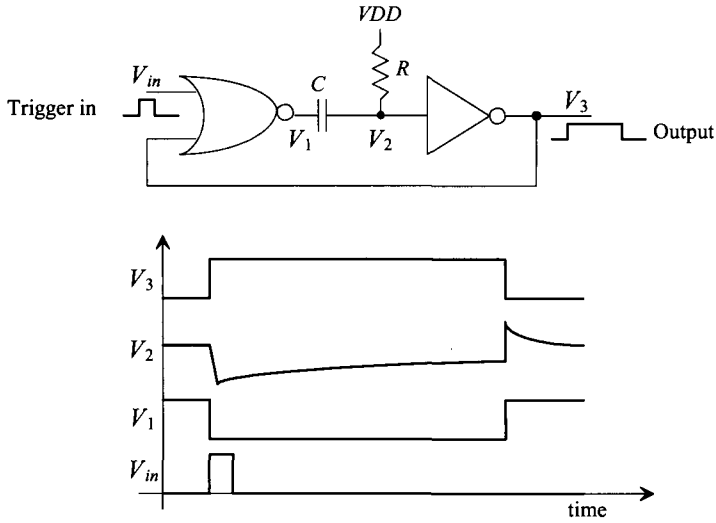

Figure 18.10 Operation of the monostable multivibrator.

This time also defines the output pulse width, neglecting gate delays, since the inverter switches low. The inverter output, V_3, going low causes V_1 to go back to *VDD* and V_2 to go to *VDD* + *VDD*/2. If the resistor or capacitor is bonded out (connected to the output pads), the ESD diodes may keep V_2 from going much above *VDD* + 0.7. The time it takes V_2 to decay back down to *VDD* limits the rate at which the one-shot can be retriggered. Also note that the trigger input can be longer than the output pulse width. Longer output pulse widths may cause V_2 to go as high as 10 V as well as limit the maximum trigger rate.

18.2.2 The Astable Multivibrator

An example of an astable multivibrator is shown in Fig. 18.11. This circuit has no stable state and thus oscillates. To analyze the behavior of this multivibrator, let's begin by assuming that the output, V_3, has just switched high. The output going high causes V_1 to go high (to *VDD* + V_{SP1}), forcing V_2 low. The voltage across the capacitor after this switching takes place is given by

$$V_c(t) = V_1(t) - \overbrace{V_3(t)}^{=VDD} = (VDD + V_{SP1}) \cdot e^{\frac{-t}{RC}} - VDD \qquad (18.18)$$

The output of the astable will go low, $V_3 = 0$, when $V_1 = V_{SP1}$. Substituting this condition into the previous equation gives the time the output is high (or low) and is given by

$$t_1 = RC \cdot \ln \frac{VDD + V_{SP1}}{V_{SP1}} = t_2 \qquad (18.19)$$

If $V_{SP1} = VDD/2$, then

$$t_1 = t_2 = 1.1RC \qquad (18.20)$$

and the frequency of oscillation is

$$f_{osc} = \frac{1}{t_1 + t_2} = \frac{1}{2.2RC} \tag{18.21}$$

Again, if the resistor and capacitor are bonded out, the ESD diodes on the pads will limit the voltage swing of V_1.

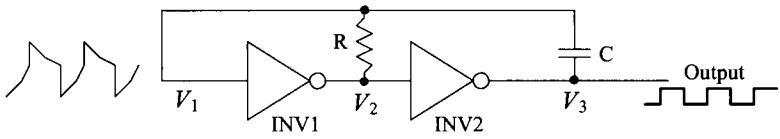

Figure 18.11 An astable multivibrator.

18.3 Input Buffers

Input buffers are circuits that take a chip's input signal, with imperfections such as slow rise and fall times, and convert it into a clean digital signal for use on-chip. If the buffer doesn't "slice" the data in the correct position, timing errors can occur. For example, consider the waveforms seen in Fig. 18.12. If the input signal is sliced too high or too low, the output signal's width is incorrect. In high-speed systems this reduces the timing budget in the system and can result in errors.

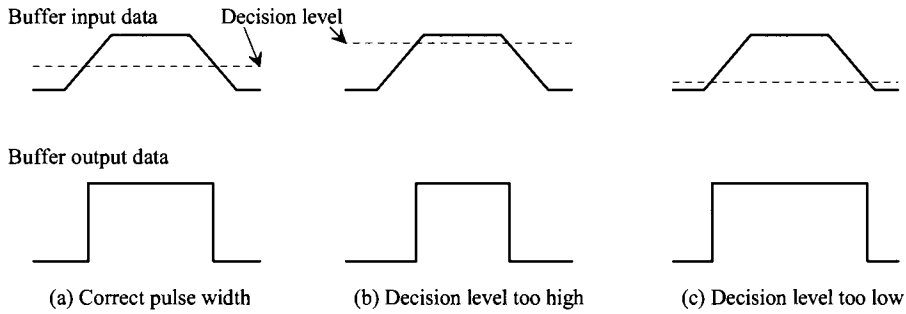

Figure 18.12 Timing errors in regenerating digital data.

18.3.1 Basic Circuits

If not careful, simple circuits can introduce unwanted pulse width variations because of differences in rise and fall times. Consider the inverter circuit seen in Fig. 18.13. The switching point voltage of the inverter, because of process, *VDD* (voltage), or temperature variations (PVT) will move around. Further, differences in the PMOS and the NMOS resistance will affect the rise and fall times of the inverter's output signal. The output of the first inverter, in Fig. 18.13, sees a much larger load capacitance than the second inverter. The delay time from the input going high to the output going high is roughly

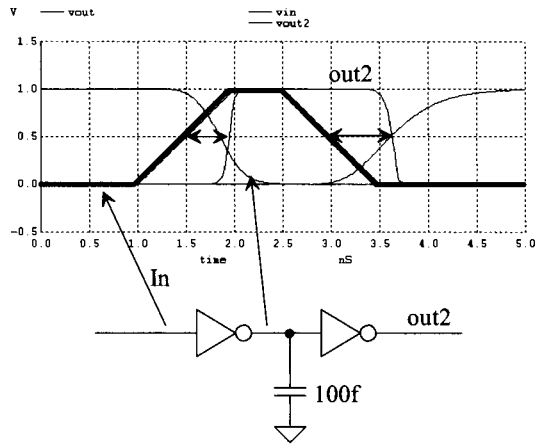

Figure 18.13 How skew is introduced into a high-speed signal.

400-ps. However, the delay time between the input and the output going low is 600 ps. As the input signal travels through the digital system, the time skew added to the input signal can add up and result in timing errors (the data is received too early or too late at different points in the system). Note that had we matched the loading of each inverter, the propagation delays would be more similar, Fig. 18.14. When the input signal goes high, the output of the first inverter goes low (t_{PHL}) and the output of the second inverter goes high (t_{PLH}). The total delay is the sum of $t_{PHL} + t_{PLH}$. However, when the input signal goes low, the output of the first inverter goes high (t_{PLH}) and the output of the second inverter goes low (t_{PHL}), resulting in the same sum ($t_{PHL} + t_{PLH}$). *If possible, make the number of t_{PHL} delays in series with a high-speed signal even and equal to the number of t_{PLH} delays.*

Of course, to better equalize the delays, the second inverter in Fig. 18.14 would need an additional bit of loading (an inverter connected to its output). Also, the input signal should transition faster in an attempt to match the transition times of the inverters.

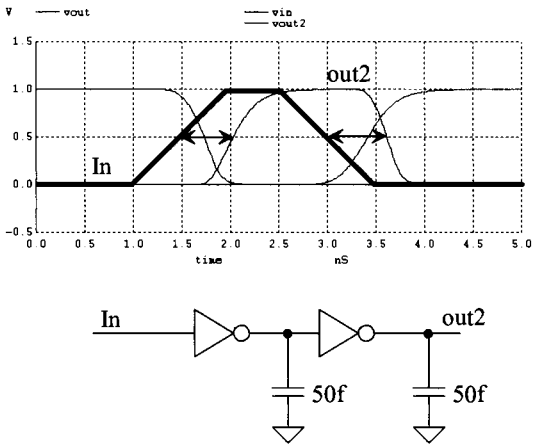

Figure 18.14 How equalizing delays can be used to reduce skew.

Skew in Logic Gates

Consider the NAND gate in Fig. 18.15. A different delay will be added to an input signal depending on which input of the NAND gate is used. As seen in the figure, the *A* input, with the *B* input high, propagates to the output slightly quicker than the *B* input (with the *A* input high). For the NAND gate, this difference in propagation delays is only a factor for the NMOS devices (because they are in series with the output of the gate).

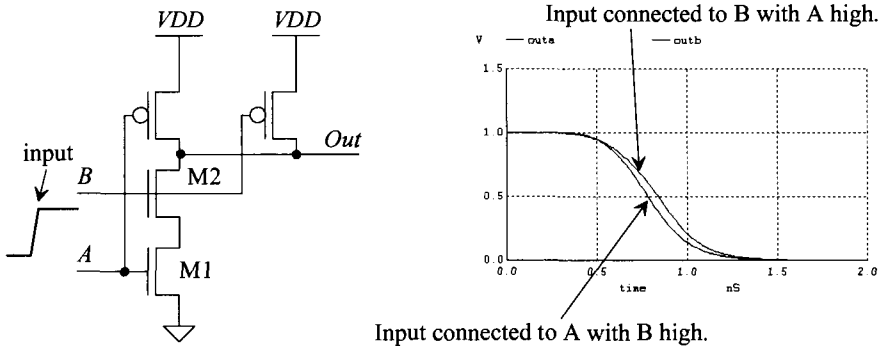

Figure 18.15 The skew introduced by using different inputs.

Figure 18.16 shows how two NAND gates can be used in parallel to eliminate the differences in the propagation delay between inputs. The series NMOS are arranged so that no matter which input is toggled the output changes at the same rate. Note that two of the PMOS devices can be eliminated to simplify the circuit without affecting the propagation delays.

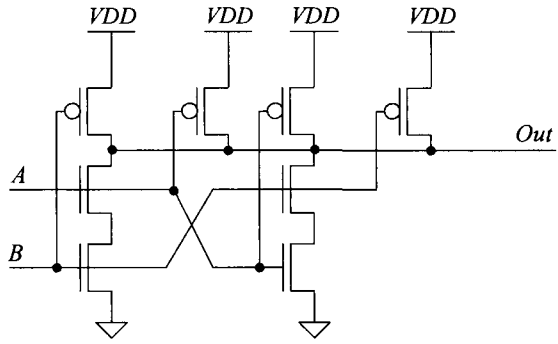

Figure 18.16 Using two NAND gates in parallel to reduce input-dependent skew.

The previous discussion neglected the effects of the gate's switching point voltage. If the input signals are not transitioning to full logic levels (*VDD* and ground) or the rise and fall times are not fast (compared to the gate delay time), then the point where the input circuit switches is critical. This leads us to our next topic.

18.3.2 Differential Circuits

In order to precisely slice input data, as seen in Fig. 18.12, a reference voltage may be transmitted, on a different signal path, along with the data. Alternatively, the data may be transmitted differentially (an input and its complement). In either case a differential amplifier is needed, Fig. 18.17. A differential amplifier input buffer (which we'll simply call an input buffer from this point on) amplifies the difference between the two inputs. In the simplest case one input to the input buffer is a DC voltage, say 0.5 V (*Vinm* in Fig. 18.17). When the other input (*Vinp*) goes above 0.5 V, the output of the buffer changes states (goes from a low to a high) or

$$Vinp > Vinm \rightarrow \text{out} = \text{"1"} \tag{18.22}$$

and

$$Vinp < Vinm \rightarrow \text{out} = \text{"0"} \tag{18.23}$$

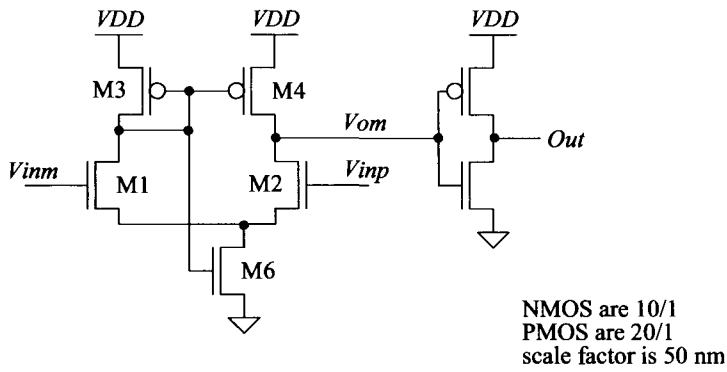

Figure 18.17 An (n-flavor) input buffer for high-speed digital design.

The diff-amp in Fig. 18.17 is based on the topologies seen in Ch. 22. This circuit is *self-biased* because no external references are used to set the current in the circuit (the gate of M6 is tied up to the gate of M3). When *Vinp* is larger than *Vinm*, the current in M2 is larger than the current in M1 ($V_{GS2} > V_{GS1}$). The current in M1 flows through M3 and is mirrored by M4 (and so M4's current is less than M2's current). This causes the diff-amp's output, *Vom*, to go towards ground (until the current in M2 equals the current in M4) and the output of the inverter, *Out*, to go high. Note that the gain from the *Vinp* input to the output of the circuit is larger than the gain from *Vinm* to the output (M3, being diode-connected, is a lower resistance than M4). It is generally a good idea to connect the reference voltage to the *Vinm* input.

The DC simulation results for the buffer in Fig. 18.17 are shown in Fig. 18.18. The x-axis is the *Vinp* input swept from 0 to 1 V. The *Vinm* input is held from 0 to 1 V in 200 mV steps. When *Vinm* is held at 400 mV and *Vinp* goes above 400 mV, the output changes from 0 to 1 (although there is a small offset which necessitates that *Vinp* go to approximately 415 mV before the output transitions).

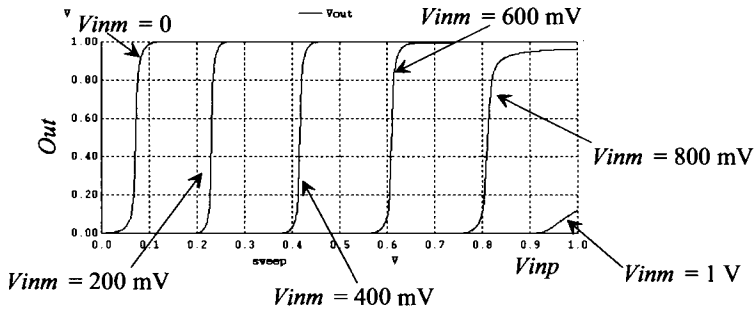

Figure 18.18 Simulating the DC behavior of the buffer in Fig. 18.17.

Transient Response

An example transient response for the buffer in Fig. 18.17 is seen in Fig. 18.19. A very small increase in *Vinp* above *Vinm* is required to make the output of the buffer switch states. We have several practical questions that should be answered with variations of this simulation. For example, what are the minimum and maximum values of *Vinm* allowed. Next, why are the delays between *Vinp* going high and going low different? Is it because of the offset seen in Fig. 18.18 (the output doesn't precisely switch at a *Vinm* 400 mV)? Let's provide some discussion concerning these concerns.

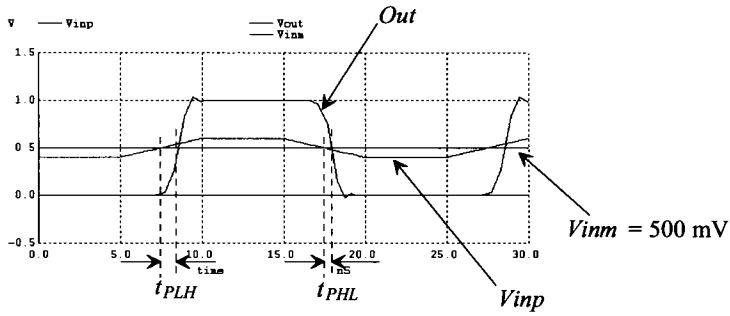

Figure 18.19 Transient response of the input buffer in Fig. 18.17 driving a 50 fF load.

Looking at Fig. 18.17, we can see that if the inputs fall below V_{THN} (= 250 mV here), then the circuit won't work very quickly (the MOSFETs move into the subthreshold region). So we would expect the propagation delays to increase. Indeed, as seen in Fig. 18.20, the delays go up. Ideally, the delay of the buffer is independent of power supply voltage, temperature, or input signal amplitudes (or pulse shape). To get better performance for lower input level signals, we might use the PMOS version of the buffer in Fig. 18.17, as seen in Fig. 18.21. Resimulating this buffer with the signals seen in Fig. 18.20 gives the results seen in Fig. 18.22. The delays are considerably better, however, there is an offset that appears rather large (because the output changes at the same time as *Vinp* going past *Vinm*, indicating that an offset is present). To avoid this

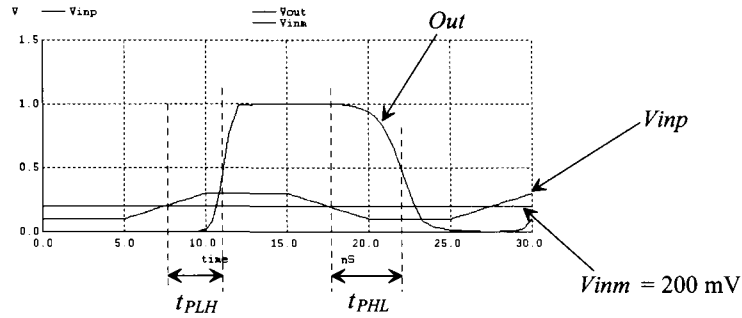

Figure 18.20 Resimulating with lower input signal voltages.

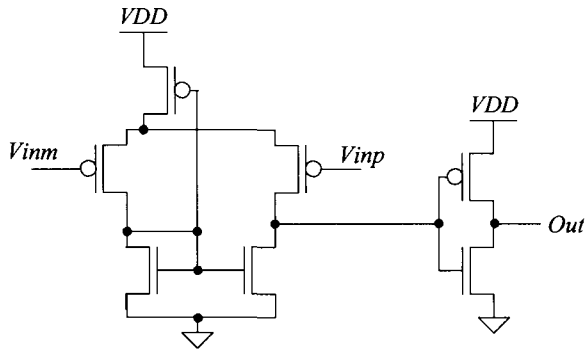

Figure 18.21 A PMOS input buffer for high-speed digital design.

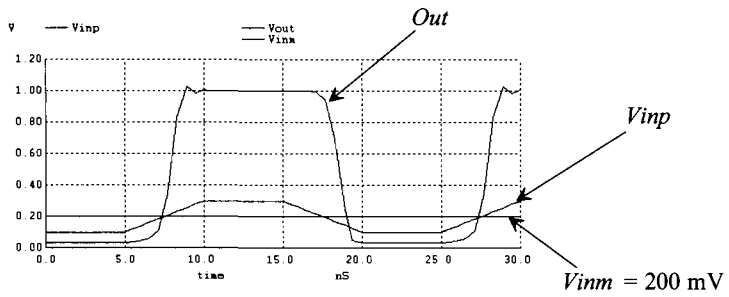

Figure 18.22 Repeating the simulation in Fig. 18.20 with the buffer in Fig. 18.21.

offset, we might use the NMOS buffer in Fig. 18.17 with the PMOS buffer in Fig. 18.21 to form a buffer that operates well with input signals approaching ground or *VDD*. The result is seen in Fig. 18.23. By using the buffers in parallel, the complementary nature results in a buffer that is robust and works over a wide range of operating voltages. Figure 18.24 shows a DC sweep simulation for the buffer with the *Vinp* input swept and the *Vinm* changed in increments of 100 mV. Note the smaller offset.

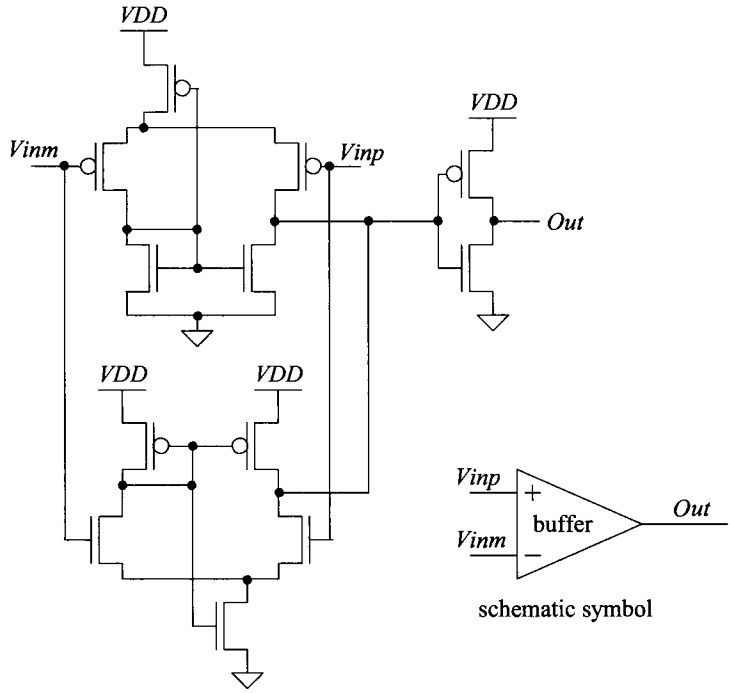

Figure 18.23 A rail-to-rail input buffer based on the topologies in Figs. 18.17 and 18.21.

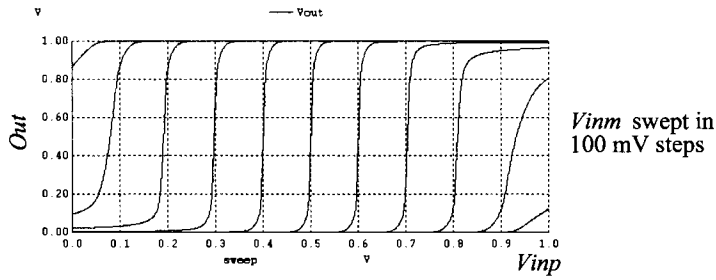

Figure 18.24 DC characterisitics of the buffer in Fig. 18.23.

Example 18.2

Design a high-speed input buffer based on the topology in Fig. 18.17 with a small amount of hysteresis.

In any circuit that has hysteresis we have some positive feedback. We can introduce positive feedback into the buffer in Fig. 18.17 by adding a long L MOSFET across the output inverter, Fig. 18.25. When the output is low, this turns the long L MOSFET on and make the self-biased diff-amp work harder to pull the input of the inverter to ground. When the output is high, the long L MOSFET is off and doesn't affect the circuit. ■

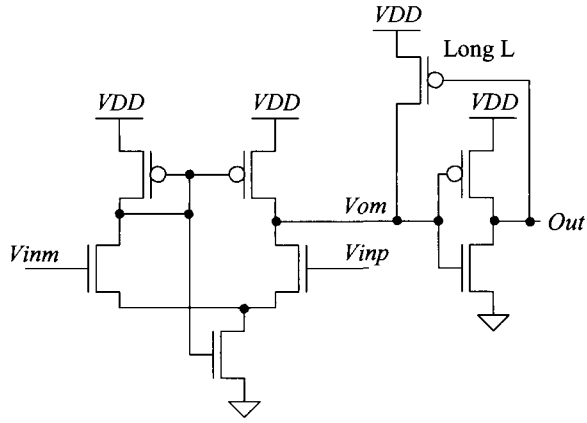

Figure 18.25 An input buffer for high-speed digital design with hysteresis.

18.3.3 DC Reference

In the previous section we assumed we had a DC voltage, *Vinm* , at precisely the correct voltage to slice the data (in the middle). In a real system the data varies and the communication channel is bandlimited (behaves like a lowpass filter). The result is that the amplitudes of the data vary depending on the data and the channel frequency response. Consider the simple RC lowpass filter and data used to model a transmission system as seen in Fig. 18.26. The ideal point where we slice the output data changes with the input data. What we need is a circuit that determines the maximum and minimum of an input waveform and outputs the average of the two to slice the buffer's input data in the center.

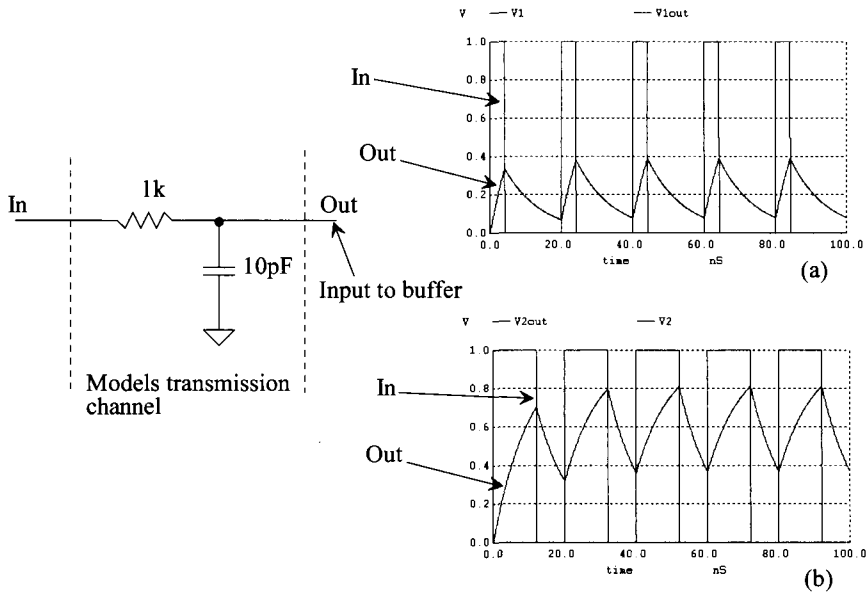

Figure 18.26 How the shape of the data changes through a communication channel.

Towards this goal consider the peak detector circuit seen in Fig. 18.27. The buffer from Fig. 18.23 can be used in this circuit. When the input, v_{in}, goes above the voltage stored on the capacitor, v_{peak}, the output of the buffer goes low, turning on the long-length MOSFET and pulling the output towards *VDD*. As v_{peak} approaches v_{in}, the MOSFET starts to shut off. As a result the output voltage across the capacitor, v_{peak}, corresponds to the peak voltage of the input signal. This peak detector can be used to generate a reference voltage that falls within the middle of the input data, Fig. 18.28. The peak and valley detectors are used to find the minimum and maximum of the input signal. The two resistors average the minimum voltages and feed the result (the DC average of the input) to the bottom buffer circuit. The resistors also are used to leak charge off of the capacitors so that the averaging circuit can follow changes in the input data (the averaging is actually a *running average*). Figure 18.29 shows some simulation results. In the top plots the output signal from Fig. 18.26a is applied to the input of the DC generation circuit. As expected, the output of the DC generation circuit, after a start-up delay, goes right to the middle of the input data.

The speed (response time) of this generation circuit can be increased by reducing the resistors and capacitors in the circuit. However, if the values are reduced too much, a long string of zeroes or ones will cause the DC generation circuit's output (labeled "average" in Fig. 18.28) to go to ground or *VDD*. The bottom traces in Fig. 18.29 show the results of applying the output signal from Fig. 18.26b to the DC generation circuit. Again, the output moves quickly to the center of the data. What's more interesting in these figures is a comparison between the original input data and the regenerated output data (labeled *In* and *Out* in Fig. 18.29). The output data pulse widths are considerably different from the input pulse widths (remembering that there is a delay through both the channel RC seen in Fig. 18.26 and the buffer in Fig. 18.28). Ideally, the pulse widths (the data) of the input and output are the same. Looking at the responses in Fig. 18.26a, we see that the effect of the finite channel bandwidth is to distort the channel's output data. *The only solution to this problem is to make the channel transmission bandwidth effectively wider.* An equalizer (discussed in the next chapter) can be used for this purpose at the cost of reduced signal swing. We can also reduce the input impedance of the input buffer to lower the time constant associated with the channel. Let's discuss this second approach.

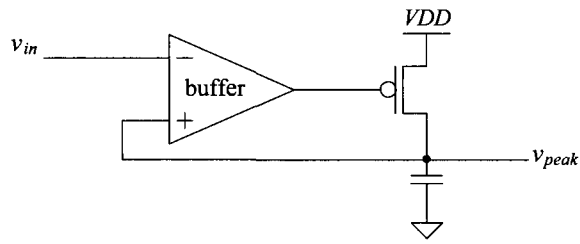

Figure 18.27 CMOS peak detector.

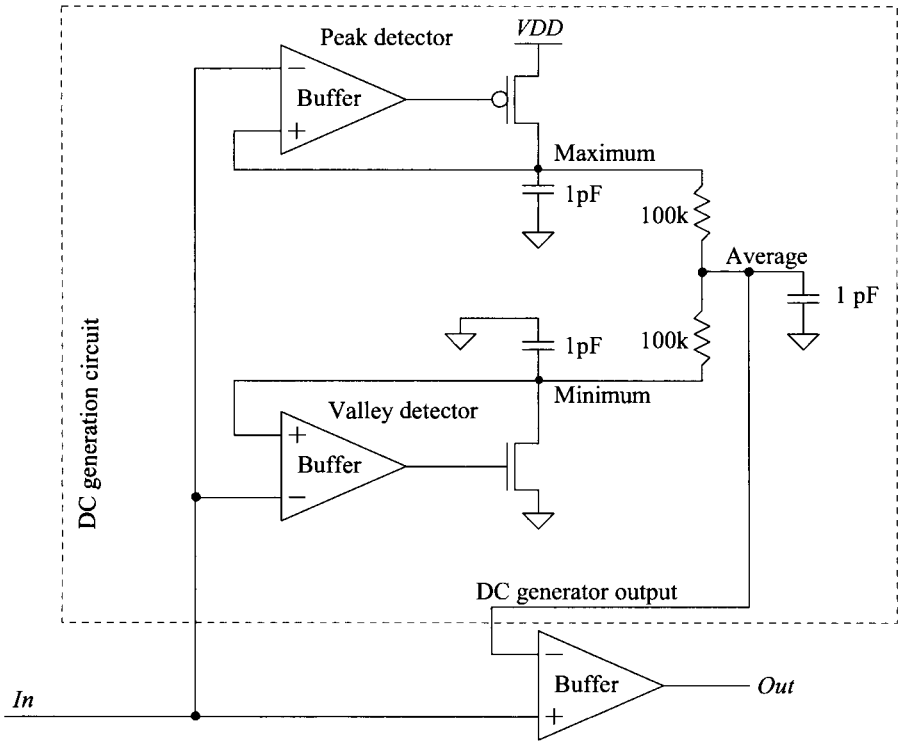

Figure 18.28 A DC generation circuit.

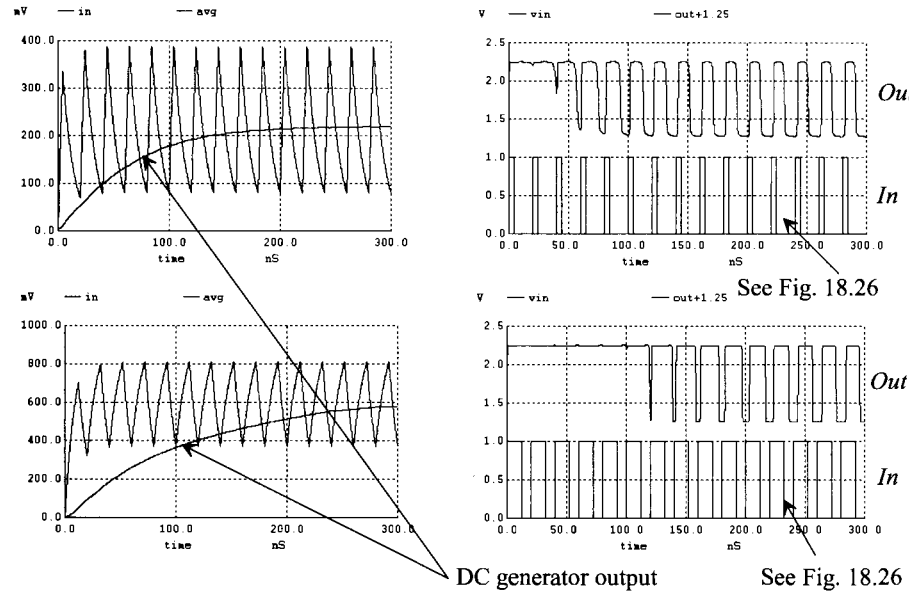

Figure 18.29 The output of the DC restore circuit in Fig. 18.28.

18.3.4 Reducing Buffer Input Resistance

A simple solution to increasing the effective bandwidth of the transmission channel is to reduce the input resistance of the input buffer. The time constant associated with the channel in Fig. 18.30 is 10 ns. When we connect the buffer to the transmission channel, the time constant drops to 3.33 ns (the three 1k resistors in parallel multiplied by the 10 pF capacitance). The drawbacks of this approach are increased power dissipation and reduced input signal amplitudes. Figure 18.31 shows how the buffer in Fig. 18.30 behaves with the input signals seen in Fig. 18.26a. The distortion (difference in the pulse widths of ones and zeroes when comparing the communication channel input, *In* , and the buffer output, *Out*) is much better.

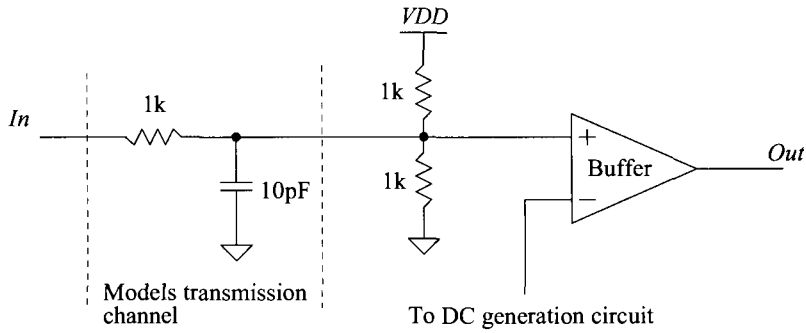

Figure 18.30 Reducing the input resistance of the input buffer.

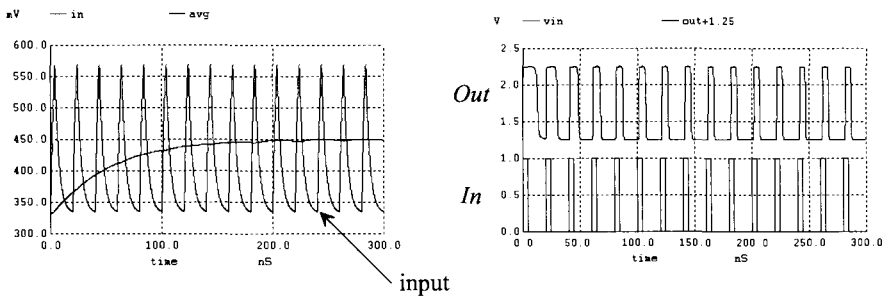

Figure 18.31 How reducing the input resistance of the buffer reduces the input signal amplitude (bad) and distortion (good).

Figure 18.32 shows an alternative low input resistance input buffer. When the input goes high, M1 turns on and M4 shuts off. This causes M2 to turn on and M5 to shut off. The output then goes high. When the input goes low, M1 turns off and M4 turns on (with M2 shutting off and M5 turning on). The result: the output goes low. Again, the power burned by M1 and M4 can be high if the transistors aren't sized properly. Further, the input swing is limited to a threshold voltage away from the supply voltages. This reduces the input voltage swing and further enhances the speed.

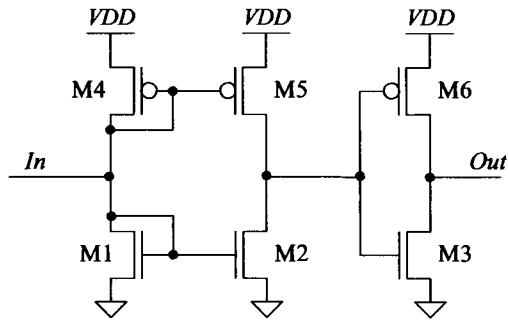

Figure 18.32 A low-input resistance input buffer.

18.4 Charge Pumps (Voltage Generators)

Often, when designing CMOS circuits, positive and negative DC voltages are needed that do not lie between ground and *VDD*. An example of an application where a larger DC voltage source is needed was seen in Ch. 16 when we discussed Flash memory (see Fig. 16.59). A simple circuit, sometimes called a voltage pump (or more often, a *charge pump*), useful in generating a voltage greater than *VDD*, is seen in Fig. 18.33.

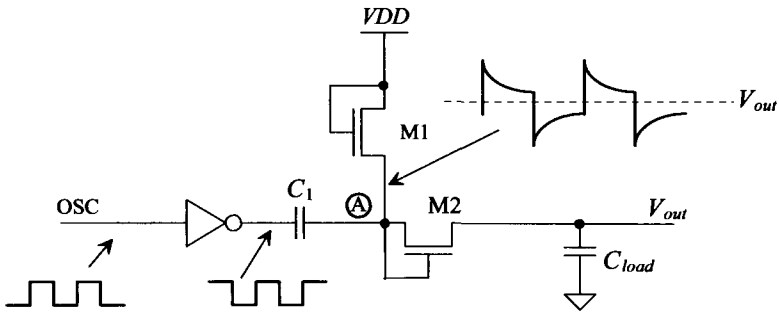

Figure 18.33 Pump used to generate a voltage greater than *VDD*.

The operation of the voltage pump of Fig. 18.33 can be explained by first realizing that both M1 and M2 operate like a diode. M1 is simply used to pull point A to a voltage of $VDD - V_{THN}$. M2 allows the charge from C_1 to charge C_{load} but not vice-versa. Let's begin the description of the circuit operation by assuming that the output of the inverter is low and point A is at a potential of $VDD - V_{THN}$. When the output of the inverter goes high, the potential at point A increases to $VDD + (VDD - V_{THN}) = 2 \cdot VDD - V_{THN}$. This turns on M2 and charges C_{load} to $2 \cdot (VDD - V_{THN})$, [an extra V_{THN} because of M2's gate-source voltage drop], provided $C_1 >> C_{load}$ and the oscillator frequency allows the capacitors to fully charge or discharge before changing states. In most practical situations, C_{load} and C_1 are comparable in size, and the output of the pump is loaded with a

DC load. The result is an output voltage with a startup time; that is, V_{out} does not immediately rise to $2 \cdot (VDD - V_{THN})$ but requires several oscillator cycles to reach steady state. Also, the output has a ripple dependent on the DC load. Figure 18.34 shows the simulation results for the circuit of Fig. 18.13 using 10/1 NMOS (scale factor of 50 nm) with $C_{load} = C_1 = 1$ pF and an oscillator frequency of 10 MHz. Using this simple pump with a DC load, such as a resistor, may require employing larger MOSFETs and capacitors to avoid excessive voltage droop.

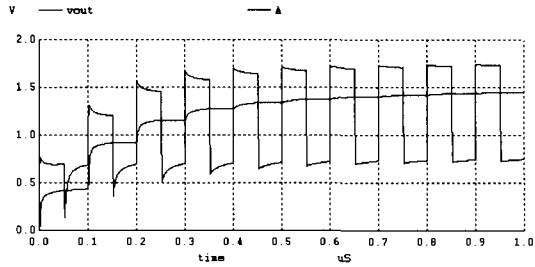

Figure 18.34 Simulating the operation of the voltage pump in Fig. 18.33.

Negative Voltages

The positive voltage pump uses n-channel MOSFETs, while the negative voltage pump, Fig. 18.35, uses p-channel MOSFETs. The reason for this comes from the requirement that the diode formed with the n+ (p+) implant used in the drain/source of the MOSFET combined with the p-substrate (n-well) does not become forward-biased. Forward biasing this parasitic diode is an *important concern* and is often the reason why some more exotic pump topologies can't be implemented. For example, in Fig. 18.35, we connect the well of the PMOS devices to ground instead of to their respective sources. Consider what would have happened had we connected the well to the source of the MOSFET. When the output voltage goes negative, the (n-type) well goes negative too. If the substrate (p-type) is at ground, this forward biases the n-well to substrate diode acting to clamp the output of the pump at a negative diode drop. While we could have left the bodies of the PMOS (the n-wells) tied to *VDD*, here we chose to connect them to ground so that the body effect wasn't so severe (a lower threshold voltage).

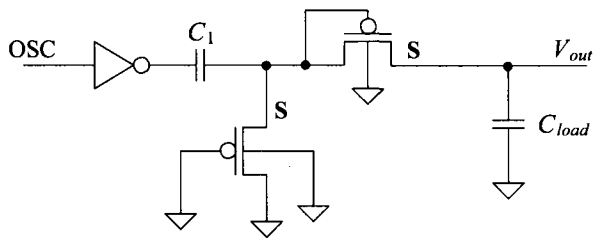

Figure 18.35 Negative voltage pump.

Using MOSFETs for the Capacitors

The capacitors used in Figs. 18.33 and 18.35 can be replaced with MOSFETs. An example of using n-channel MOSFETs in place of the capacitors in Fig. 18.33 is shown in Fig. 18.36. The main requirement on a MOSFET used as a capacitor is that its V_{GS} remain greater than V_{THN} at all possible operating conditions. In other words, the MOSFET must remain in the strong inversion region so that its capacitance is a constant $C'_{ox} \cdot W \cdot L$. The capacitor, C_{load}, in Fig. 18.36 remains in strong inversion because $V_{out} >> V_{THN}$. The capacitor C_1 remains in strong inversion because, when the inverter output is low, the voltage on the gate of C_1 is $VDD - V_{THN}$ (= V_{GS}). When the output of the inverter is high (VDD), the voltage on the gate of C_1 is $2 \cdot VDD - V_{THN}$. In both cases (the output of the inverter high and low), $V_{GS} = VDD - V_{THN}$, and the MOSFET is in the strong inversion region.

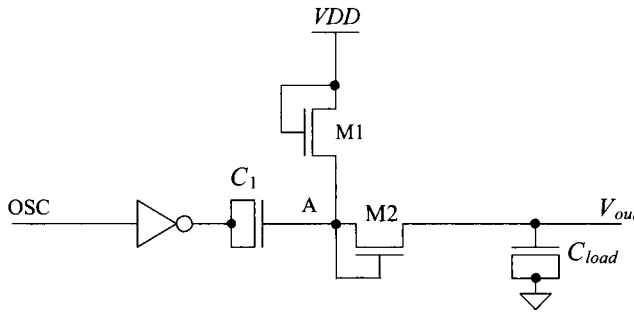

Figure 18.36 Using MOSFETs as capacitors.

18.4.1 Increasing the Output Voltage

Figure 18.37 shows a voltage pump with a higher output voltage. The increase in the output voltage comes from eliminating the threshold voltage drop at the gate and drain of M7. This allows the output to swing up to $2 \cdot VDD - V_{THN}$.

To understand the operation of the circuit, let's assume that the voltage at point A is low and the voltage at point C is $VDD - V_{THN}$. When the output of INV1 goes high, point A is VDD and the voltage at point C swings up to $2 \cdot VDD - V_{THN}$. This causes M4, M5, and M6 to turn on and pull points D and E to VDD. Now when point B goes high (point A goes back to zero), points D and E swing up to $2 \cdot VDD$ and the output goes to $2 \cdot VDD - V_{THN}$. Note that MOSFETs M2 and M3 are not needed; unless the pump drives a DC load , they never turn on. Also, separating points D and E is unnecessary unless the pump supplies a DC current.

18.4.2 Generating Higher Voltages: The Dickson Charge Pump

The voltage pumps of the last section are limited to voltages less than $2 \cdot VDD$ and greater than $-2 \cdot VDD$. Figure 18.38 shows a scheme for generating arbitrarily high voltages (limited by the breakdown voltage of the capacitors or the oxide breakdown of the MOSFETs). Again, the MOSFETs are used as diodes in this configuration.

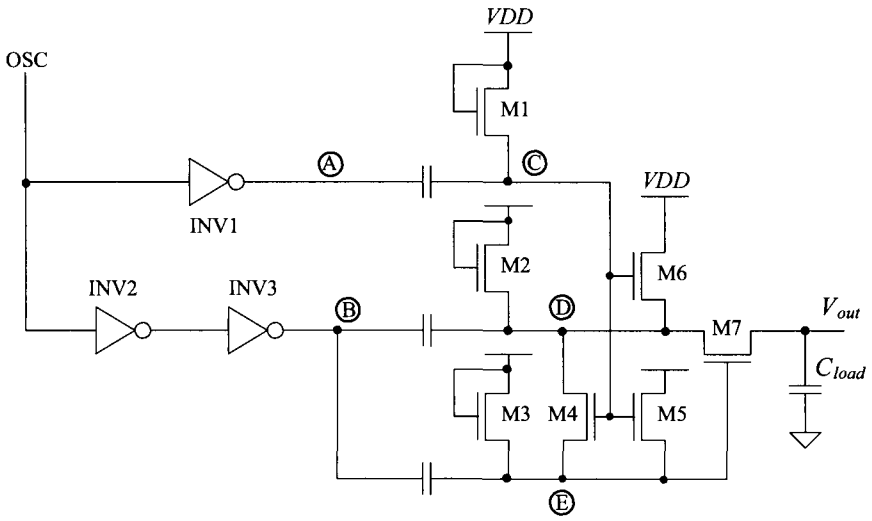

Figure 18.37 Increased output voltage pump.

In the following description of circuit operation, we assume steady-state operation with no DC load present. When CLK is low, point A is pulled, by M1, to $VDD - V_{THN}$. When CLK goes high, point A swings up to $2 \cdot VDD - V_{THN}$. Diode M2 turns on, and point B charges to $2 \cdot VDD - 2 \cdot V_{THN}$. When CLK goes low, $\overline{\text{CLK}}$ goes high and point B swings up to $3 \cdot VDD - 2 \cdot V_{THN}$. When $\overline{\text{CLK}}$ goes low, point B swings back down to $2 \cdot VDD - 2 \cdot V_{THN}$. This operation proceeds through the circuit to the last stage of the multiplier. The output of the multiplier swings from $(N+1) \cdot VDD - N \cdot V_{THN}$ down to $N \cdot VDD - N \cdot V_{THN}$. C_N can be made larger than the other capacitors to reduce this ripple.

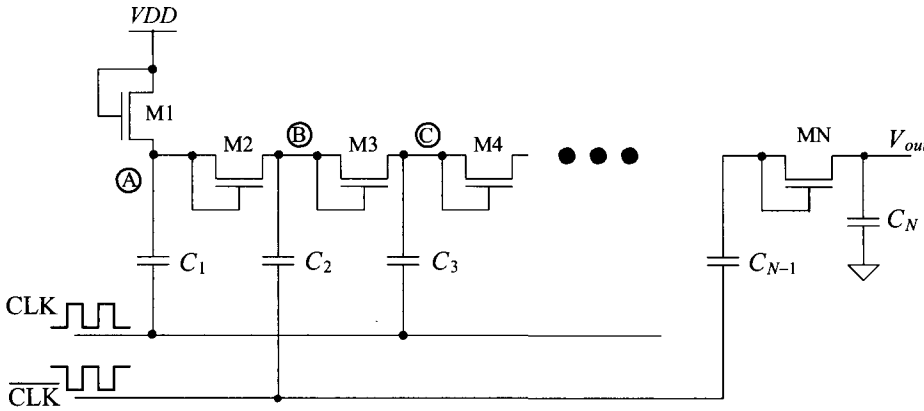

Figure 18.38 N-stage voltage multiplier (the Dickson charge pump).

Clock Driver with a Pumped Output Voltage

To fully turn on NMOS switches, a driver configuration is needed with a pulsed output voltage greater than $VDD + V_{THN}$ (with body effect). One such configuration is seen in Fig. 18.39. When the input to the circuit is a logic low, the output of INV1 is a high and the output of INV2 is a low. Node B in the figure is at roughly *VDD*, and node A is at roughly 2*VDD*. M1 is off and M2 is on. The output of the driver is a logic low (ground). When the input of the circuit goes high, the output of INV1 goes low. This causes node A to go to *VDD*. The output of INV2 goes high, and node B boots up to 2*VDD* (M1 on M2 off). The output of the driver circuit then goes to 2*VDD* as well. Notice that one side of the cross-coupled NMOS devices is sized smaller than the other side. This is to minimize layout area and power (the charging and discharging of the parasitic capacitors doesn't waste power). Node A doesn't supply any power to the output of the circuit. It is simply used to turn M2 on so that node B is precharged to *VDD* when the input to the circuit is low. A larger capacitor is used on node B because the charge that goes to load must be supplied by this capacitor. If the output load capacitance gets large, then the size of this capacitor must be increased. When designing the driver, it's a good idea to characterize the performance as a function of the load capacitance.

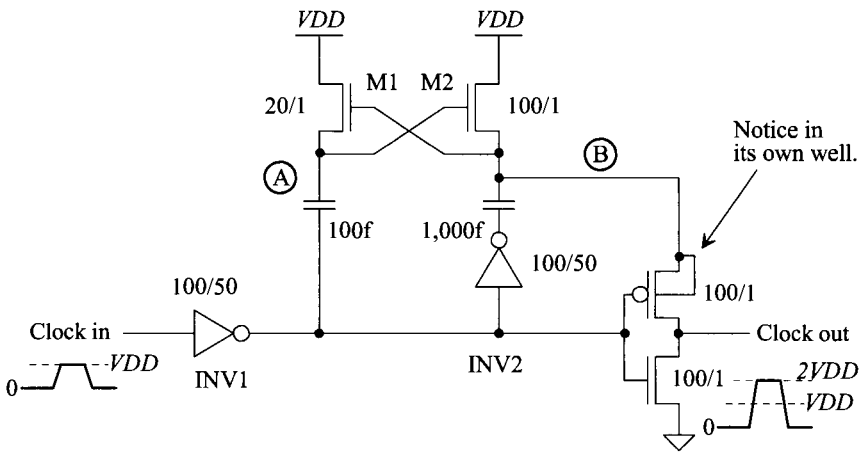

Figure 18.39 Charge-pump clock driver.

NMOS Clock Driver

Figure 18.40a shows an NMOS bootstrapped inverter. This circuit is useful to avoid latch-up since an n-well isn't present. The pull-up device, Mpu, is made 4 times longer than the pull-down device, Mpd, so that the output voltage can swing closer to ground. The transistor, Mc, is used as a capacitor to "boot" the gate of Mpu above *VDD* so that it can turn fully on and drive the output to *VDD*. Md is used as a diode, as in the other charge pumps seen in this chapter, to ensure that the boot node doesn't drop below $VDD - V_{THN}$. Note that this isn't a static circuit, that is, the input must be active else the high output voltage is only $VDD - 2V_{THN}$. In order to avoid continuous current flow when both Mpd and Mpu are conducting the NMOS "clock" driver (a buffer) seen in Fig. 18.40b can be used. The 40/1 output devices are both actively driven.

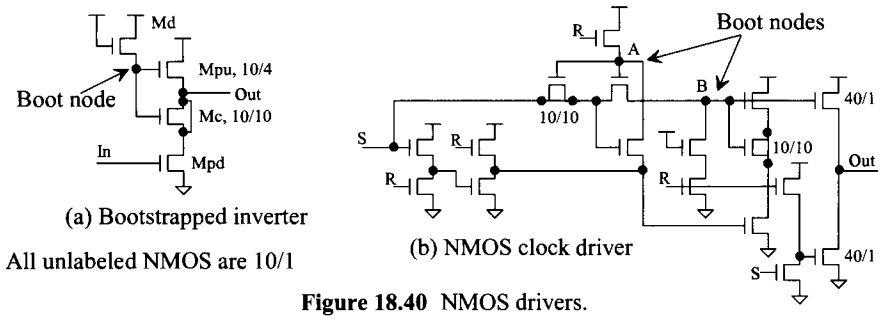

Figure 18.40 NMOS drivers.

18.4.3 Example

A common application of a voltage generator in digital circuits is generating a negative substrate bias; that is, instead of tying the substrate to ground, the substrate is held at some negative voltage. Typically, this negative voltage is between –0.5 and –1 V. "Pumping" the substrate negative is found in some DRAMs. A negative substrate bias has several benefits. It (1) stabilizes n-channel threshold voltages, (2) increases latch-up immunity after power up, (3) prevents forward biasing n+ to p-substrate pn junction, (4) allows chip inputs to go negative without forward biasing a pn junction, (5) prevents substrate from going locally above ground, (6) reduces depletion capacitances associated with the n+ to p-substrate junction, and (7) reduces subthreshold leakage current.

A simple substrate pump is shown in Fig. 18.41. In this circuit we can use n-channel MOSFETs to generate a negative potential, unlike Fig. 18.35, since the negative voltage is connected to the substrate. In this situation, the drain/source implants of the n-channel MOSFETs cannot become forward biased. Note the absence of the load capacitance. It turns out that the capacitance of the substrate to everything else in the circuit presents a very large capacitance to the pump. In other words, the substrate itself is a very large capacitor.

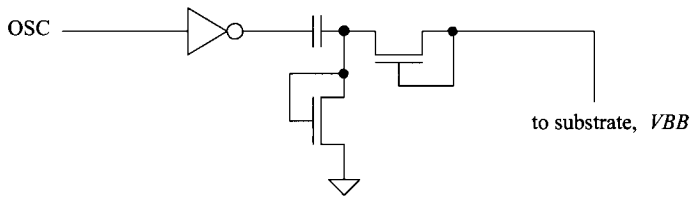

Figure 18.41 Simple substrate pump.

An example oscillator circuit that is used to drive the substrate pump is shown in Fig. 18.42. This is a standard ring oscillator with a NAND gate to enable/disable the oscillator. Capacitors are added at a few points in the middle of the oscillator to increase the delay and lower the frequency of the oscillator so that the pump's capacitors fully charge.

The final component in a substrate pump is the regulator, a circuit that senses the voltage on the substrate and enables or disables the substrate pump (the oscillator). Using

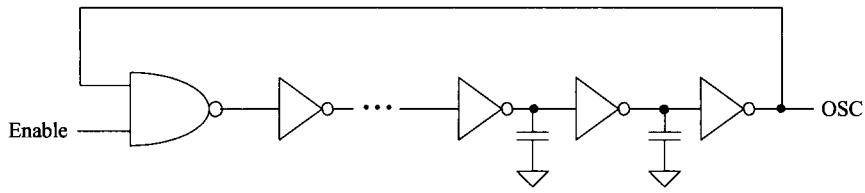

Figure 18.42 Ring oscillator with enable.

a comparator with hysteresis, a precision voltage reference, and a level shifting circuit, the enable signal can be generated with the circuit of Fig. 18.43. The hysteresis of the comparator determines the amount of ripple on the substrate voltage. Forcing a constant current through the two MOSFETs, M1 and M2, compels their source-gate voltages to remain constant (note how the body effect is eliminated by using p-channel MOSFETs), causing the MOSFETs to behave as if they were batteries. The battery action of M1 and M2 shifts the substrate voltage up so that it lies in the input range of the comparator. The number of MOSFETs (in this case two) and the magnitude of the current I determine the substrate voltage.

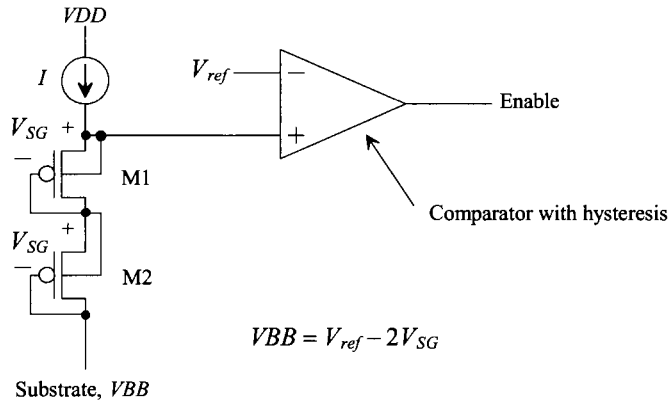

Figure 18.43 Regulator circuit used in substrate pump.

A simpler and less accurate implementation of the regulator is shown in Fig. 18.44. The comparator and voltage reference are implemented with an inverter and M1–M3. MOSFET M3 causes the inverter to have hysteresis, that is, behave like a Schmitt trigger. MOSFETs M1 and M2 form an inverter with a switching point voltage of approximately V_{THN}. The current source of Fig. 18.43 is implemented with the long L MOSFET M4 in Fig. 18.44. The level shifting is performed with the n-channel MOSFETs M5 and M6. When point A gets above a potential of V_{THN}, the Enable output goes high, causing the substrate pump to turn on and drive the substrate voltage negative. When point A gets pulled, via the substrate voltage through M5 and M6, below V_{THN}, the Enable output goes low and the pump shuts off. The substrate voltage generated with this circuit is approximately $-V_{THN}$ with body effect.

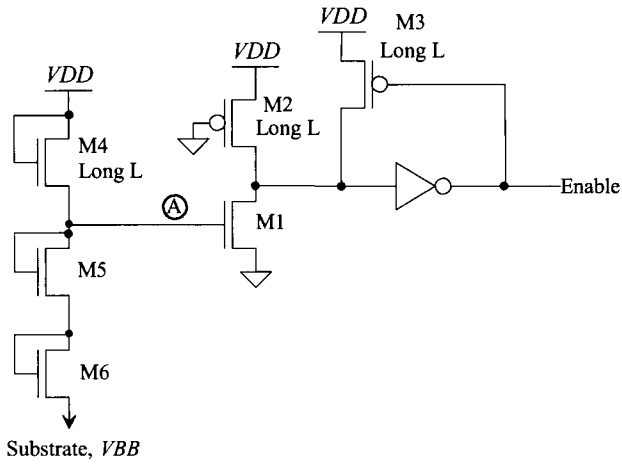

Figure 18.44 Simpler substrate regulator.

ADDITIONAL READING

[1] R. J. Baker, "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," US Patent 7,102,932, September 5, 2006.

[2] F. Pan and T. Samaddar, *Charge Pump Circuit Design*, McGraw-Hill, 2006. ISBN 978-0071470452.

[3] H. Lin, N.-H. Chen, and J. Lu, "Design of Modified Four-Phase CMOS Charge Pumps for Low-Voltage Flash Memories," *Journal of Circuits, Systems, and Computers*, Vol. 11, No. 4, pp. 393-403, 2002. Excellent paper.

[4] N. Otsuka and M. A. Horowitz, "Circuit techniques for 1.5-V power supply flash memory," *IEEE Journal of Solid-State Circuits,* Vol. 32, pp. 1217–1230, August 1997.

[5] M. Bazes, "Two Novel Full Complementary Self-Biased CMOS Differential Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 2, pp. 165-168, February 1991.

[6] J. F. Dickson, "On-Chip High-Voltage Generation in MNOS (sic) Integrated Circuits Using an Improved Voltage Multiplier Technique," *IEEE Journal of Solid State Circuits*, Vol. SC-11, No. 3, June 1976.

[7] J. Millman and H. Taub, *Pulse, Digital, and Switching Waveforms*, McGraw-Hill Publishers, 1965. ISBN 07-042386-5. Information on multivibrators and oscillators.

[8] O. H. Schmitt, "A Thermionic Trigger," *Journal of Scientific Instruments*, Vol. XV, pp. 24–26, No. 1, Jan. 1938. Information on the "Schmitt trigger."

PROBLEMS

For the following problems use the short-channel CMOS process with a scale factor of 50 nm and a *VDD* of 1 V.

18.1 Design a Schmitt trigger with V_{SPL} = 0.35 and V_{SPH} = 0.55 V. Use SPICE to verify your design.

18.2 Estimate t_{PHL} and t_{PLH} for the Schmitt trigger of Ex. 18.1, driving a 100 fF load capacitance. Compare your hand calculations to simulation results.

18.3 Design and simulate the operation of a Schmitt trigger-based oscillator with an output frequency of 10 MHz. Simulate the design using SPICE.

18.4 Estimate the total input capacitance on the control voltage input for the VCO shown in Fig. 18.8.

18.5 Design an astable multivibrator with an output oscillation frequency of 20 MHz.

18.6 Design and simulate the operation of a one-shot that has an output pulse width of 100 ns. Comment on the maximum rate of retrigger and how ESD diodes connected to bonding pads will affect the circuit operation if the resistor and capacitor are bonded out.

18.7 Design and simulate a 100 MHz oscillator using the astable multivibrator in Fig. 18.11. Comment how process shifts in the resistor and capacitor affects the oscillation frequency. If the resistor and capacitor are bonded out, will the ESD diodes affect the circuit's operation?

18.8 Using the buffer seen in Fig. 18.23 to drive a load capacitance of 100 *fF*, plot the propagation delays against the *Vinp* input signal amplitude when *Vinm* is 250, 500, and 700 mV. (*Vinp* is centered around *Vinm.*)

18.9 The DC restore circuit seen in Fig. 18.28 has limitations, such as it stops working if a long string of 1s or 0s is applied to the input buffer or the input data moves too quickly and the long RC time constants keep the DC restore output from following the center of the data. Comment, with the help of SPICE simulation results, on these limitations. Show how changing the values of the resistors and capacitors can compensate for these limitations. (For example, using longer time constants allows for longer strings of ones are zeroes before the DC restore signal is invalid.)

18.10 Using the model for the transmission channel seen in Figs. 18.26 and 18.30, show that the circuit in Fig. 18.32 will work as an input buffer. Using SPICE show the limitations of the buffer (signal amplitude and speed). Also, comment on the power pulled by the buffer.

18.11 Design a nominally 2 V voltage generator that can supply at most 1 μA of DC current (2 MEG resistor). Simulate the operation of your design with SPICE.

18.12 Design and simulate the operation of a nominally –1 V substrate pump. Comment on the design trade-offs.