Chapter

20

Current Mirrors

In this chapter we turn our attention towards the design, layout, and simulation of current mirrors (a circuit that sources [or sinks] a constant current). As we observed back in Fig. 9.1, and the associated discussion, the ideal output resistance, r_o, of a current source is infinite. Achieving high output resistance (meaning that the output current doesn't vary much with the voltage across the current source) will be the main focus of this chapter.

It's very important that the reader first understand the material in Ch. 9 concerning the selection of biasing currents and device sizes and how they affect the gain/speed of the analog circuits. We'll use the parameters found in Tables 9.1 and 9.2 in many of the examples in this chapter.

20.1 The Basic Current Mirror

The basic NMOS current mirror, made using M1 and M2, is seen in Fig. 20.1. Let's assume that M1 and M2 have the same width and length and note that $V_{GS1} = V_{DS1} = V_{GS2}$. Because the MOSFETs have the same gate-source voltages, we expect (neglecting channel-length modulation) them to have the same drain current. If the two resistors in the drains of M1/M2 are equal, the drain of M2 will be at the same potential as the drain of M1 (this is important). By matching the size, V_{GS}, and I_D of two transistors, we are assured that the two MOSFETs have the same drain-source voltage, ($V_{GS1} = V_{DS1} = V_{GS2} = V_{DS2}$).

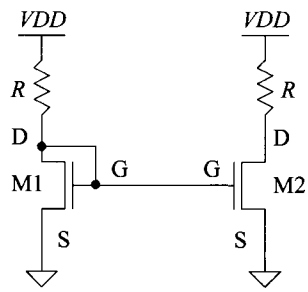

Figure 20.1 A basic current mirror.

20.1.1 Long-Channel Design

Examine Fig. 20.2. In this figure we show a current mirror and the equivalent circuit representation of a current source. Looking at M1, we can write

$$I_{REF} = I_{D1} = \frac{KP_n}{2}\frac{W_1}{L_1}(V_{GS1} - V_{THN})^2(1 + \lambda(V_{DS1} - V_{DS1,sat})) \qquad (20.1)$$

knowing $V_{DS1} = V_{GS1}$ and $V_{DS1,sat} = V_{GS1} - V_{THN}$. For M2, we write

$$I_O = I_{D2} = \frac{KP_n}{2}\frac{W_2}{L_2}(V_{GS1} - V_{THN})^2(1 + \lambda(V_O - V_{DS1,sat})) \qquad (20.2)$$

noting $V_{GS1} = V_{GS2}$, $V_{DS1,sat} = V_{DS2,sat}$, and V_O is the voltage across the current source. Looking at the ratio of the drain currents, we get

$$\frac{I_O}{I_{REF}} = \frac{W_2/L_2}{W_1/L_1} \cdot \frac{1 + \lambda(V_O - V_{DS1,sat})}{1 + \lambda(V_{DS1} - V_{DS1,sat})} \qquad (20.3)$$

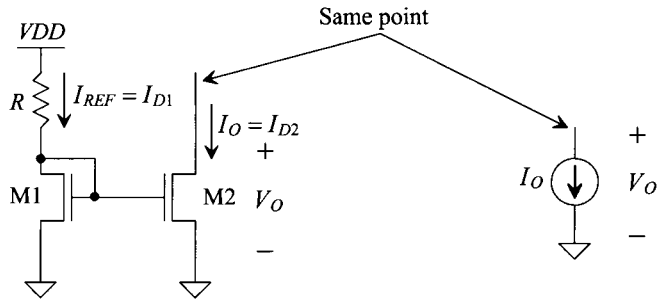

Figure 20.2 The current mirror and how we think about it.

Generally, the lengths of the devices in the current mirror are equal (let's assume they are for the moment). If, also at this time, we don't concern ourselves with channel-length modulation ($\lambda = 0$), we get a very useful result, that is,

$$\frac{I_O}{I_{REF}} = \frac{W_2}{W_1} \qquad (20.4)$$

By simply scaling the width of M2, we can adjust the size of our output current. Figure 20.3 shows an example of this scaling (using PMOS devices).

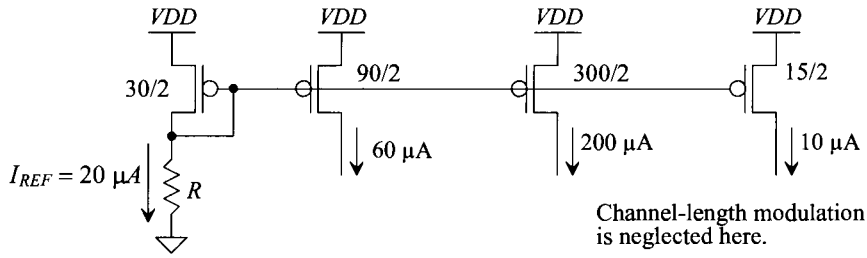

Figure 20.3 How current mirrors are ratioed.

Example 20.1

Determine the value of the resistor, R, needed in Figs. 20.2 and 20.3 so that the reference drain currents are 20 μA. Use the long-channel parameters seen in Table 9.1. Simulate the operation of the NMOS mirror with the calculated resistor value.

In Fig. 20.2 (the NMOS current mirror), we can write

$$I_{REF} = 20\ \mu A = \frac{VDD - V_{GS1}}{R} \approx \frac{KP_n}{2} \cdot \frac{10}{2} \cdot \left(\overbrace{V_{GS1}}^{1.05\ V} - \overbrace{V_{THN}}^{0.8} \right)^2 = \frac{KP_n}{2} \cdot \frac{10}{2} \cdot (0.25)^2$$

(notice how we indicate "approximately" because channel-length modulation is not included in the equations) or

$$R = \frac{5 - 1.05}{20\ \mu A} \approx 200\ k\Omega$$

For Fig. 20.3 (the PMOS current mirror), we can write

$$I_{REF} = 20\ \mu A = \frac{VDD - V_{SG}}{R} \approx \frac{KP_p}{2} \cdot \frac{30}{2} \left(\overbrace{V_{SG}}^{1.15\ V} - \overbrace{V_{THP}}^{0.9} \right)^2 = \frac{KP_p}{2} \cdot \frac{30}{2} \cdot (0.25)^2$$

or

$$R = \frac{5 - 1.15}{20\ \mu A} \approx 200\ k\Omega$$

Simulation of the operation of the NMOS current mirror is seen in Fig. 20.4. The reference current isn't exactly 20 μA (and we shouldn't expect it to be). The x-axis is a sweep of the voltage across the current source, V_O. Note that below $V_{DS,sat}$ (= 250 mV here) M2 triodes and the output current, I_O , goes to zero. The output *compliance* range for this current source (the range of output voltages where the current source behaves like a current source, that is, not an open or a resistor) is between VDD and $V_{DS,sat}$. The point where $V_O = V_{DS1} = V_{GS1}$ is where $I_O = I_{REF}$ (again this is important for matching two currents). Finally, note that I_{REF} and V_{GS1} are not dependent on V_O. ■

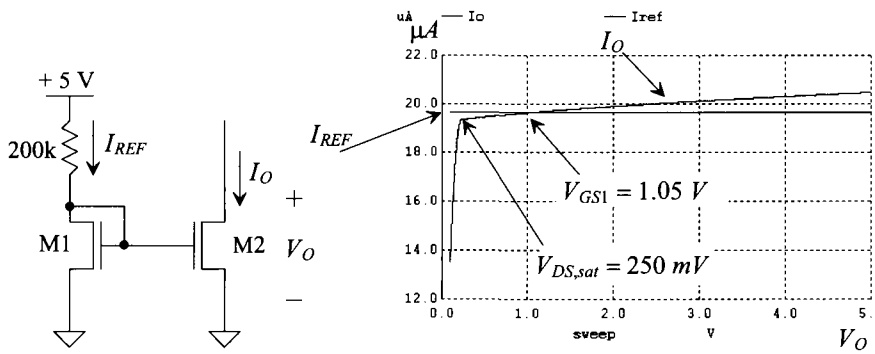

Figure 20.4 The operation of an NMOS current mirror.

20.1.2 Matching Currents in the Mirror

Many analog applications are susceptible to errors due to layout. In circuits in which devices need to be matched, layout becomes a critical factor. For example, in the basic current mirror shown in Fig. 20.2, first-order process errors can cause the output current, I_O, to be significantly different from the reference current. Process parameters such as gate-oxide thickness, lateral diffusion, oxide encroachment, and oxide charge density can drastically affect the performance of a device. Layout methods can be used to minimize the first-order effects of these parameter variations.

Threshold Voltage Mismatch

In a given current mirror application, the values for the threshold voltages are critical in determining the overall accuracy of the mirror. Again, examine the basic current mirror shown in Fig. 20.2. Since both devices have the same value for V_{GS} and assuming the sizes and transconductance parameters for both devices are equal, let's examine the effect of a mismatch in threshold voltages between the two devices. If it is assumed that the threshold mismatch is distributed across both devices such that

$$V_{THN1} = V_{THN} - \frac{\Delta V_{THN}}{2} \tag{20.5}$$

$$V_{THN2} = V_{THN} + \frac{\Delta V_{THN}}{2} \tag{20.6}$$

where V_{THN} is the average value of V_{THN1} and V_{THN2} and ΔV_{THN} is the mismatch, then

$$\frac{I_O}{I_{REF}} = \frac{\frac{KP_n}{2}\frac{W}{L}(V_{GS} - V_{THN} - \frac{\Delta V_{THN}}{2})^2}{\frac{KP_n}{2}\frac{W}{L}(V_{GS} - V_{THN} + \frac{\Delta V_{THN}}{2})^2} = \frac{\left[1 - \frac{\Delta V_{THN}}{2(V_{GS} - V_{THN})}\right]^2}{\left[1 + \frac{\Delta V_{THN}}{2(V_{GS} - V_{THN})}\right]^2} \tag{20.7}$$

If both expressions are squared and the higher order terms are ignored, then the first-order expression for the ratio of currents becomes

$$\frac{I_O}{I_{REF}} \approx 1 - \frac{2\Delta V_{THN}}{V_{GS} - V_{THN}} = 1 - \frac{2\Delta V_{THN}}{V_{DS,sat}} \tag{20.8}$$

Equation (20.8) is quite revealing because it shows that as V_{GS} decreases, the difference in the mirrored currents increases due to threshold voltage mismatch. This is particularly critical for devices that are separated by relatively long distances because the threshold voltage is susceptible to process gradients. *To attain high speed and to reduce the effects of threshold voltage mismatch, a large gate overdrive voltage should be used* (remembering for a long-channel process that $V_{ovn} = V_{DS,sat} = V_{GS} - V_{THN}$). Of course the drawback, for a current mirror, is a reduced range of compliance (the MOSFET enters the triode region earlier).

Transconductance Parameter Mismatch

The same analysis can be performed on the transconductance parameter, KP_n. If $KP_{n1} = KP_n - \Delta KP_n/2$ and $KP_{n2} = KP_n + \Delta KP_n/2$, where KP_n is the average of KP_{n1} and KP_{n2}, then assuming perfect matching on all other parameters, the difference in the currents becomes

$$\frac{I_O}{I_{REF}} = \frac{KP_n + 0.5\Delta KP_n}{KP_n - 0.5\Delta KP_n} \approx 1 + \frac{\Delta KP_n}{KP_n} \tag{20.9}$$

Since KP_n is a process parameter, we might think that as CMOS scales downwards (C'_{ox} goes up) the mismatch due to oxide variations and mobility differences might get better. However, there is less averaging of these variations with the smaller layout sizes. Practically, as we're about to see, differences in V_{DS} dominate the matching behavior.

Drain-to-Source Voltage and Lambda

One aspect of current mirror design that is *critical* for generating accurate currents is the drain-to-source voltage. As seen in Fig. 20.4, the only point where the currents of the devices are actually the same is when their V_{DS} values are equal. In Eq. (20.3) the ratio of the output current to the reference current is affected by both the matching in the drain-to-source voltages (V_O and V_{DS1}) and the device λs. If, for example in the short-channel process (see Table 9.2), $V_{DS1} = .35$ V, $V_{DS2} = V_O = .75$ V, and $\lambda_1 = \lambda_2 = 0.6$ V^{-1}, then

$$\frac{I_O}{I_{REF}} = \frac{1+\lambda_2 \cdot V_O}{1+\lambda_1 \cdot V_{DS1}} = \frac{1+0.6 \cdot 0.75}{1+0.6 \cdot 0.35} = 1.20 \qquad (20.10)$$

resulting in 20% error! It is extremely important, for good matching, that the V_{DS} values of the MOSFETs in the current mirror are equal.

Layout Techniques to Improve Matching

Most general analog applications require the length of the gate to be longer than minimum since the channel-length modulation, λ , has less effect on longer devices than on shorter ones (as discussed in Ch. 9). As a result, the minimum-sized devices found in digital circuits are not used as often in general analog design (however, see Ch. 26). However, the larger devices can result in larger parasitics if some layout issues are not considered. Figure 20.5a illustrates a basic MOSFET device with a large *W/L*. The implant resistance of the source and drain can be modeled as shown in Fig. 20.5b. The implant resistance can easily be reduced by simply adding as many contacts as possible along the width of both the source and the drain as seen in Fig. 20.5c. The increase in the number of contacts results in lower resistance, more current capability, and a more distributed current load throughout the device. However, as the device width increases, another technique is used which distributes the parasitics (both resistive and capacitive) into smaller contributions.

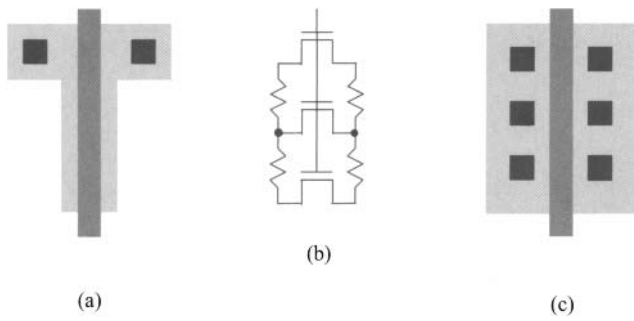

Figure 20.5 (a) Large device with a single contact and (b) its equivalent circuit. (c) Adding more contacts to reduce parasitic resistance.

Examine Fig. 20.6. In this figure, a single device with a large W/L is split into several parallel devices, each with a width one-fourth of the original W. One result of splitting the device into several parts is smaller overall parasitic capacitance associated with the reverse-biased implant substrate diode (the drain or source depletion capacitance to substrate). Since values of C_{db} and C_{sb} are proportional to W, the split device reduces these parasitics by a factor of $(n + 1)/2n$ where n is the number of parallel devices and is odd. If n is even, then the C_{sb} is reduced by one-half and C_{db} is reduced by $(n + 2)/2n$. As seen in Fig. 20.6b, putting the devices in parallel also reduces the parasitic resistance in series with both the source and the drain (it gets cut roughly in half too).

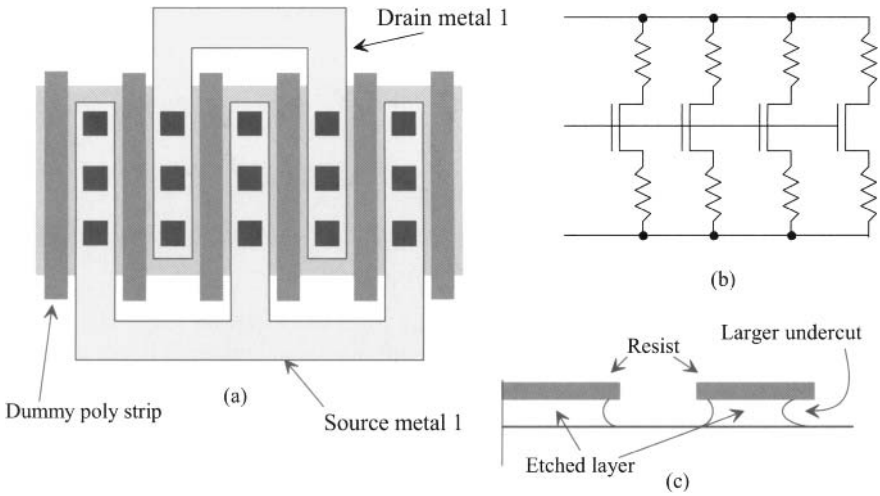

Figure 20.6 (a) A parallel device with dummy strips, (b) the equivalent circuit, and (c) undercutting.

Notice also, that Fig. 20.6a has dummy poly strips on both sides of the device. These strips are used to help minimize the effects of undercutting the poly on the outer edges after patterning, Fig. 20.6c. If the dummy strips had not been used, the poly would have been etched out more under the outermost gates, resulting in a mismatch between the four parallel devices.

When matching two devices, it is imperative that the two devices be as symmetrical as possible. Always orient the two devices in the same direction, unlike those illustrated in Fig. 20.7.

Splitting the devices into parallel devices and interdigitizing them can distribute process gradients across both devices and thus improve matching. An example of this is seen in Fig. 20.8. In (a) the current mirror seen in (b) is laid out. Each MOSFET in (b) is split up into four MOSFETs. If the W/L of each MOSFET in (b) is 80/2, then the size of each MOSFET (finger) in (a) is 20/2. Note the use of dummy poly strips on this layout. A good exercise at this point is to lay out the mirror of Fig. 20.8 in a common-centroid arrangement (see Ch. 5). Using a large layout area (long lengths and wide widths) and common-centroid layouts can result in significant improvements in matching.

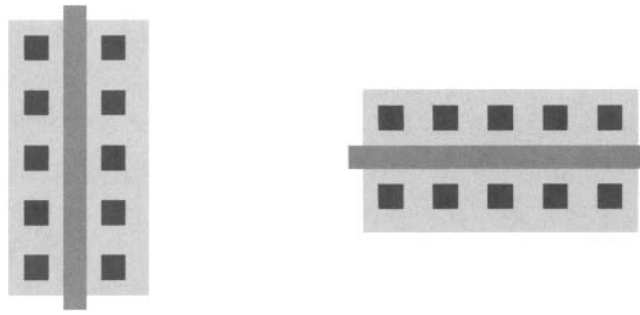

Figure 20.7 Devices with differing orientation (bad).

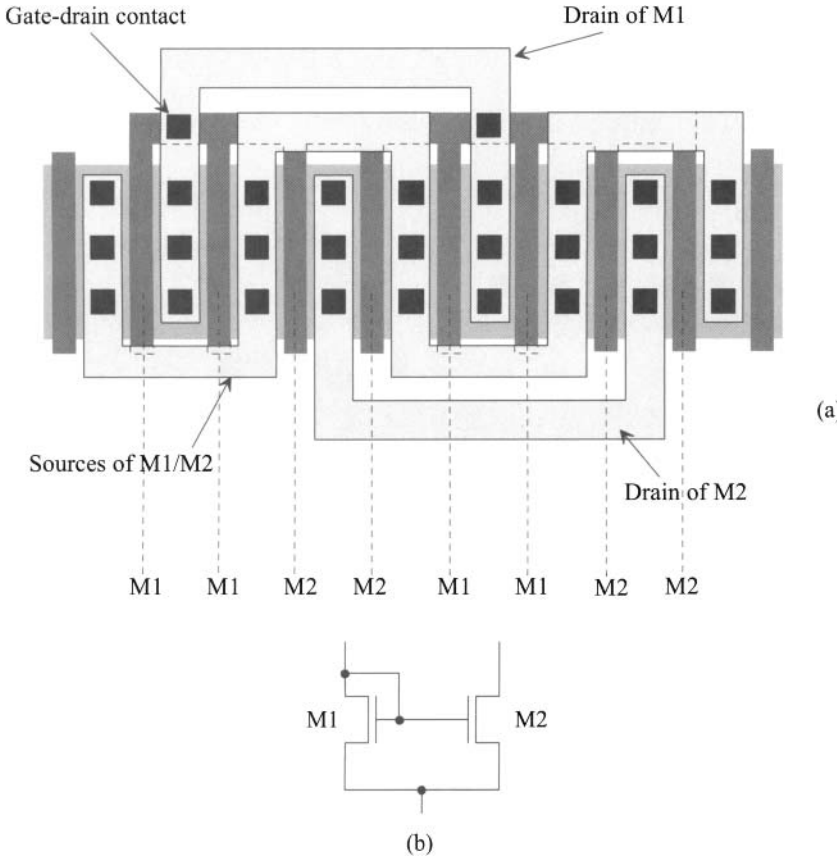

Figure 20.8 (a) Layout of a simple current mirror using interdigitation and (b) equivalent circuit.

Layout of the Mirror with Different Widths

When laying out the current mirror, the lateral diffusion, L_{diff}, under the gate oxide (Fig. 5.13) and the oxide encroachment, W_{enc}, can affect the actual length and width, respectively, of the MOSFET. If not careful with the layout, this will affect the mirror's ratio. Equation 20.3 can be rewritten, without including the differences due to drain-source voltage and lambda, as

$$\frac{I_O}{I_{REF}} = \frac{(W_{2drawn} - 2W_{enc}) \cdot (L_{1drawn} - 2L_{diff})}{(W_{1drawn} - 2W_{enc}) \cdot (L_{2drawn} - 2L_{diff})} \qquad (20.11)$$

If the requirement that $L_{1drawn} = L_{2drawn}$ is imposed, then the widths of the devices determine the relative currents in the mirror. Figure 20.9a shows a current mirror layout without width compensation. If W_{enc} is 0.1, then for this layout,

$$\frac{I_O}{I_{REF}} = \frac{40 - .2}{20 - .2} = 2.01 \text{ (a 1\% error due to poor layout)}$$

Figure 20.9b shows how to lay out a current mirror to avoid these problems. The layout of M2 is two MOSFETs in parallel. This can be specified in SPICE by adding M = X after the MOSFET statement in the netlist, where X is the number of MOSFETs,

```
M1    Vd1   Vd1   0    0    NMOS    L=2   W=20
M2    Vd2   Vd1   0    0    NMOS    L=2   W=20   M=2
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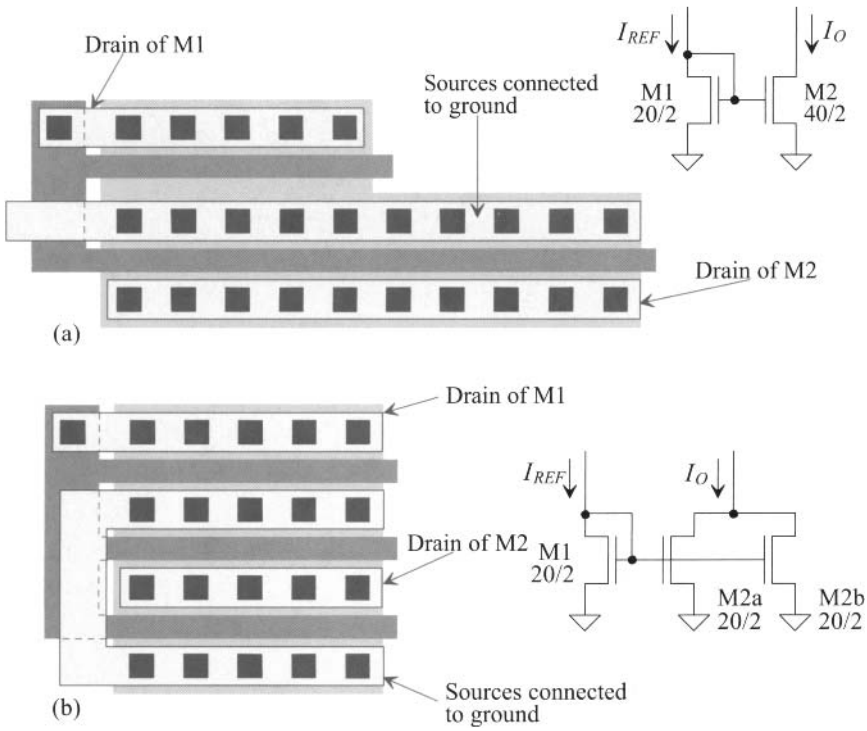


Figure 20.9 Layout of a current mirror (a) without width correction and (b) with width correction.

20.1.3 Biasing the Current Mirror

Using a resistor to set the bias current, as seen in Figs. 20.2–20.4, can result in currents that are too dependent on the power supply value and temperature. Consider the current mirror seen in Fig. 20.10a. In this design we've used the sizes and bias current given in Table 9.2 (the short-channel CMOS process) to select the resistor. In particular, $V_{SG} = 0.35\ V$ so the gate potential is 0.65 *V*. Figure 20.10b shows how the reference and output currents vary if *VDD* is swept from 900 mV to 1 V. The reference current is linearly dependent on *VDD* (as seen in Ex. 20.1). The output current is dependent on both the reference current and the V_{DS} (λ) of M2. In general, we want a reference current that isn't dependent on power supply or ground variations (noise). This is an important point. Consider the following example.

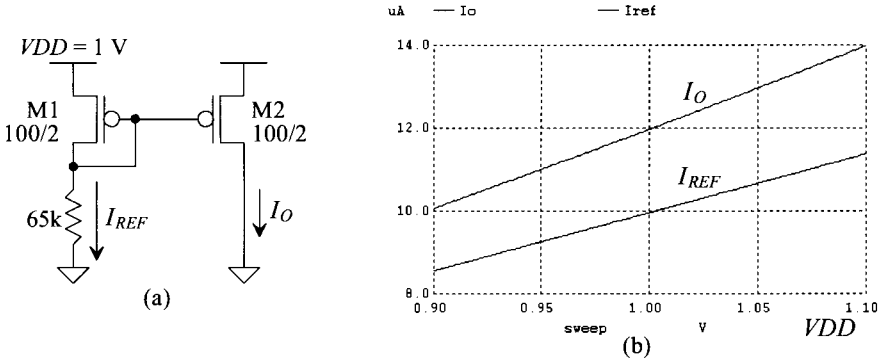


Figure 20.10 How reference and output current vary with VDD.

Example 20.2

Regenerate Fig. 20.10 if the 65k resistor is replaced with an ideal 10 μA current source, Fig. 20.11a. Explain the results.

The simulation results are seen in Fig. 20.11b. Note how the output current variation with *VDD* is much better than what is seen in Fig. 20.10. The reference current through M1 is, of course, a constant. The output current is larger than the

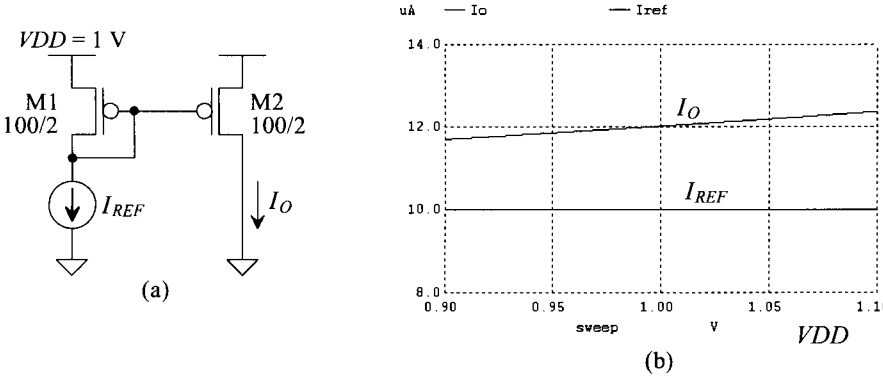


Figure 20.11 Showing that VDD variations don't affect the reference current.

reference current because $V_{SD1} < V_{SD2}$ (notice how often this point is coming up in the design of current mirrors). The reason I_O varies is due to the finite output resistance ($\lambda \neq 0$) of M2, Eq. (20.2).

The point of this example is that it is desirable to have a bias current that doesn't vary with changes in *VDD* or ground. ■

Using a MOSFET-Only Reference Circuit

Let's try replacing the resistor bias with a MOSFET, Fig. 20.12. If we assume long-channel behavior, then

$$VDD = V_{SG3} + V_{GS1} \tag{20.12}$$

or

$$VDD = \sqrt{\frac{2I_{REF}}{KP_p \frac{W_3}{L_3}}} + V_{THP} + \sqrt{\frac{2I_{REF}}{KP_n \frac{W_1}{L_1}}} + V_{THN} \tag{20.13}$$

If we are going to think of M3 as a resistor, as in Fig. 20.2, so that we mirror the current in M1, then we solve for the size of M3. Using the data from Table 9.1, we get

$$5 = \sqrt{\frac{2 \cdot 20}{40 \cdot \frac{W_3}{L_3}}} + 0.9 + \sqrt{\frac{2 \cdot 20}{120 \cdot \frac{10}{2}}} + 0.8 \rightarrow \frac{W_3}{L_3} = 0.11 \approx \frac{10}{90} \tag{20.14}$$

If we are going to think of M1 as a resistor, as in Fig. 20.10a, so that we mirror the current in M3, then we solve for the size of M1 as we did in Eq. (20.14) and get

$$\frac{W_1}{L_1} \approx \frac{10}{270} \tag{20.15}$$

Figure 20.13 shows the operation of these MOSFET bias circuits with *VDD* swept from 4.5 to 5.5 V. Note that, at 5 V, we should have a bias current of 20 μA. What we get is 14 μA. The reason that we have such a large difference is due to neglecting the output resistance of the MOSFETs (and the effects of mobility degradation). Note that the sensitivities, how the output current changes with *VDD*, are roughly 8 μA/V. (Let's compare this to hand-calculated values of sensitivity next.)

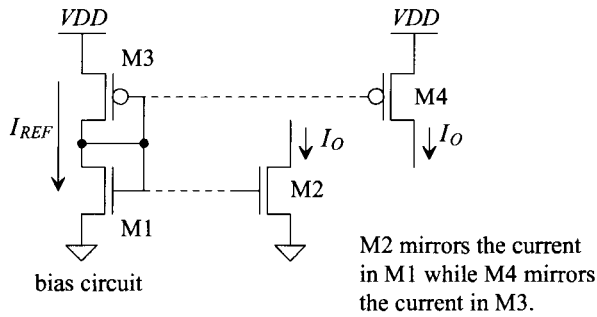


Figure 20.12 A MOSFET-only bias circuit.

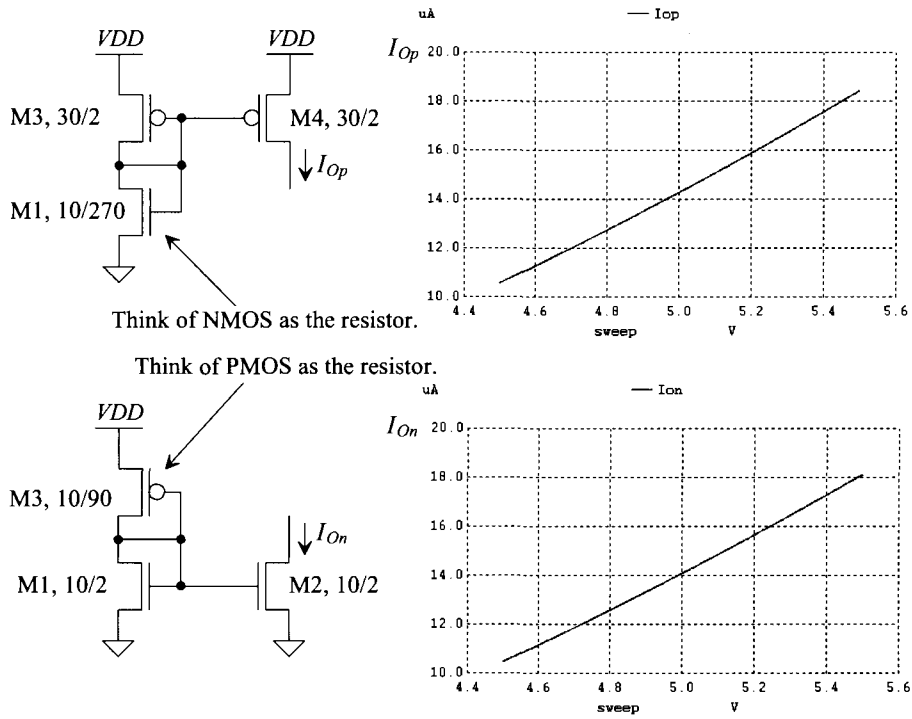


Figure 20.13 Behavior of MOSFET-only bias circuits with changes in VDD.

To determine I_{REF}'s sensitivity to *VDD*, let's take the derivative of the I_{REF} in Eq. (20.13) with respect to *VDD*. First let's write

$$(VDD - V_{THN} - V_{THP})^2 = I_{REF} \cdot \overbrace{\left[\sqrt{\frac{2L_3}{KP_p \cdot W_3}} + \sqrt{\frac{2L_1}{KP_n \cdot W_1}}\right]^2}^{K} \tag{20.16}$$

and next

$$\frac{\partial I_{REF}}{\partial VDD} = \frac{2 \cdot VDD}{K} - \frac{2 \cdot (V_{THN} + V_{THP})}{K} \tag{20.17}$$

Using the values in Table 9.1 and Eqs. (20.14) or (20.15), K is approximately 547×10^3 V^2/A so

$$\frac{\partial I_{REF}}{\partial VDD} = 12\ \mu A/V \tag{20.18}$$

For every millivolt change in *VDD* (around *VDD* = 5 V), we get 12 nA change in I_{REF}. As a comparison from Ex. 20.1, we can write (assuming the change in V_{GS} with *VDD* small)

$$\frac{\partial I_{REF}}{\partial VDD} \approx \frac{1}{R} = \frac{1}{200k} = 5\ \mu A/V \tag{20.19}$$

For every millivolt change in *VDD* we get 5 nA change in bias current.

Supply Independent Biasing

Instead of putting the resistor in the drain side of the current mirror, let's consider placing it in the source side, Fig. 20.14a. One of the problems with this approach is that if we try to mirror the current in M2 using M5 we won't know the value of the mirrored current. It's not obvious how V_{GS2} and V_{GS5} are related. In (b) we add a diode connected M1 so that its current can be mirrored (by M5). The next question is how do we force the same current through both M1 and M2? Figure 20.14c shows the addition of a PMOS current mirror to do this. From (c) we can write

$$V_{GS1} = V_{GS2} + I_{REF} \cdot R \tag{20.20}$$

which can only be valid if $V_{GS1} > V_{GS2}$. To ensure that this is the case, we use a larger value of β in M2, that is, we *multiply-up* M1's β in M2 so that less gate-source voltage is needed to conduct I_{REF}. Generally, this is done by simply using a larger width in M2. The resulting circuit is called a *Beta-multiplier* reference circuit. Knowing

$$V_{GS} = \sqrt{\frac{2I_D}{\beta}} + V_{THN} \tag{20.21}$$

$\left(\beta = KP_n \cdot \frac{W}{L}\right)$ and

$$\beta_2 = K \cdot \beta_1 \text{ (which is satisfied by } W_2 = K \cdot W_1) \tag{20.22}$$

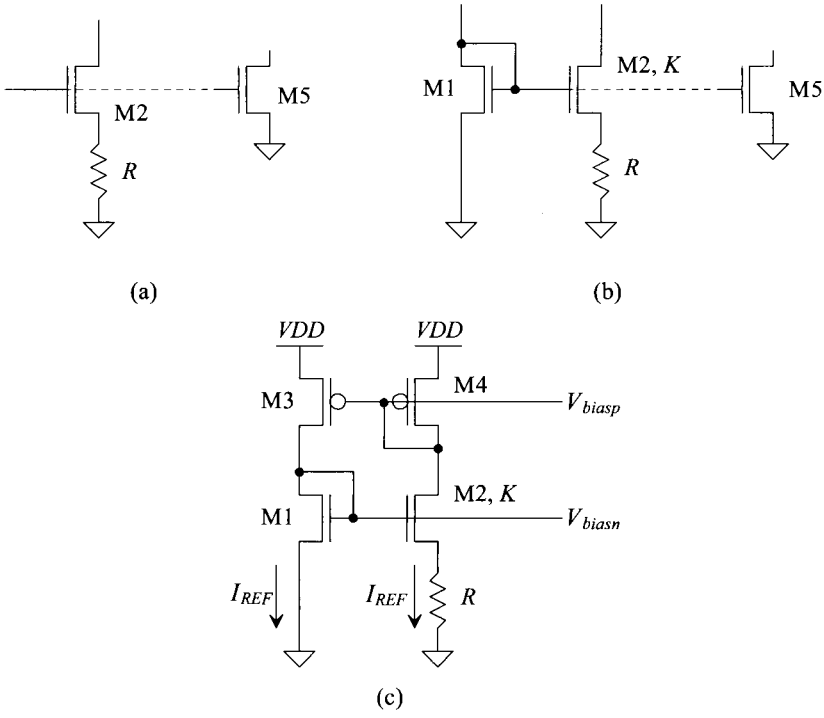


Figure 20.14 Developing the Beta-multiplier reference.

we can write

$$I_{REF} = \frac{2}{R^2 KP_n \cdot \frac{W_1}{L_1}}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \text{ or } V_{DS,sat} = V_{GS} - V_{THN} = \frac{2}{R \cdot KP_n \cdot \frac{W_1}{L_1}}\left(1 - \frac{1}{\sqrt{K}}\right) \quad (20.23)$$

It's important to note I_{REF} and V_{ovn} ($= V_{GS} - V_{THN}$), neglecting the finite output resistance of the MOSFETs which wasn't included in the derivation of Eq. (20.23), are independent of *VDD*. Solving for R with the values given in Table 9.1 and a K of 4 gives $R = 6.5\ k\Omega$. Note that this circuit, when $K = 4$, is sometimes called a *constant-g_m* bias circuit because

$$g_m = \sqrt{2KP_n \frac{W}{L} \cdot I_{REF}} = \frac{1}{R} \quad (20.24)$$

a constant independent of MOSFET process shifts. Figure 20.15 shows the schematic of a bias circuit based on the sizes, bias currents, and $V_{DS,sat}$ given in Table 9.1.

Note that a "start-up circuit" was included in Fig. 20.15. In any self-biased circuit there are two possible operating points: the one we just described and the unwanted one where zero current flows in the circuit. This unwanted state occurs when the gates of M1/M2 are at ground while the gates of M3/M4 are at *VDD*. When in this state, the gate of MSU1 is at ground and so it is off. The gate of MSU2 is somewhere between *VDD* and $VDD - V_{THP}$. MSU3, which behaves like an NMOS switch, turns on and leaks current into the gates of M1/M2 from the gates of M3/M4. This causes the current to snap to the desired state and MSU3 to turn off. *Note that during normal operation the start-up circuit should not affect the Beta-multiplier's operation.* The current through MSU3 should be zero (or very small).

The Beta-multiplier is an example of a circuit that uses positive feedback. The addition of the resistor kills the closed loop gain (a positive feedback system can be stable if its closed loop gain is less than one). However, if we decrease the size of the resistor, we increase the gain of the loop and push the feedback system closer to instability. An example of when this could occur is if the parasitic capacitance on the source of M2 to ground is large (effectively shorting M2's source to ground). If the resistor, for example, is bonded out off-chip to set the current, it is likely that this bias circuit will oscillate.

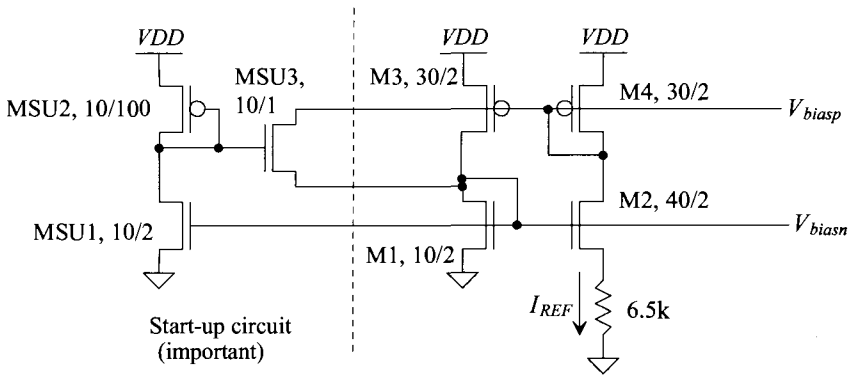


Figure 20.15 Beta-multiplier reference for biasing in the long-channel process described in Table 9.1.

Figure 20.16 shows how the reference currents through M1 and M2 vary with *VDD*. The minimum value of *VDD* can be estimated by looking at the minimum value of voltage across the drain-source of M3 and M1. For M3 this is $V_{SD3,sat}$ or 250 mV (because we are using the parameters from Table 9.1 in the design of this current reference). For M1 this is $V_{DS1} = V_{GS1} = 1.05$ V. We can then write

$$VDD_{\min} = V_{SD3,sat} + V_{GS1} = 1.3\ V \tag{20.25}$$

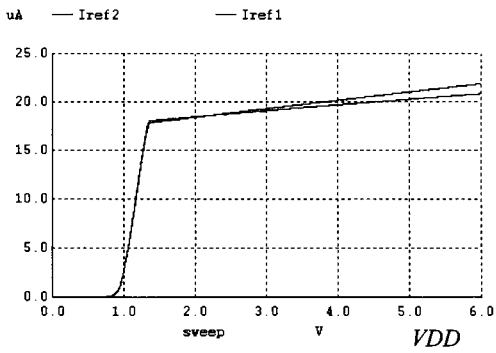


Figure 20.16 The reference currents through M1 and M2 in the Beta-multiplier.

Finally, the sensitivity of I_{REF} is directly dependent on the output resistance of the MOSFETs. From the simulations

$$\frac{\partial I_{REF}}{\partial VDD} \approx 800\ nA/V$$

or almost an order of magnitude better than the previous reference circuits

---

Example 20.3

Estimate the voltage on the gate of M6 and its drain current in Fig. 20.17.

M3 and M4 are biased to source 20 μA of current. Since $V_{GS1} = V_{GS2} = V_{DS1}$ (and M1/M2 have the same drain current, see Fig. 20.1 and the associated discussion), it follows that $V_{GS6} = V_{DS2} = V_{GS1} = 1.05$ V. *We treat M6, for biasing purposes, as if its gate were tied to the gates of M1 or M2.* It follows then that $I_{D6} = 20$ μA. ■

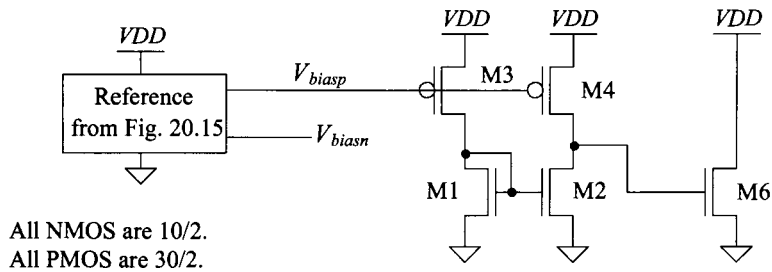


Figure 20.17 Circuit used in Ex. 20.3

20.1.4 Short-Channel Design

Figure 20.18 shows a Beta-multiplier biasing circuit based on the values given in Table 9.2 as well as simulation results showing how the reference currents vary with *VDD*. From Eq. (20.25) and Table 9.2 we would expect VDD_{min} to be 400 mV. At *VDD* = 1 V the reference currents are indeed 10 μA. However, what we see is a horrible sensitivity to changes in *VDD*. Reviewing Figs. 9.31 and 20.10 we see the low output resistance of the short-channel devices causes the drain current to change significantly with changes in drain-to-source voltage. In some analog applications this variation isn't that harmful. However, if the Beta-multiplier circuit is to behave like a true current reference, the reference currents shouldn't vary with changes in *VDD*.

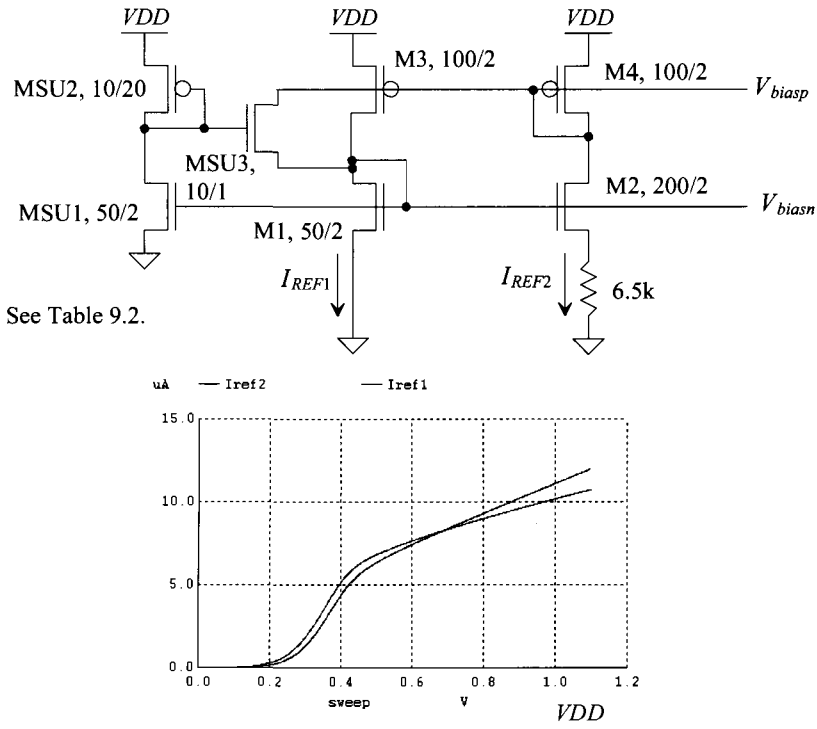


Figure 20.18 Beta-multiplier reference for short-channel design (see Table 9.2).

To reduce the sensitivity, we need to reduce the variations in the drain-to-source voltages of the NMOS devices with changes in *VDD*. Consider adding a differential amplifier (diff-amp) to the basic Beta-multiplier seen in Fig. 20.19. Note that M4 is no longer diode-connected so its drain can move to the same potential as M2's drain, that is, V_{biasn}. The start-up circuit (required) is not shown. The idea is to use the amplifier to compare the drain voltage of M1 (V_{biasn}) with the drain voltage of M2 (V_{reg}) and regulate them to be equal. The result is an effective increase in M2's output resistance. For example, if V_{reg} is above V_{biasn}, the amplifier's output voltage increases. This drives the

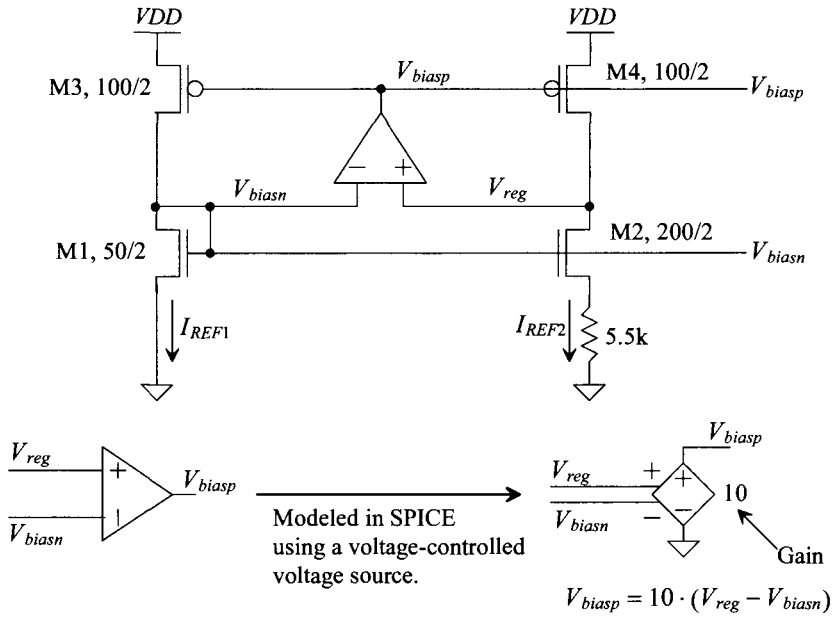


Figure 20.19 Increasing the output resistance of short-channel MOSFETs using feedback. The result, for the Beta-multiplier circuit, is better power supply sensitivity.

gate of M4 upwards, lowering the current it supplies and causing V_{reg} to drop back down. At the same time the gate of M3 is also increased, causing it to source less current. This causes a drop in V_{biasn} (the same as V_{reg} because of the symmetry as discussed in Fig. 20.1 or Ex. 20.3). Figure 20.20 shows how the reference current, in Fig. 20.19, changes with *VDD* when the added amplifier has a gain of 10. We've lowered R to 5.5k to more accurately set the current and used, in the simulation, a voltage-controlled voltage source for the amplifier.

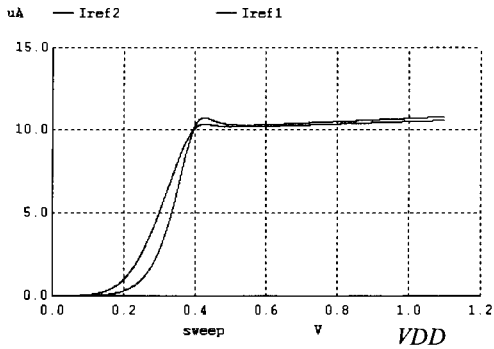


Figure 20.20 Improvement with the added amplifier.

Figure 20.21 shows a possible differential amplifier configuration. The PMOS devices form a current mirror while the NMOS devices will, when $V_{biasn} = V_{reg}$, simply mirror the current in M1. If $V_{biasn} \neq V_{reg}$ then the imbalance causes the amplifier output to swing up or down providing the desired action.

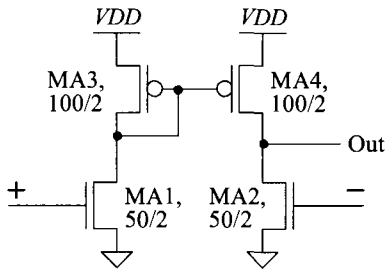
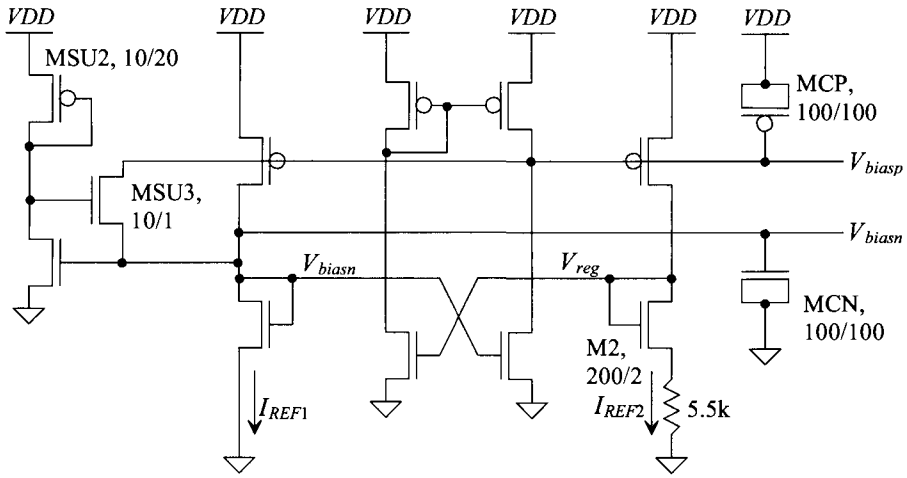


Figure 20.21 A possible implementation of the diff-amp in Fig. 20.19.

Figure 20.22 shows the improved current reference for use in a short-channel CMOS process (where devices have very low output resistances). The amplifier in Fig. 20.21 is placed in the reference, as indicated in Fig. 20.19. As with any feedback scheme, stability is of critical importance. As we'll see in the coming chapters, a feedback amplifier with only a single high-impedance node (meaning no diode-connected MOSFETs or MOSFET-source terminals are connected to the node) is straightforward to compensate (make stable). So that the reference has a single high-impedance node, that is V_{biasp}, we connected M2's gate to its drain (instead of to V_{biasn}). We get the same effect, as



All unlabeled NMOS are 50/2.
All unlabeled PMOS are 100/2.

Figure 20.22 Improved current reference for short-channel devices. See also Sec. 23.1.3 for more information.

seen in Fig. 20.19 but the gain around the loop is reduced. To make the reference stable, we add capacitors (MCP and MCN) to the circuit. The high-impedance node is the critical point for adding the compensation capacitor (that is MCP is the critical capacitance). If the reference drives a significant number of MOSFETs (so these driven MOSFETs provide the load capacitance), then MCP and MCN may be excluded from the design. Figure 20.23 shows how the reference currents change with *VDD*.

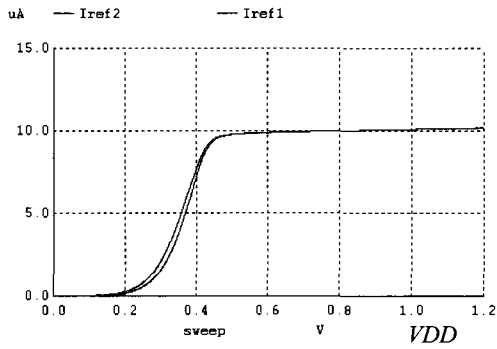
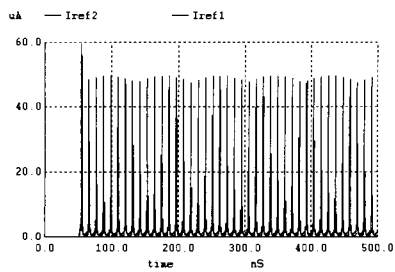


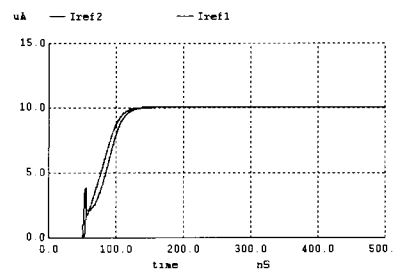
Figure 20.23 Variation of reference currents with VDD for the circuit in Fig. 20.22.

An Important Note

It's extremely important to understand that together with the benefits of better power supply sensitivity are the undesired traits of feedback, that is, the potential for an unstable circuit. For example, Fig. 20.24a shows what happens to the reference currents if we remove MCP and MCN in Fig. 20.22 and then apply a step voltage to *VDD* (that is, *VDD* steps from 0 to 1 V at 50 ns in the simulation). Clearly, the reference is not stable and the currents oscillate. In (b) we do the same thing but with MCP and MCN present. The response shows first-order behavior, and oscillations are not present. We might think we are done with the reference and move on to the other analog circuit designs. However, further characterization of the current reference using simulations is warranted. For example, what happens if *VDD* has a 50 mV squarewave signal coupled to it at 100 MHz? How does the reference behave with this signal (a squarewave *VDD* that oscillates between 1 and 1.05 V at 100 MHz)? In general, no analog circuit has good power supply noise rejection at high frequencies. To remedy this, the power supply is decoupled (a large capacitor is placed from *VDD* to ground to remove high-frequency noise).



(a) MCP and MCN not present



(b) MCP and MCN present

Figure 20.24 What happens when VDD is pulsed from 0 to 1 at 50 ns.

20.1.5 Temperature Behavior

While we've been focusing on how the reference current changes with *VDD,* it's also important to know how the current changes with temperature. Looking at the basic current mirror in Fig. 20.11a, note that if I_{REF} is a constant, independent of temperature, then the output current will also be independent of temperature. That's not to say that the MOSFET characteristics aren't changing because they are; they change at the same rate. Because they change together, the current mirror relationship is still valid and M2 mirrors the current in M1. Of course, if M1 is located at a different physical location than M2 and each is heated differently, a mismatch in the currents will result. *The point is that the temperature behavior of the reference current determines the temperature behavior of all mirrored currents.*

Using the short-channel CMOS parameters we know, from Ch. 9 (Fig. 9.30b), that the change in V_{THN} with temperature is –0.6 mV/C° (for an NMOS device). For the PMOS device we can vary temperature and look at the change in V_{THP}. Using the mirror in Fig. 20.11 and looking at the V_{SG} at different temperatures results in the plots seen in Fig. 20.25. We see that it also varies at a rate of –0.6 mV/C°.

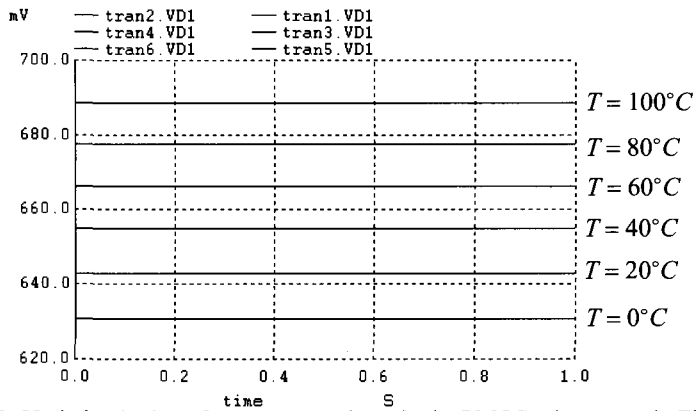


Figure 20.25 Variation in the reference gate voltage in the PMOS mirror seen in Fig. 20.11.

Resistor-MOSFET Reference Circuit

For a resistor-MOSFET reference circuit (Fig. 20.2), we can write (neglecting the MOSFET's finite output resistance)

$$I_{REF} = \frac{VDD - V_{GS}}{R} \tag{20.26}$$

The change in I_{REF} with temperature is

$$\frac{\partial I_{REF}}{\partial T} = -\frac{VDD - V_{GS}}{R^2} \cdot \frac{\partial R}{\partial T} - \frac{1}{R} \cdot \frac{\partial V_{GS}}{\partial T} \tag{20.27}$$

or

$$\frac{\partial I_{REF}}{\partial T} = -I_{REF} \cdot \frac{1}{R}\frac{\partial R}{\partial T} - \frac{1}{R} \cdot \frac{\partial V_{GS}}{\partial T} \tag{20.28}$$

We know that to write the reference current as a function of temperature we use

$$I_{REF}(T) = I_{REF}(T_0) \cdot (1 + TCI_{REF} \cdot (T - T_0)) \tag{20.29}$$

where the temperature coefficient of the reference current is

$$TCI_{REF} = \frac{1}{I_{REF}} \cdot \frac{\partial I_{REF}}{\partial T} \tag{20.30}$$

Rewriting Eq. (20.28) using Eq. (20.26) yields

$$TCI_{REF} = \frac{1}{I_{REF}} \cdot \frac{\partial I_{REF}}{\partial T} = -\frac{1}{R}\frac{\partial R}{\partial T} - \frac{1}{VDD - V_{GS}}\frac{\partial V_{GS}}{\partial T} \tag{20.31}$$

Noting, again, that the temperature coefficient is not a constant but rather changes with temperature (even though this isn't indicated in Eq. (20.29)) just like a small-signal parameter, e.g., g_m, changes with the DC operating point.

Example 20.4

Determine the temperature behavior of the reference current in the mirror seen in Fig. 20.10. Verify the answer with SPICE.

If the temperature coefficient of the resistor, $TCR = \frac{1}{R}\frac{\partial R}{\partial T} = 2000\ ppm/C^\circ$ (= 0.002) and we assume after looking at Fig. 9.30 that $\frac{\partial V_{GS}}{\partial T} \approx \frac{\partial V_{THN}}{\partial T} \approx -0.6\ mV/C^\circ$ then, knowing the parameters used in Table 9.2 were the basis for the design of the current mirror in Fig. 20.10,

$$TCI_{REF} = -0.002/C^\circ - \frac{1}{1 - 0.35} \cdot (-0.6\ mV/C^\circ) \approx -1{,}000\ ppm/C^\circ$$

and so

$$I_{REF}(T) = 10 \cdot (1 - 0.001 \cdot (T - 27))\ \mu A$$

At 100 C° the reference current is 9.27 μA and at 0 C° it's 10.27 μA (of course, the reference current is approximately 10 μA at 27 C°). Figure 20.26 shows the SPICE simulation results. ■

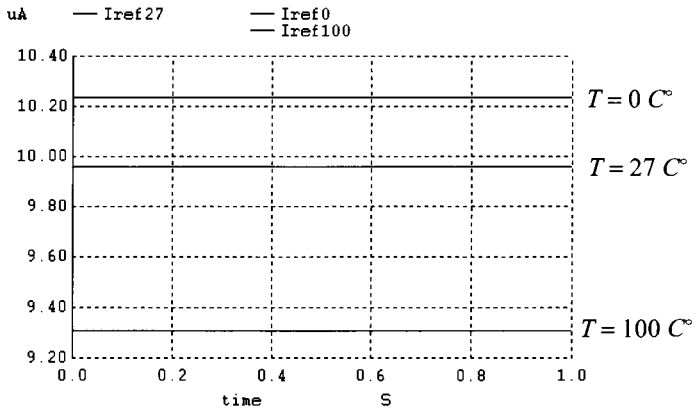


Figure 20.26 Example 20.4 showing the temperature behavior of the reference current in Fig. 20.10.

MOSFET-Only Reference Circuit

For the MOSFET-only bias circuit, Fig. 20.12, we can write the reference current as (see Eq. [20.16])

$$I_{REF} = \frac{VDD^2 - 2VDD \cdot (V_{THN} + V_{THP}) + (V_{THN} + V_{THP})^2}{\left(\sqrt{\frac{2L_3}{KP_p \cdot W_3}} + \sqrt{\frac{2L_1}{KP_n \cdot W_1}}\right)^2} \tag{20.32}$$

Knowing $KP_n = M \cdot KP_p$, where M is 3 for our long-channel process and 2 for our short-channel process (see Tables 9.1 and 9.2), we can write

$$I_{REF} = KP_n \cdot \frac{VDD^2 - 2VDD \cdot (V_{THN} + V_{THP}) + (V_{THN} + V_{THP})^2}{\left(\sqrt{\frac{M \cdot 2L_3}{W_3}} + \sqrt{\frac{2L_1}{W_1}}\right)^2} \tag{20.33}$$

or

$$\frac{\partial I_{REF}}{\partial T} = \frac{\partial KP_n}{\partial T} \cdot \frac{VDD^2 - 2VDD \cdot (V_{THN} + V_{THP}) + (V_{THN} + V_{THP})^2}{\left(\sqrt{\frac{M \cdot 2L_3}{W_3}} + \sqrt{\frac{2L_1}{W_1}}\right)^2} +$$

$$\frac{KP_n}{\left(\sqrt{\frac{M \cdot 2L_3}{W_3}} + \sqrt{\frac{2L_1}{W_1}}\right)^2} \cdot \left(-2VDD \cdot \left(\frac{\partial V_{THN}}{\partial T} + \frac{\partial V_{THP}}{\partial T}\right) + 2(V_{THN} + V_{THP})\left(\frac{\partial V_{THN}}{\partial T} + \frac{\partial V_{THP}}{\partial T}\right)\right) \tag{20.34}$$

Dividing both sides by Eq. (20.33) gives

$$\frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial T} = \frac{1}{KP_n} \frac{\partial KP_n}{\partial T} + \frac{2\left(\frac{\partial V_{THN}}{\partial T} + \frac{\partial V_{THP}}{\partial T}\right)(V_{THN} + V_{THP} - VDD)}{VDD^2 - 2VDD \cdot (V_{THN} + V_{THP}) + (V_{THN} + V_{THP})^2} \tag{20.35}$$

noting, from Eq. (9.52), that the first term is simply −1.5/T.

Example 20.5

Determine the temperature behavior of the reference current in the MOSFET-only bias circuit seen in Fig. 20.13.

We note that both references in Fig. 20.13 have the same temperature behavior since Eq. (20.35) doesn't show a width or length dependence (there is a dependence in the reference current though). Figure 20.13 used the long-channel MOSFET parameters from Table 9.1 where

$$V_{THN} = 0.8,\ V_{THP} = 0.9,\ \frac{\partial V_{THN}}{\partial T} = -1\ mV/C^\circ,\ \frac{\partial V_{THP}}{\partial T} = -1.4\ mV/C^\circ$$

and VDD = 5 V with I_{REF} = 13.5 μA (measured in the simulation that generated Fig. 20.13) at T = 300 K°. Plugging the numbers into Eq. (20.35) gives

$$TCI_{REF} = \frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial T} = -\frac{1.5}{300} + \frac{2(-0.0024)(-3.3)}{25 - 17 + 2.89} = -0.005 + 0.00146 \approx -3,500\ ppm/C^\circ$$

and so $I_{REF}(T) = 13.5(1 - 0.0035(T - T_0))\ \mu A$. ■

Temperature Behavior of the Beta-Multiplier

To determine the temperature behavior of the Beta-multiplier, we take the derivative of Eq. (20.23) with respect to temperature

$$\frac{\partial I_{REF}}{\partial T} = \frac{-4}{R^3 KP_n \cdot \frac{W_1}{L_1}}\left(1-\frac{1}{\sqrt{K}}\right)^2 \cdot \frac{\partial R}{\partial T} - \frac{2}{R^2 KP_n^2 \cdot \frac{W_1}{L_1}}\left(1-\frac{1}{\sqrt{K}}\right)^2 \frac{\partial KP_n}{\partial T} \quad (20.36)$$

Dividing both sides by I_{REF} (Eq. [20.23]) gives

$$TCI_{REF} = \frac{1}{I_{REF}} \cdot \frac{\partial I_{REF}}{\partial T} = -2\left(\frac{1}{R}\frac{\partial R}{\partial T}\right) - \frac{1}{KP_n}\frac{\partial KP_n}{\partial T} \quad (20.37)$$

Example 20.6

Determine the temperature behavior of the Beta-multiplier seen in Fig. 20.22.

If the temperature coefficient of the resistor, $TCR = \frac{1}{R}\frac{\partial R}{\partial T} = 2000\ ppm/C°$ then

$$TCI_{REF} = -0.004 + \frac{1.5}{300} = 1000\ ppm/C°$$

and so

$$I_{REF}(T) = 10 \cdot (1 + 0.001 \cdot (T - 27))\ \mu A$$

The positive TC of the resistor subtracts from the negative TC of the mobility to stabilize the current reference. If the mobility change with temperature is complicated by velocity saturation effects, then simulations become invaluable to determine the actual temperature performance of the circuit. ■

Voltage Reference Using the Beta-Multiplier

Let's try designing the Beta-multiplier where the gate voltage of M1 (see Figs. 20.15 or 20.22) is a constant independent of temperature. In this type of design we aren't using this voltage directly to bias anything so we'll change the label from V_{biasn} to V_{REF}. Using Eqs. (20.22) and (20.23) gives

$$V_{REF} = V_{GS1} = \frac{2}{R \cdot KP_n \cdot \frac{W}{L}}\left(1-\frac{1}{\sqrt{K}}\right) + V_{THN} \quad (20.38)$$

Taking the derivative with respect to temperature gives

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{THN}}{\partial T} - \frac{2}{R \cdot KP_n \cdot \frac{W}{L}}\left(1-\frac{1}{\sqrt{K}}\right) \cdot \left(\frac{1}{R}\frac{\partial R}{\partial T} + \frac{1}{KP_n} \cdot \frac{\partial KP_n}{\partial T}\right) \quad (20.39)$$

If we want the change with temperature to be zero, $\partial V_{REF}/\partial T = 0$, then we can select the resistor based on

$$R = \frac{2}{\frac{\partial V_{THN}}{\partial T} \cdot KP_n \cdot \frac{W}{L}}\left(1-\frac{1}{\sqrt{K}}\right) \cdot \left(\frac{1}{R}\frac{\partial R}{\partial T} + \frac{1}{KP_n} \cdot \frac{\partial KP_n}{\partial T}\right) \quad (20.40)$$

Using the parameters from Table 9.1 with $K = 4$ and a resistor temperature coefficient of 0.002 gives a resistor value of 5 kΩ. Figure 20.27 shows the SPICE simulation results. The variation is approximately 60 mV/100 C° or 600 μV/C°.

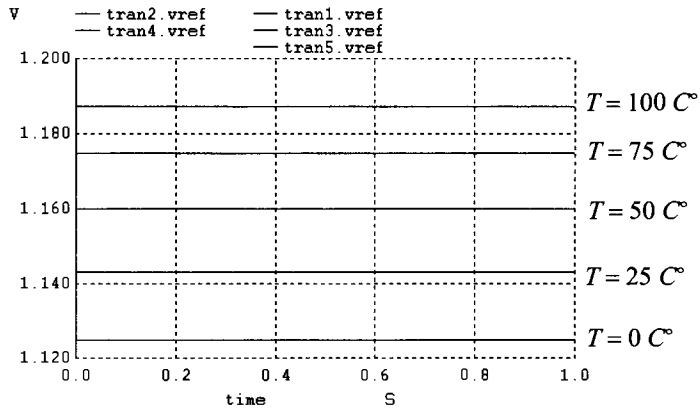


Figure 20.27 Temperature performance of a voltage reference using the Beta-multiplier.

20.1.6 Biasing in the Subthreshold Region

In some CMOS designs (for example, low-power designs) the MOSFETs may be operated in the weak or subthreshold regions. If a resistor is used to bias a current mirror, as seen in Fig. 20.10, its value can be very large. For example, if we use the short-channel process with VDD = 1 V and a V_{SG} of approximately V_{THP} (= 280 mV) with an I_D of 10 nA, we need a resistor with a value of

$$I_{REF} = \frac{VDD - V_{SG}}{R} \rightarrow R = 72\ M\Omega\ ! \tag{20.41}$$

Clearly, this isn't practical. To bias circuits for subthreshold operation, let's use the Beta-multiplier. From Eq. (9.17) we can write

$$V_{GS1} = nV_T \cdot \ln\left(\frac{I_{REF} \cdot L_1}{I_{D0} \cdot W_1}\right) + V_{THN} \tag{20.42}$$

and

$$V_{GS2} = nV_T \cdot \ln\left(\frac{I_{REF} \cdot L_1}{I_{D0} \cdot K \cdot W_1}\right) + V_{THN} \tag{20.43}$$

Knowing

$$I_{REF} = \frac{V_{GS1} - V_{GS2}}{R} \tag{20.44}$$

we get

$$I_{REF} = \frac{n \cdot V_T}{R} \cdot \ln K \tag{20.45}$$

or

$$R = \frac{n \cdot V_T}{I_{REF}} \cdot \ln K \tag{20.46}$$

Using the values above, that is, K = 4 and an I_{REF} of 10 nA, gives an R (assuming n = 1) of approximately 3.5 MΩ. Still large but much better than 72 MΩ.

20.2 Cascoding the Current Mirror

In this section we discuss increasing the output resistance of a current mirror so that it behaves more ideally. Figure 20.28 shows the problem with using a single MOSFET for a current source. Instead of being a constant, the output current, I_O, increases as the voltage across the current source, V_O, increases. We model this increase using the MOSFET's output resistance, r_o (see Table 9.2). If we can hold the drain-source voltage of the MOSFET constant, then the current doesn't vary. However, this requires a fixed V_O. To avoid this, we'll add circuitry in between the current-mirrored MOSFET and V_O.

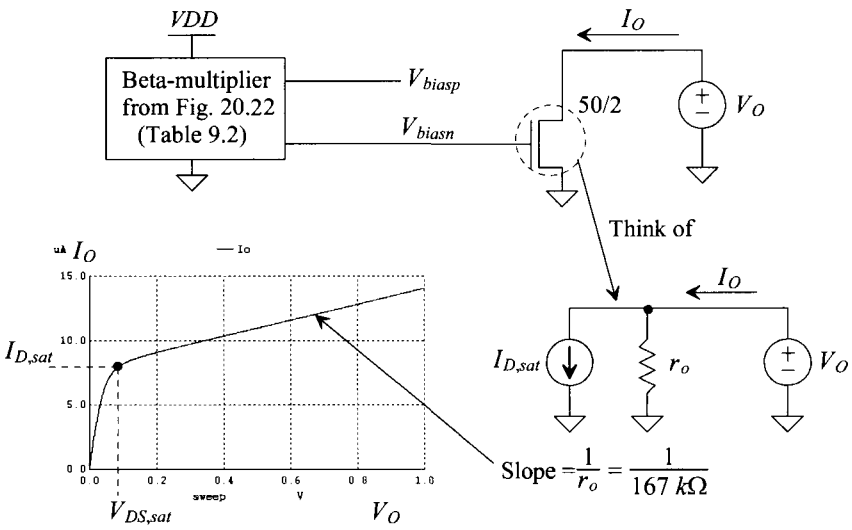


Figure 20.28 How the finite output resistance of the MOSFET affects the output current.

20.2.1 The Simple Cascode

The simple cascode current mirror made with M1–M4 is seen in Fig. 20.29. The name "cascode" is a vestige from the days of vacuum tubes when a common-cathode amplifier was cascaded (in series with) a common-grid amplifier. Drawing an analogy with MOSFETs, the cathode of a tube is equivalent to the source of a MOSFET. The grid of a tube corresponds to the gate of a MOSFET and the anode to the drain of the MOSFET.

It's important to realize that I_O is still determined by the gate-source voltages of M1 and M2. Changing the sizes of M3 and M4 simply changes the drain-source voltages of M1/M2, affecting the matching of their drain currents, as indicated by Eq. (20.10). Again, this (the gate-source voltages of M1/M2 determine the currents) is important to understand since, in the next several pages, we present different modifications to this basic cascode circuit. These modifications attempt to hold the drain source voltages of M1/M2 more constant to increase the current mirror's output resistance (make I_O change less with changes in V_O).

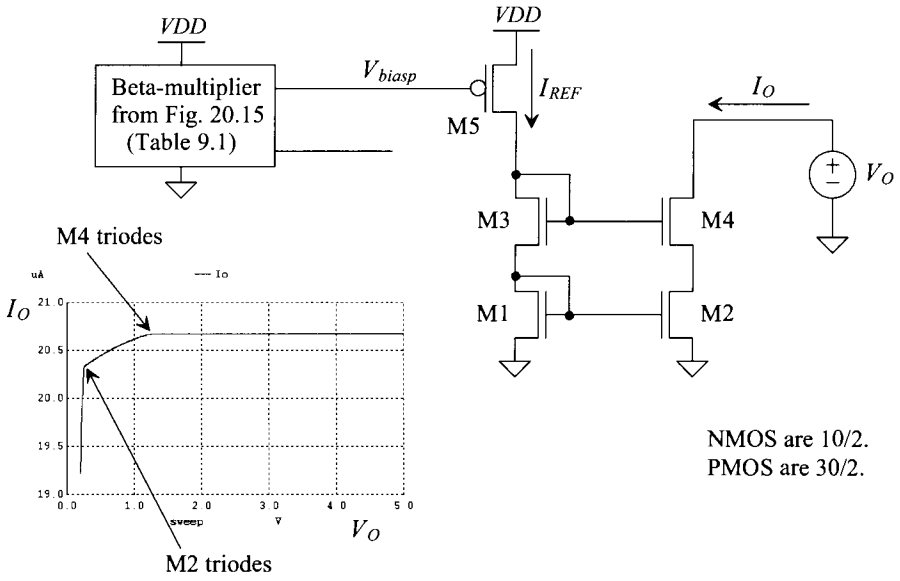


Figure 20.29 Biasing of the cascode current source and its operation.

DC Operation

The voltage on the gate of M4 in Fig. 20.29 is (remembering the actual values for these specific biasing conditions is given in Table 9.1)

$$2V_{GS} = 2(V_{DS,sat} + V_{THN}) \tag{20.47}$$

The voltage on the drain of M2, assuming that it is operating in the saturation region, is V_{GS}. The minimum voltage across the current source is then

$$V_{O,\min} = V_{DS,sat4} + V_{GS} = 2V_{DS,sat} + V_{THN} \tag{20.48}$$

Plugging in the numbers from Table 9.1, we get $V_{O,\min} = 1.3\ V$. Reviewing Fig. 20.29, we see that M4 starts to move into the triode region at this voltage.

To keep both M2 and M4 operating in the saturation region, we need only a $V_{DS,sat}$ across each one. In the next section we'll use this fact to design a *low-voltage cascode* current mirror.

Cascode Output Resistance

To estimate the output resistance of the cascode current mirror, let's apply a test voltage to the simplified cascode schematic seen in Fig. 20.30. We treat M1 and M3 as DC bias sources (AC grounds) and assume that the DC voltage on the drain of M4 is large enough to ensure that M2 and M4 are operating in the saturation. Further we draw the output resistances external to the devices. Note that M2's AC gate source voltage is zero and its drain voltage is $-v_{gs4}$. The resistance seen looking into the drain of M4 is

$$. R_o = \frac{v_T}{i_T} \tag{20.49}$$

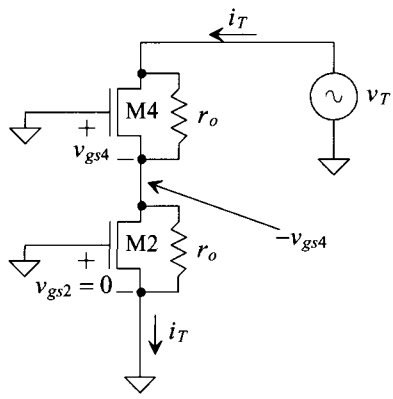


Figure 20.30 AC circuit used to determine the output resistance of a cascode current source.

Looking at Fig. 20.30, we can write

$$-v_{gs4} = i_T \cdot r_o \tag{20.50}$$

The current through M4 is then

$$i_T = g_m v_{gs4} + \frac{v_T - (-v_{gs4})}{r_o} \tag{20.51}$$

Substituting (20.50) into (20.51) gives

$$i_T = g_m(-i_T \cdot r_o) + \frac{v_T}{r_o} - i_T \tag{20.52}$$

Solving for the output resistance

$$R_o = (2 + g_m r_o) r_o \approx g_m r_o^2 \tag{20.53}$$

This result should be remembered because it will be referred to often. Using the numbers from Tables 9.1 and 9.2, we can tabulate the output resistance of cascode structures as seen in Table 20.1.

Table 20.1 Output resistances for cascode structures.

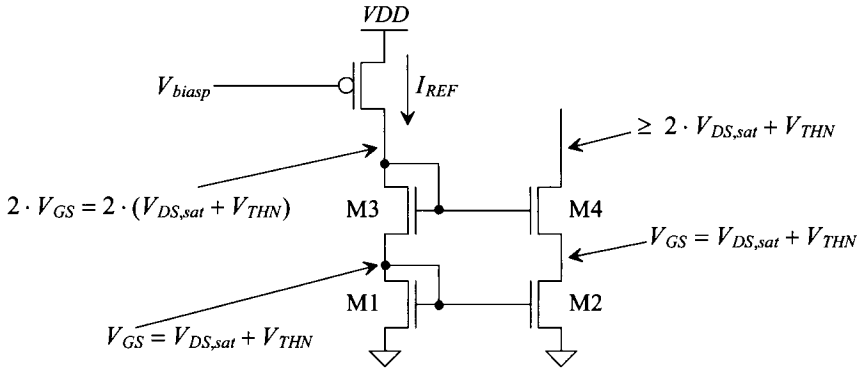
Cascode type	Long-channel process, Table 9.1, R_o	Short-channel process, Table 9.2, R_o
PMOS	2.4 GΩ	16.6 MΩ
NMOS	3.75 GΩ	4.2 MΩ

Notice the large difference (almost three orders of magnitude) between the output resistance of the short- and the long-channel devices. Again, this is the reason we need to use special circuit techniques when designing in short-channel processes.

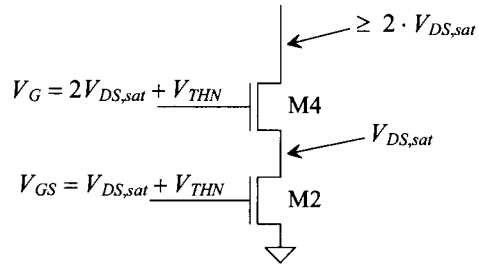
Finally, note that the output resistance can be determined from a plot like the one seen in Fig. 20.29 (or Fig. 20.28) by plotting the reciprocal of the derivative of the output current.

20.2.2 Low-Voltage (Wide-Swing) Cascode

Figure 20.31a shows the regularly biased cascode structure. The key point of this figure is that the drain of M2 is not at the minimum voltage required to keep it in saturation, $V_{DS,sat}$, but rather it is held at a threshold voltage above this minimum. In (b) the cascode is biased for lowest voltage operation. What this means is that the drain of M4, V_o, can go to the minimum possible voltage that keeps M2/M4 in saturation, that is, $2V_{DS,sat}$. Again, it's important to notice that the gate-source voltages of M1/M2 are what set the currents in the mirror.



(a) Regular cascode structure



(b) Low-voltage (aka wide-swing) structure

Figure 20.31 DC voltages in (a) a cascode current mirror and in (b) a low-voltage cascode.

To generate the gate voltage of M2, we simply use a diode-connected MOSFET as seen in almost every schematic in this chapter. From Eq. (20.1), for example, we can write

$$I_{REF} = \frac{KP_n}{2} \cdot \frac{W}{L}(V_{GS} - V_{THN})^2 \qquad (20.54)$$

neglecting channel-length modulation. To generate the bias voltage for M4, we can adjust the width and length of a MOSFET, MWS, as seen in Fig. 20.32. We can write, knowing $V_{DS,sat} = V_{GS} - V_{THN}$

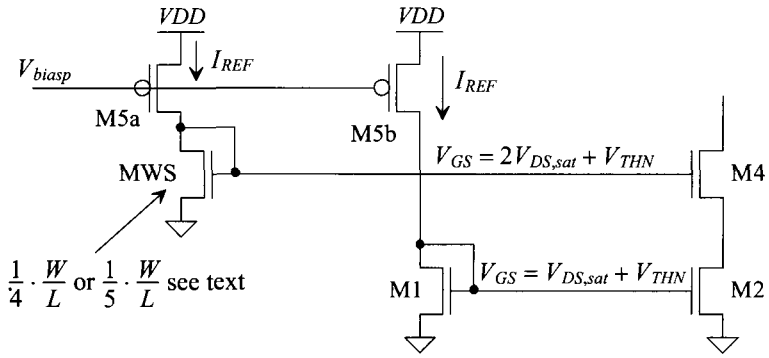


Figure 20.32 Generating a bias voltage for M4.

$$I_{REF} = \frac{KP_n}{2} \cdot \frac{W_{MWS}}{L_{MWS}} (2(V_{GS} - V_{THN}) + V_{THN} - V_{THN})^2 \qquad (20.55)$$

or

$$I_{REF} = \frac{KP_n}{2} \cdot \frac{W_{MWS}}{L_{MWS}} \cdot 4(V_{GS} - V_{THN})^2 \qquad (20.56)$$

Using our device sizes from either Tables 9.1 or 9.2, we can make the length of MWS four times the length of the other MOSFETs or

$$\frac{W}{L} = \frac{W_{MWS}}{L_{MWS}} \cdot 4 \qquad (20.57)$$

If we use the same widths, then

$$L_{MWS} = 4 \cdot L \qquad (20.58)$$

If Eq. (20.58) is valid, then Eq. (20.56) is equal to Eq. (20.54).

Note that, as seen in Fig. 20.31b, we are biasing M2 right on the edge of the triode region when we use Eq. (20.58) to size MWS. In many situations we may want to move M2 further into the saturation region. Intuitively, we would think that by increasing the length of MWS we increase its effective resistance and so the voltage drop across it goes up. If we increase MWS's length further, the gate voltage of M4 goes up and thus so does the drain voltage of M2. M2 is moved further away from the edge of the triode region into the saturation region. The minimum voltage across the current source increases. It's important to understand that it's OK for M2 to be biased away from the triode region by a small amount.

Example 20.7

Regenerate Fig. 20.29 using a wide-swing cascode structure.

The simulation results are seen in Fig. 20.33. It appears that the output resistance is really large until $V_O < V_{DS,sat}$. However, if we zoom in around $2V_{DS,sat}$ (= 500 mV here), we would see that the slope increases and M4 triodes. ■

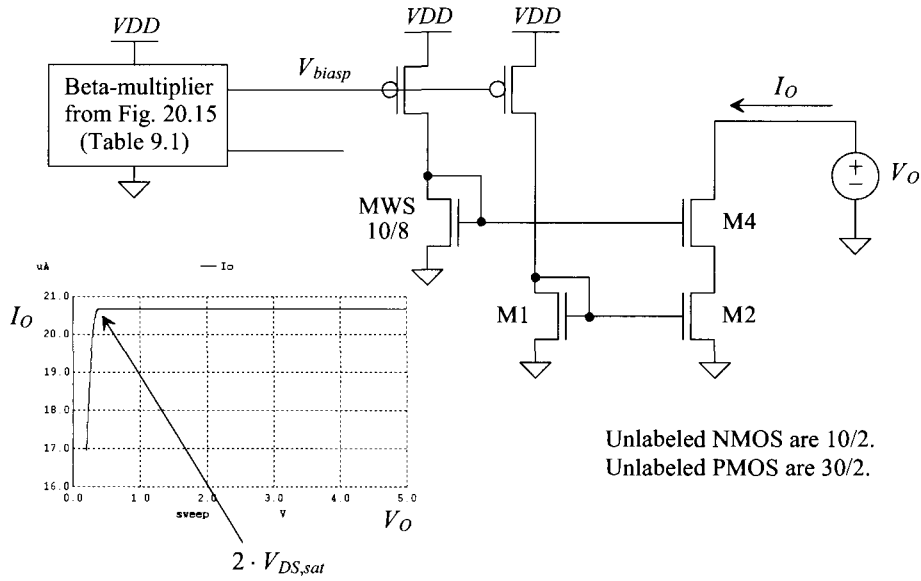


Figure 20.33 Wide-swing cascode current source in the long-channel process.

An Important Practical Note

In general we won't design a wide-swing current sink by setting the length to four times the length used in the rest of the design. As just mentioned, this biases M2 right on the edge of the triode region (point A) in Fig. 20.34. Stealing a current from the drain of M2 will move M2 into the triode region, point B. If we bias M2 further into the saturation region, point C, then more current must be removed before M2 triodes and the output resistance of the current source decreases. When we design folded-cascode amplifiers later, we will steal or add current in this way. For general *long-channel design,* we'll use

$$\frac{W_{MWS}}{L_{MWS}} = \frac{1}{5} \cdot \frac{W}{L} \tag{20.59}$$

or using the same widths then

$$L_{MWS} = 5 \cdot L \tag{20.60}$$

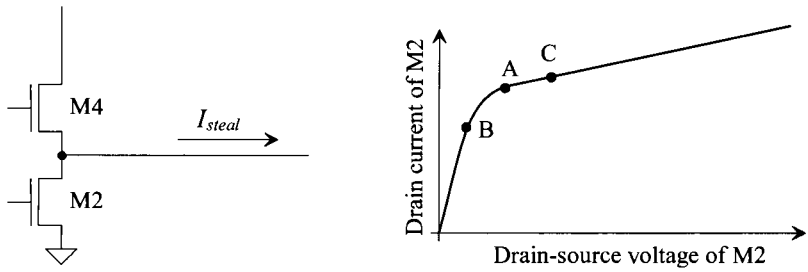


Figure 20.34 Showing how stealing current from M2 moves it into the triode region.

Layout Concerns

When we go to layout the long L device seen in Fig. 20.32, we might simply layout a single MOSFET with the appropriate length. However, the threshold voltage can vary significantly with the length of the device. Figure 20.35 shows a method where MOSFETs connected in series with the same widths and their gates tied together behave like a single MOSFET with the sum of the individual MOSFET's lengths. Because each device is identical, changes in the threshold voltage shouldn't affect the biasing circuit.

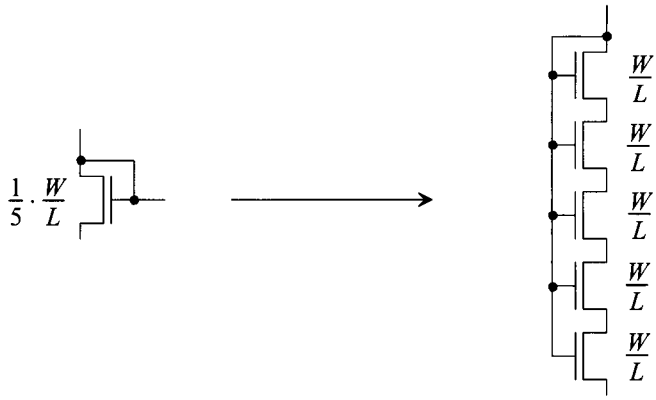


Figure 20.35 Using equal length devices to implement a long L MOSFET.

20.2.3 Wide-Swing, Short-Channel Design

When designing a wide-swing current mirror in a short-channel CMOS process, we know

$$V_{DS,sat} \neq V_{GS} - V_{THN} = V_{ovn} \tag{20.61}$$

Further, as seen in Fig. 9.32 in Ch. 9, the output resistance of a short-channel MOSFET depends on the drain-to-source voltage. Figure 20.36 shows a wide-swing current mirror designed in the short-channel CMOS process (see Table 9.2). Note that the current is approximately 4 μA when it should be, as seen in Fig. 20.23, 10 μA. Further, if we were to measure the output resistance, we would get approximately 600k, which is considerably less than the 4 MΩ seen in Table 20.1. As seen in Fig. 9.32, the output resistance at $V_{DS,sat}$ isn't 166k as indicated in Table 9.2 but much less. To increase the output resistance, let's attempt to bias M2 deeper into the saturation region. Let's do this by using a larger value of voltage on the gate of M4. For our short-channel design, let's try

$$\frac{W_{MWS}}{L_{MWS}} = \frac{1}{25} \cdot \frac{W}{L} \tag{20.62}$$

or a five times smaller ratio than what we used for the long-channel devices (Eq. [20.59]). The simulation results for the circuit in Fig. 20.36 are seen in Fig. 20.37 when MWS is sized 10/10. Notice that our output current is closer to 10 μA. Studying Fig. 20.36 and remembering our constant theme in this chapter that good matching requires both equal V_{GS} and V_{DS}, we see a concern. M1's drain-to-source voltage isn't the same as M2's. By

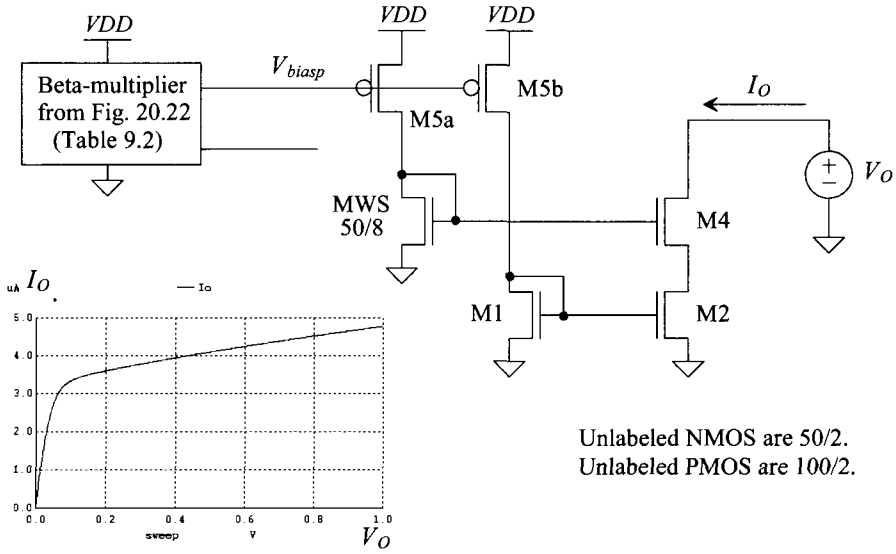
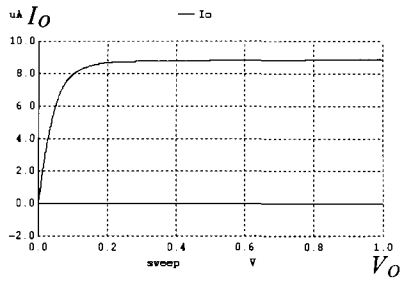


Figure 20.36 Wide-swing cascode current source in the short-channel process (bad).

making the gate voltage of M4 larger, we act to equalize the two drain-to-source voltages (we increase the drain voltage of M2) causing the output current to approach the current that flows in M1 (10 μA). Let's attempt to make the current mirrors more symmetrical in an effort to equilibrate the drain-to-source voltages of M1 and M2.

Figure 20.38 shows the addition of a MOSFET, M3, to lower M1's V_{DS} so that it matches M2's V_{DS}. The 10 μA current through M5b can now be mirrored accurately. M1's gate voltage increases until M1 (and thus M2) can sink the current supplied by M5b with the smaller V_{DS}. *For all wide-swing current mirrors the topology seen in Fig.* 20.38 *using M3 should be used.* Note also, in Fig. 20.38, the larger voltage needed across the current source to keep M2/M4 saturated. The drains of M1 and M2 are at 150 mV or considerably above $V_{DS,sat}$ (which is 50 mV from Fig. 9.32). M3 is moving close to the triode region. Equation (20.62) can be modified to move M3 away from triode by using a larger W/L device (say 1/10); however, the output resistance will decrease (again as seen in Fig. 9.32, the decrease in V_{DS} results in smaller output resistance, r_o).



MWS is 10/10 in Fig. 20.36.

Figure 20.37 Increasing the W/L of MWS to 1/25 the other W/Ls.

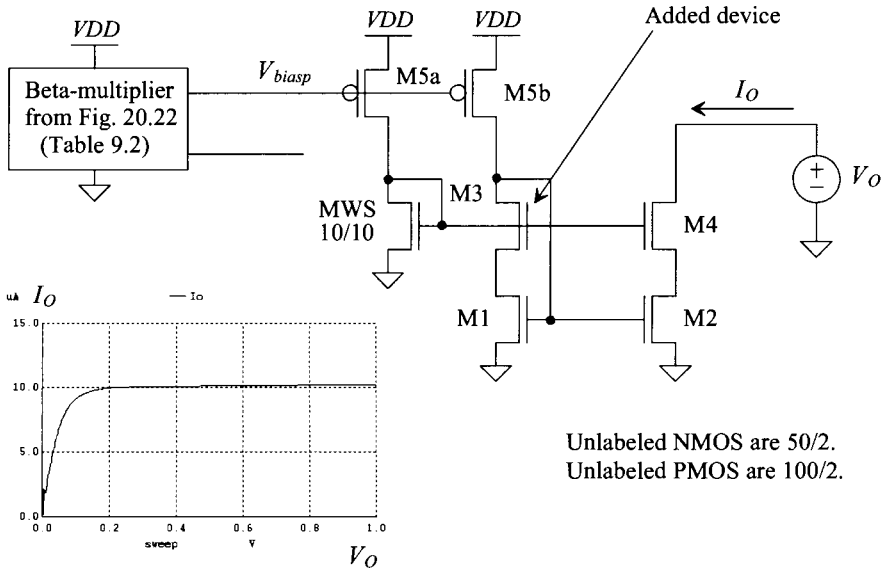


Figure 20.38 Wide-swing cascode current source in the short-channel process (good). Notice the drain-to-source voltages of M1 and M2 are the same.

Example 20.8

Regenerate the plot seen in Fig. 20.38 if MWS is sized using

$$\frac{W_{MWS}}{L_{MWS}} = \frac{1}{10} \cdot \frac{W}{L} \tag{20.63}$$

The simulation results are seen in Fig. 20.39 where MWS is sized 10/4. The output resistance is roughly four times smaller than what we got in Fig. 20.38 using Eq. (20.62). M3 is biased further away from the triode region. The point here is that there isn't any single equation that governs the selection of MWS size for all processes. Design trade-offs must be made.

Note that an interesting simulation to run at this point is to verify that the current mirror still functions correctly with small *VDD* (as seen in Fig. 20.23 with *VDD* down to 0.5 V). The output voltage, V_O, can still go to 1 V. ■

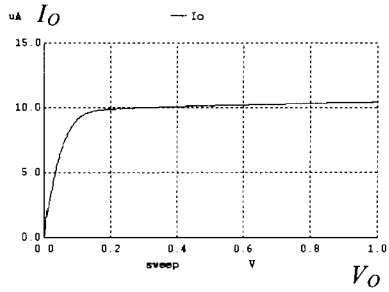


Figure 20.39 Resimulating the circuit in Fig. 20.39 using a 10/4 device for MWS.

20.2.4 Regulated Drain Current Mirror

Consider adding an amplifier to the basic wide-swing current mirror as seen in Fig. 20.40. The purpose of the amplifier is to regulate or hold the drain of M2 at a fixed potential (in this case, the drain potential of M1). If we can hold the drain potential of M2 perfectly fixed, then M2's drain current won't vary and the output resistance of the current mirror will be infinite. In the next section, we'll discuss general biasing circuits. We'll use the drain voltage of M1 as a bias voltage simply for regulating the drain in current mirrors.

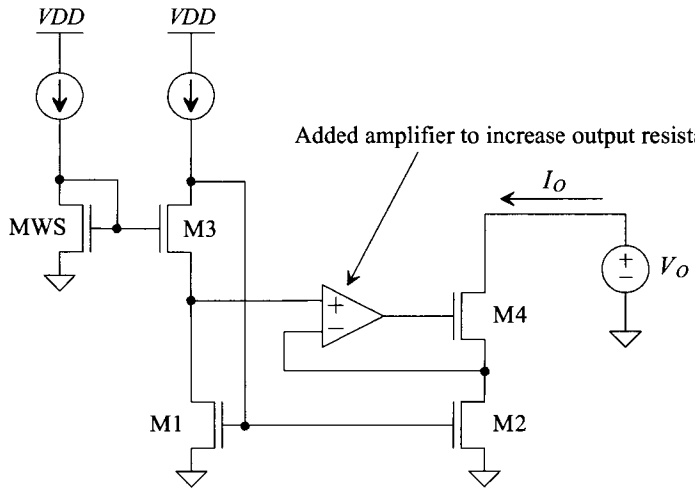


Figure 20.40 Regulating the drain of M2 using an amplifier.

We can estimate the enhancement in the output resistance of the current mirror by assuming the output of the added amplifier is related to its inputs using

$$v_{out} = A \cdot (v_+ - v_-) \tag{20.64}$$

where A is the gain of the added amplifier. Using Fig. 20.41, we can write, knowing the drain and gate of M1 are DC bias voltages (AC grounds),

$$v_{gs4} = -i_T r_o (A + 1) \tag{20.65}$$

and

$$i_T = g_m(-i_T r_o(A+1)) + \frac{v_T - i_T r_o}{r_o} \tag{20.66}$$

and finally,

$$R_o = \frac{v_T}{i_T} = 2r_o + g_m r_o^2 (A+1) \approx g_m r_o^2 \cdot A \tag{20.67}$$

When compared to Eq. (20.53), the output resistance is increased by the gain of the added amplifier. This result can be very useful (and we will use it often) in practical circuit design.

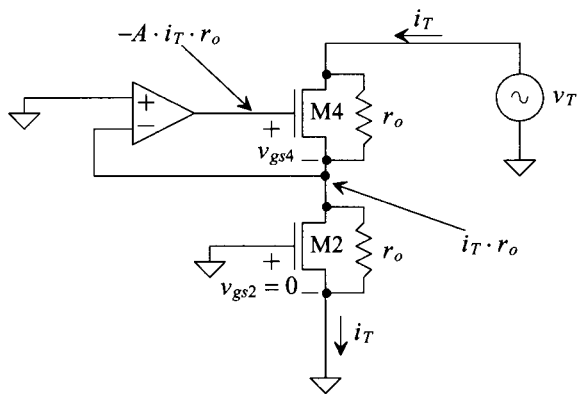


Figure 20.41 Determining the output impedance of a regulated drain current mirror.

A practical example of a current mirror that uses this technique is seen in Fig. 20.42. The drains of M1 and M2 are held at a V_{GS} by MA1 and MA2. If the drain potential of M2, for example, starts to decrease, MA2 starts shutting off, causing the gate voltage of M4 to increase, and pulling the drain potential of M2 back up. MA1 and MA2 are used to ensure that the circuit is symmetrical (M1 and M2 have the same V_{DS}). The drawback of this topology, as seen in the simulation results in the figure, is that the minimum voltage across the current mirror is $V_{DS,sat} + V_{GS}$ (just like the basic cascode, see Eq. [20.48]). The gain of the added amplifier (A) is, as we'll see in the next chapter, $g_m r_o/2$. We can estimate the output resistance as $g_m^2 r_o^3/2$ or 52 MΩ. Note that M3 is operating in the triode region.

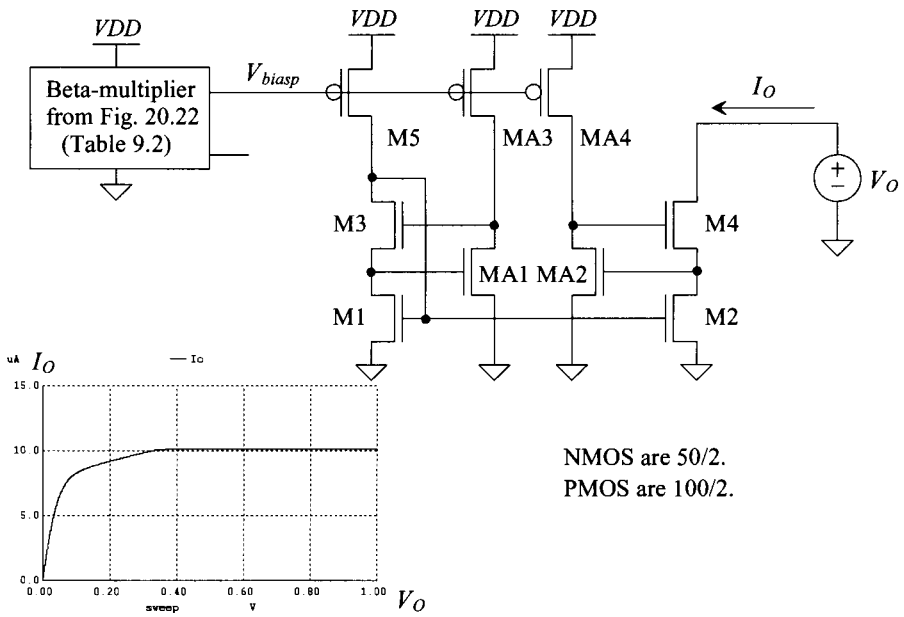


Figure 20.42 Using amplifiers to regulate the drain potentials in a current mirror.

20.3 Biasing Circuits

In this section we provide biasing circuit examples for the chapters that follow based on the data in Tables 9.1 and 9.2.

20.3.1 Long-Channel Biasing Circuits

Figure 20.43 shows a general biasing circuit for the long-channel CMOS process based on the sizes and currents given in Table 9.1. The Beta-multiplier, self-referenced circuit from Fig. 20.15 is used for biasing wide-swing current mirrors (V_{bias1} to V_{bias4}). V_{high} and V_{low} will be used later with amplifiers for regulating the drain of a MOSFET, as seen in Fig. 20.40. V_{ncas} and V_{pcas} are used for a circuit called a "floating current source" (which is discussed later). Perhaps the best way to see how this circuit can be used is to give a couple of examples.

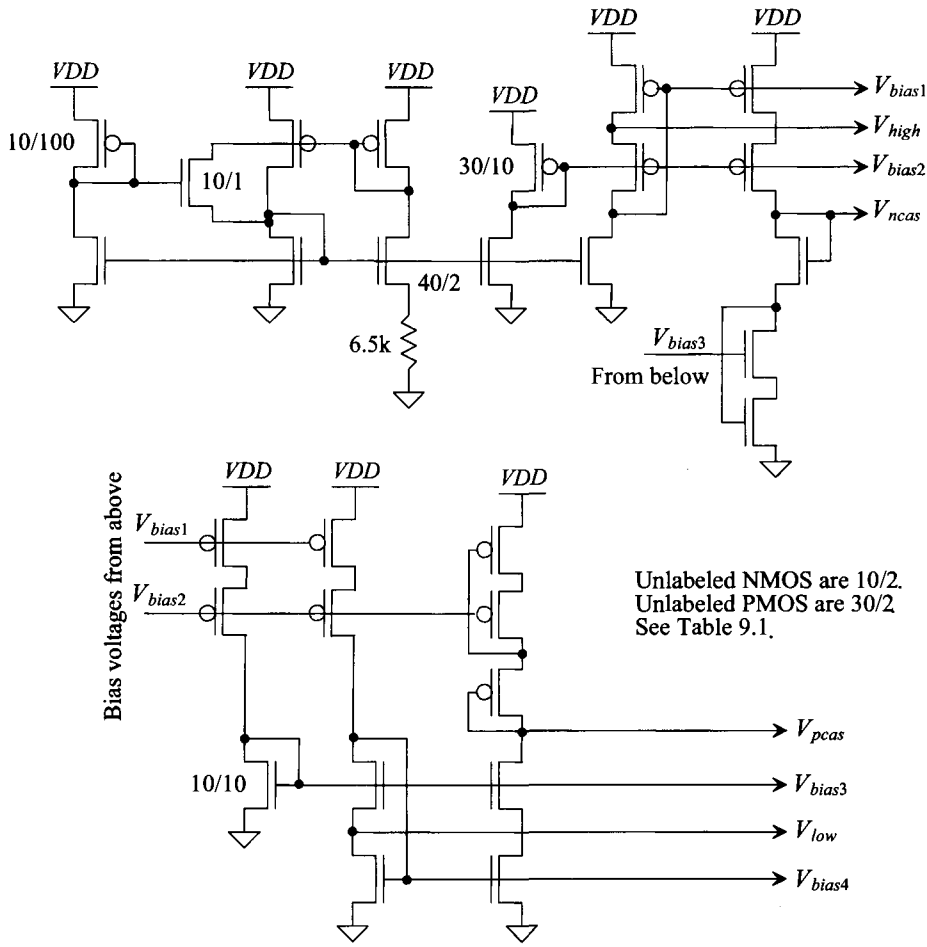
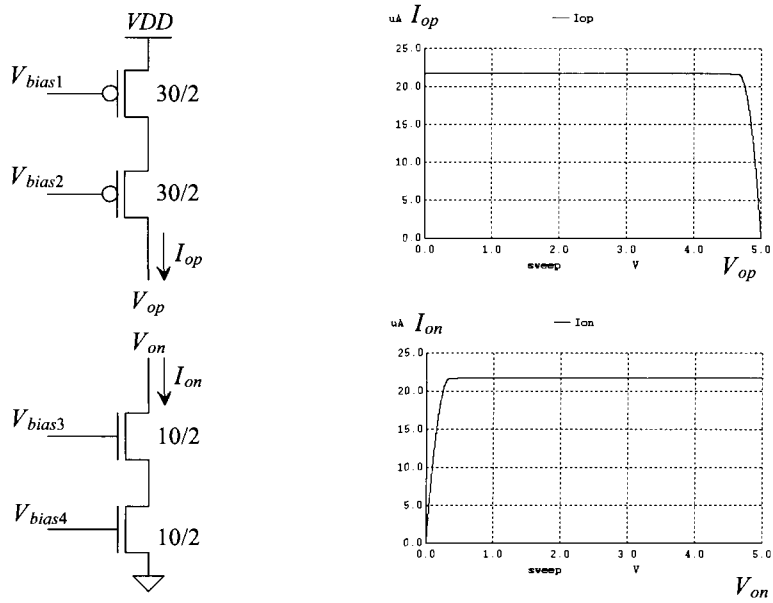


Figure 20.43 General biasing circuit for long-channel CMOS design using the data in Table 9.1

Basic Cascode Biasing

Figure 20.44 shows how the bias voltages generated in Fig. 20.43 can be used to bias both PMOS and NMOS cascode current sources. As indicated in Table 9.1 and Fig. 20.31b, the minimum voltage across the current sources is $2V_{DS,sat}$ or 500 mV. The current that flows in the current sources is nominally 20 μA.



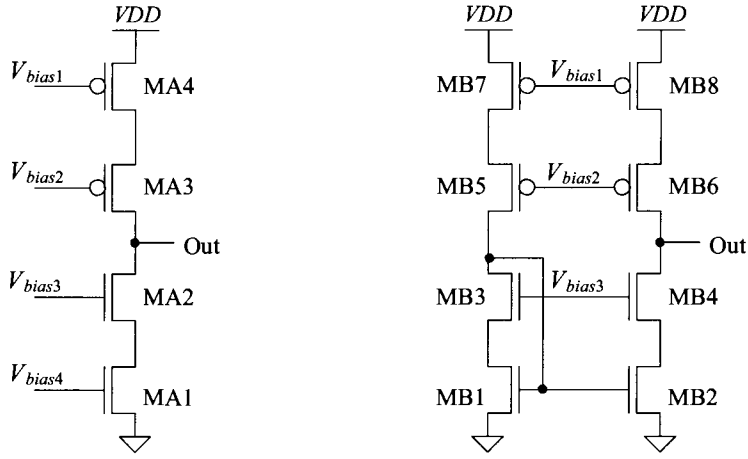
Bias voltages come from Fig. 20.43 (long-channel parameters in Table 9.1).

Figure 20.44 How cascode currents are biased and how they operate.

The Folded-Cascode Structure

Figure 20.45a shows a structure where an NMOS current source is connected to a PMOS current source. In this topology there is no way we can guarantee that the current flowing in the PMOS transistors is precisely equal to the current flowing in the NMOS transistors. This will cause the output of the circuit to move towards either *VDD* or ground (depending on which cascode structure is sourcing the most current). In (b) we fold the cascode structure over and diode-connect the folded NMOS devices (we could, just as well, have diode-connected the PMOS devices instead). Now, the gate potentials of MB1 and MB2 are set by the current that is sourced from MB5 and MB7. If the transistors are perfectly matched, the output voltage will equal the gate voltage of MB1 (the drain voltage of MB3) because of the circuit's symmetry. (We also saw this in Fig. 20.1.)

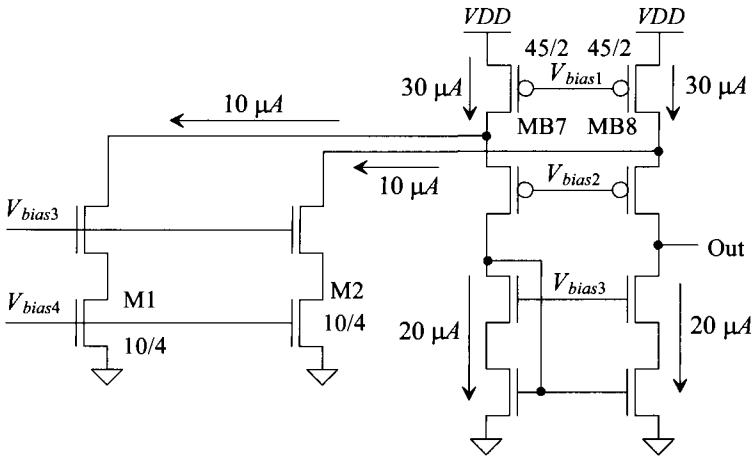
In Figure 20.46 we add some MOSFETs to steal 10 μA from MB7 and MB8. To make sure that the currents are equal, we size up MB7 and MB8 so that they source 30 μA. Note how we doubled the length of M1 and M2 so that they sink 10 μA from the same bias voltages.



(a) (b) Folded cascode structure

Bias voltages come from Fig. 20.43 (long-channel parameters in Table 9.1). All NMOS are 10/2, while all PMOS are 30/2.

Figure 20.45 Using a folded cascode structure to make sure that the current sourced by the PMOS equals the current sourced by the NMOS.



Bias voltages come from Fig. 20.43 (long-channel parameters in Table 9.1). All unlabeled NMOS are 10/2, while all unlabeled PMOS are 30/2.

Figure 20.46 Stealing current from the folded cascode structure.

20.3.2 Short-Channel Biasing Circuits

Figure 20.47 shows a biasing circuit for a general analog design short-channel process. It uses the Beta-multiplier, self-referenced bias circuit from Fig. 20.22. As indicated in Sec. 20.1.4, the critical capacitance for stability is MCP. Notice that we are using the PMOS devices in the Beta-multiplier to bias the current mirrors, whereas in Fig. 20.43 we used the NMOS devices. We picked the PMOS here simply to increase the capacitance on V_{biasp} and so to further stabilize the circuit. Figure 20.48 shows the operation of the cascode current mirrors biased with the circuit in Fig. 20.47. It's important to realize that the minimum voltage across the current source is considerably above $2V_{DS,sat}$. Again, this was a design choice (see Eqs. [20.62] and [20.63]) to increase output resistance.

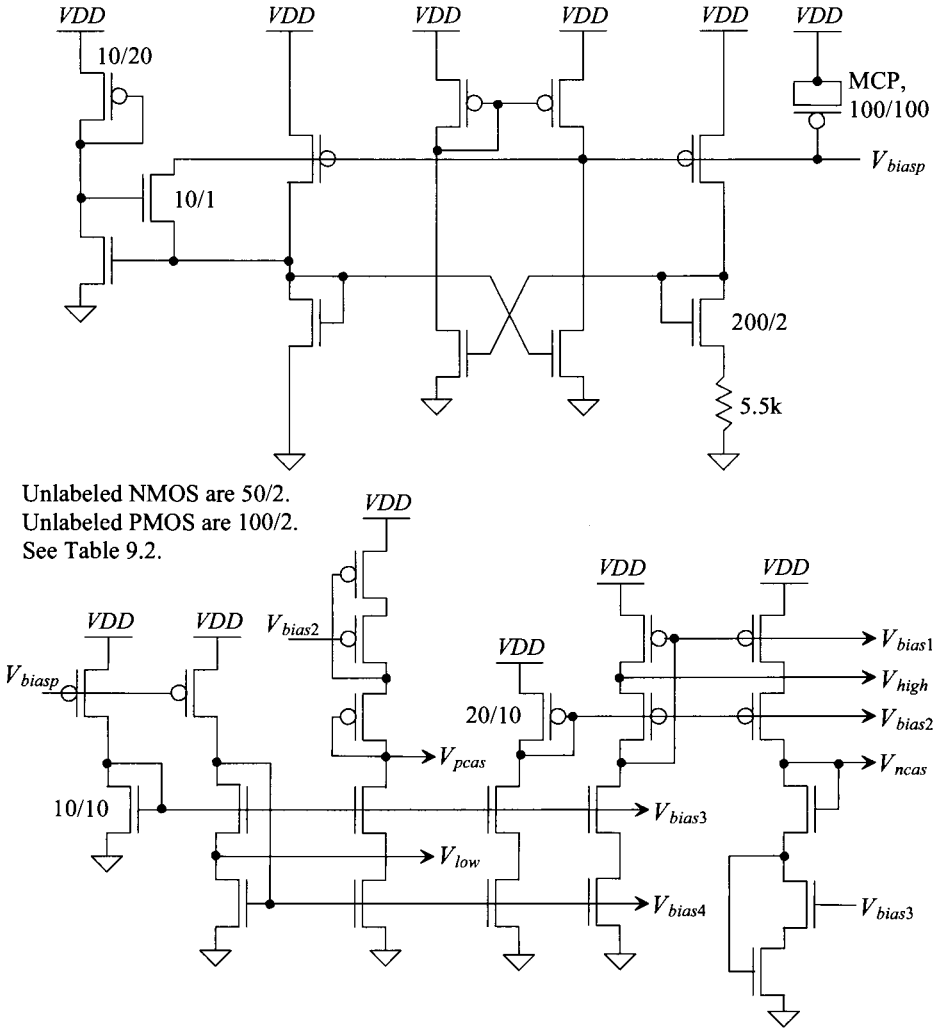
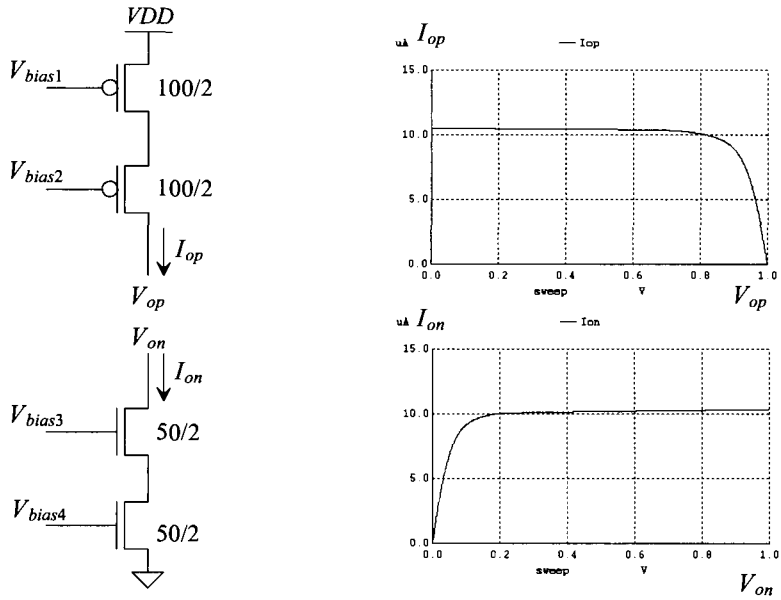


Figure 20.47 General biasing circuit for short-channel design using the data in Table 9.2.



Bias voltages come from Fig. 20.47 (short-channel parameters in Table 9.2).

Figure 20.48 Cascode current sources operating in a short-channel process.

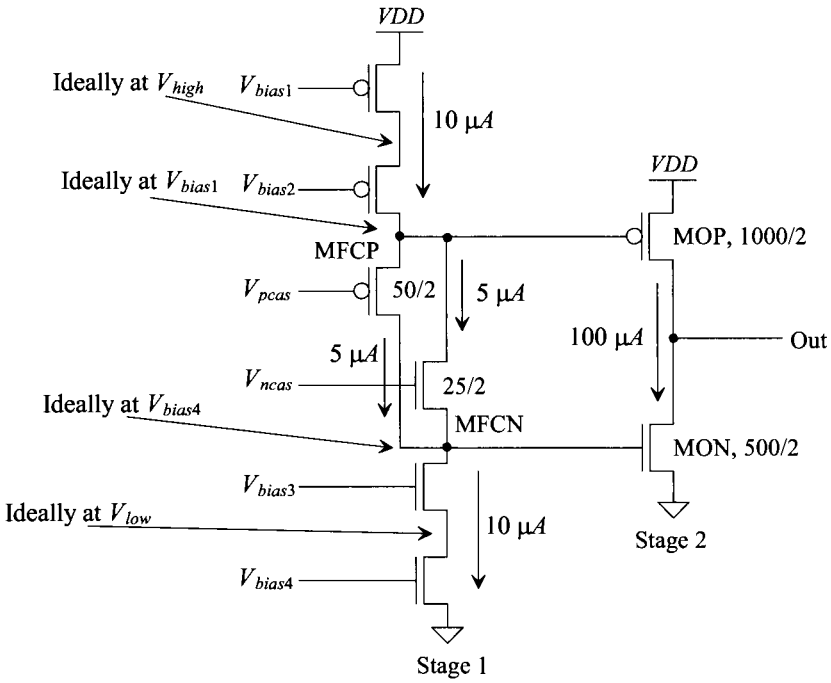
Floating Current Sources

In Fig. 20.49 we add two MOSFETs, MFCP and MFCN, to the cascode structure to form a *floating current source*. The addition of MFCN, for example, allows the voltage across the PMOS cascode structure to become V_{bias1} (assuming that matching between the bias circuit and this circuit is perfect). The voltage across the NMOS cascode becomes V_{bias4}. This can be very useful for biasing the next stage in an amplifier. For example, if we connect an NMOS (MON in the figure) device to the source of MFCN, then, because this potential is ideally V_{bias4}, we treat the MOSFET as if it were biased with V_{bias4}. Since the width of MON in the figure is ten times the widths of the other NMOS, the current in the output stage will be 100 μA. Figure 20.50 shows the simulation results with currents that flow in stage 1 and stage 2 of the circuit.

Note that the circuit in Fig. 20.49 uses all of the bias voltages except for V_{low} and V_{high}. These voltages are used with circuits that employ drain regulation, as discussed in Sec. 20.2.4.

20.3.3 A Final Comment

The bias circuits in Figs. 20.43 and 20.47 will be used in the next several chapters to provide biasing for amplifier design examples. It's important to remember our constant theme when we design current mirrors, that is, if we can set both the gate-source and the drain-source voltages of a MOSFET, we set the drain current. Similarly if we can set the drain current and gate-source voltage, then we set the drain-source voltage.



Bias voltages come from Fig. 20.47 (short-channel parameters in Table 9.2). Unlabeled NMOS are 50/2, while unlabeled PMOS are 100/2.

Figure 20.49 Biasing with a floating current source.

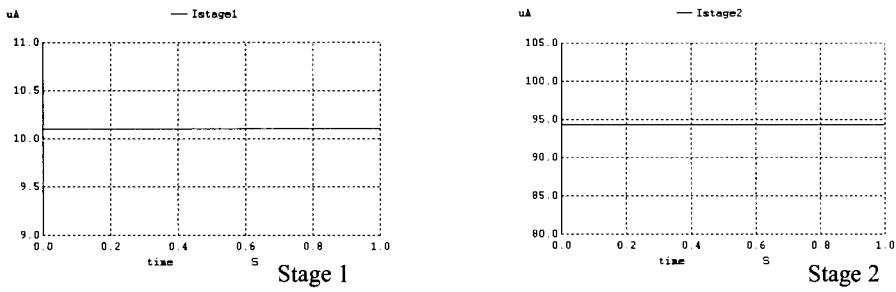


Figure 20.50 The simulated currents that flow in stages 1 and 2 of the circuit in Fig. 20.49.

ADDITIONAL READING

[1] S. J. Lovett, M. Welten, A. Mathewson, and B. Mason, "Optimizing MOS transistor mismatch," *IEEE Journal of Solid-State Circuits,* vol. 33, pp. 147–150, January 1998.

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PROBLEMS

20.1 Using the CMOS long-channel process (1 μm), determine the current flowing in the circuit seen in Fig. 20.51. Verify your answer with SPICE.

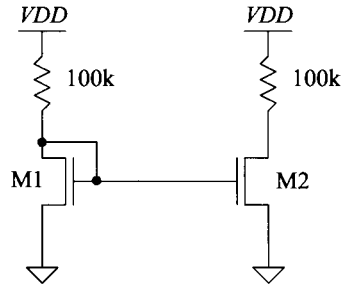

Figure 20.51 Current mirror used in Problem 20.1.

20.2 Repeat problem 20.1 for the circuit in Fig. 20.52. Can M1 and M2 be replaced with a single MOSFET? If so how and what size? If not why?

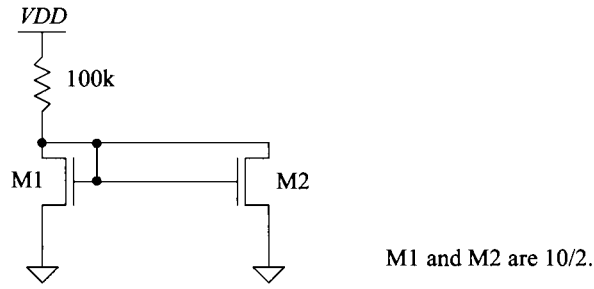

Figure 20.52 Circuit used in Problem 20.2.

20.3 Show the SPICE simulations for the PMOS devices in Ex. 20.1.

20.4 A threshold voltage mismatch in SPICE can be modeled by adding a small voltage source in series with the gate of one of the MOSFETs, as seen in Fig. 20.53. Show, using SPICE, that Eq. (20.8) is valid.

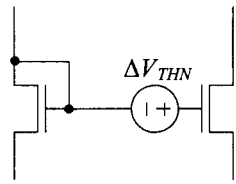

Figure 20.53 Modeling an offset voltage in SPICE (or for hand calculations).

20.5 Show, using simulations and hand-calculations, that by using a larger value of $V_{DS,sat}$ when designing bias circuits, the MOSFETs enter the triode region earlier.

20.6 In Ex. 20.2, how does the gate voltage of M1/M2 change as *VDD* is decreased? How does the V_{SG} change? Use SPICE to verify your answers.

20.7 For the same bias current used in Table 9.1 (nominally 20 μA), regenerate Fig. 20.13 if minimum-length MOSFETs are used in the current mirror. Show the hand calculations leading to the selection of the MOSFET sizes.

20.8 Suppose that the bias circuit used to generate Fig. 20.16 shows a reference current change with *VDD,* as seen in Fig. 20.54. Knowing that the reference current should be constant with changes in *VDD,* what is wrong with the reference? (What important portion of the reference is causing the problem?)

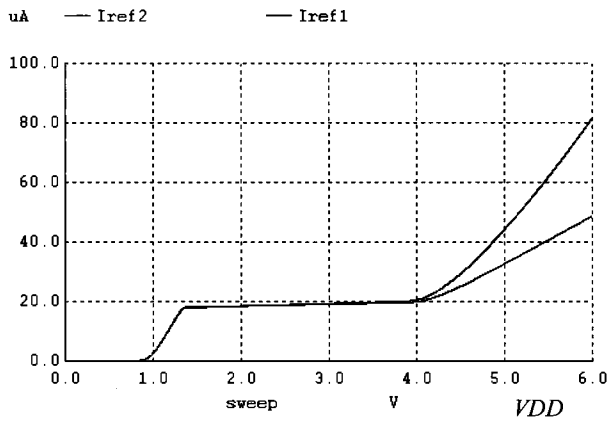

Figure 20.54 Problems with reference current increasing with VDD.

20.9 Using hand calculations, estimate the value of the voltage across *R* for the current reference in Fig. 20.15.

20.10 Using SPICE, determine if the reference circuit seen in Fig. 20.22 can become unstable with changes in *VDD*. Show that reducing the size of MCP and MCN affects the stability of the circuit.

20.11 Estimate the temperature behavior of the gate voltage of M1 in Fig. 20.10.

20.12 Design a voltage reference using the Beta-multiplier in the short-channel process and the data from Table 9.2. Generate a figure similar to Fig. 20.27 to show the temperature performance of your design.

20.13 *K* can be used to minimize *R* in Eq. (20.46) for a fixed-reference current. If M1/M2 experience a threshold voltage mismatch (see problem 20.4), discuss and show with simulations how much ΔV_{THN} can be tolerated and the error in the reference current that results.

20.14 Using an AC test voltage, determine the output resistance of the MOSFET current mirror seen in Fig. 20.28.

20.15 Based on the data in Table 9.1, what are the voltages on the drain, gate, and source terminals of M1–M4 in Fig. 20.29, assuming that the devices are operating in the saturation region? Compare your hand calculations to simulations.

20.16 If the MOSFET in Fig. 20.55 is operating in the saturation region, determine the small-signal resistance looking into its drain.

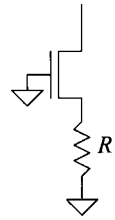

Figure 20.55 Resistance looking into the drain of a MOSFET with a source resistance. See Problem 20.16.

20.17 Suppose that the wide-swing current mirror seen in Fig. 20.38 is implemented in the long-channel CMOS process (Table 9.1). Estimate the size of MWS when M3 triodes. Verify your answer with simulations.

20.18 Label the voltages, based on the values in Table 9.1, in the schematic of the general biasing circuits seen in Fig. 20.43. Compare the tabulated values of V_{GS}, V_{DS}, etc., to the simulated values.

20.19 How would the current in Fig. 20.44 change if the width of the device connected to V_{bias2} were doubled? Were halved? Why? Explain what is going on in the circuit.

20.20 Should the voltage labeled "Out" in Fig. 20.49 be at a specific value? Why or why not?