Chapter
21

Amplifiers

In this chapter we turn our attention towards amplifiers. Single-stage amplifiers are used in virtually every op-amp design. By replacing a passive load resistor with a MOSFET transistor (called an *active load*), significant amounts of chip area can be saved. An active load can also produce higher values of resistance when compared with a passive resistor, resulting in higher gains.

Several types of active loads are studied in this chapter. The *gate-drain load* consists of a MOSFET with the gate and drain shorted and provides large bandwidths and low-output impedance at the cost of reduced gain. The *current source load* amplifier has a higher gain and output impedance at the expense of lower bandwidth. Current source load amplifiers are preferred when external feedback is applied to the amplifier to set the gain. This chapter explores basic single-stage amplifiers with active loads, as well as the trade-offs associated with each. The cascode amplifier is examined in detail along with several configurations of output stages, including the push-pull amplifier.

21.1 Gate-Drain-Connected Loads

A gate-drain-connected MOSFET (load) is half of a current mirror as seen in Fig. 20.1 in the last chapter. Here we move the discussion from the DC operating conditions and biasing presented in the last chapter to AC small-signal analysis.

21.1.1 Common-Source (CS) Amplifiers

A gate-drain-connected MOSFET (operating with a nonzero drain current) can be thought of as a resistor of value $1/g_m$ (see Fig. 9.18 and Eq. [9.25]). The four possible common-source (CS) amplifiers using gate-drain-connected loads are seen in Fig. 21.1. In each configuration, M1 and M2 are assumed to be biased in the saturation region. Notice how the source of the amplifying MOSFET (i.e., not the load or gate-drain MOSFET) is common to both the input and the output in each configuration.

Examine the circuit shown in Fig. 21.1a. Since many MOSFET amplifiers are analyzed in this chapter and the next several chapters using small-signal analysis, an intuitive analysis approach will be used. This approach allows the designer to quickly analyze the gain of a circuit. To analyze the gain of the circuit in Fig. 21.1a, begin by

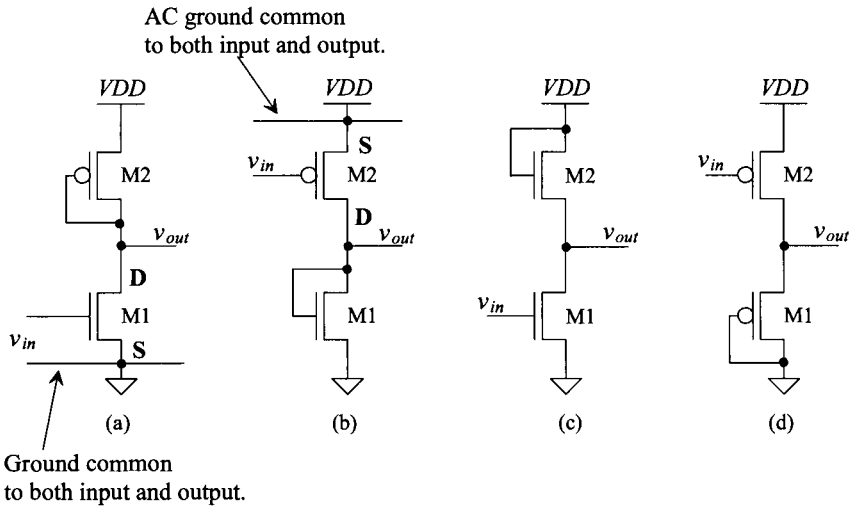


Figure 21.1 Four possible configurations of common-source amplifiers with gate-drain loads.

replacing M2 with a resistor of value $\frac{1}{g_{m2}}$ and replacing M1 with a current source of value $g_{m1} \cdot v_{in}$, provided $\frac{1}{g_{m2}} << r_{o1} || r_{o2}$. The equivalent circuit is shown in Fig. 21.2. Note that there is no body effect in either MOSFET and that only the low-frequency model is shown. Again, as seen in Ch. 9, a gate-drain-connected MOSFET has a small-signal resistance of value $\frac{1}{g_m}$. The small-signal gain of the **common-source amplifier** is given by

$$\frac{v_{out}}{v_{in}} = \frac{-i_d \cdot \frac{1}{g_{m2}}}{i_d \cdot \frac{1}{g_{m1}}} = -\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}} = -\frac{\text{resistance in the drain}}{\text{resistance in the source}} = -\frac{g_{m1}}{g_{m2}} \qquad (21.1)$$

This result is very important in the intuitive analysis. It states that the small-signal gain of a common-source amplifier is simply the resistance in the drain of M1 divided by the resistance in the source (the resistance looking into the source of M1 added to any resistance from the source of M1 to ground). The actual value of the resistance in the

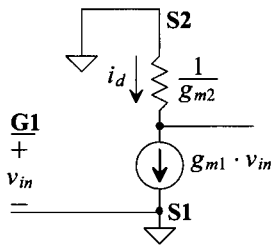


Figure 21.2 Simplified circuit of Fig. 21.1a.

drain, as will be soon seen, is $\frac{1}{g_{m2}} || r_{o1} || r_{o2}$. In most cases, however, r_o will be much greater than $\frac{1}{g_m}$, and the approximation is an accurate one.

Example 21.1

Determine the small-signal AC gain of the circuit shown in Fig. 21.3 using the intuitive method presented in Eq. (21.1).

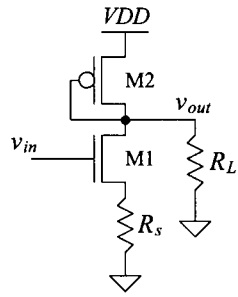


Figure 21.3 Amplifier analyzed in Ex. 21.1.

The small-signal gain of this circuit is given by

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{\text{resistance in the drain}}{\text{resistance in source}}$$

The resistance in the drain is the parallel combination of all resistances connected to the drain of M1, given by

$$\text{Resistance in the drain} = \frac{1}{g_{m2}} || R_L \text{ for } r_{o1} || r_{o2} >> \frac{1}{g_{m2}}$$

The resistance in the source is the sum of the resistance looking into the source of M1 ($1/g_{m1}$) and the resistance connected from the source of M1 to ground. For the present problem, this resistance is given by

$$R_{\text{in the source}} = \frac{1}{g_{m1}} + R_s$$

The voltage gain is then given by

$$A_v = -\frac{\frac{1}{g_{m2}} || R_L}{\frac{1}{g_{m1}} + R_s} \text{ which for } R_L \to \infty \text{ and } R_s \to 0 \text{ reduces to } -\frac{g_{m1}}{g_{m2}} \blacksquare$$

We can determine the exact gain of the amplifier of Fig. 21.1a using the full small-signal model shown in Fig. 21.4. Using KCL at the output of the amplifier gives

$$g_{m1} v_{in} + \frac{v_{out}}{r_{o2} || r_{o1}} = -g_{m2} v_{out} \tag{21.2}$$

or

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + \frac{1}{r_{o1} || r_{o2}}} = -\frac{\frac{1}{g_{m2}} || r_{o1} || r_{o2}}{\frac{1}{g_{m1}}} = -\frac{\text{resistance in the drain}}{\text{resistance in the source}} \tag{21.3}$$

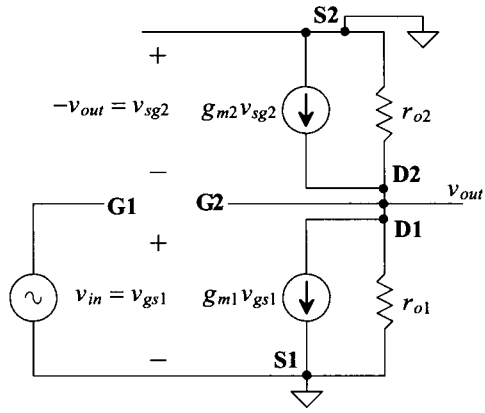


Figure 21.4 Small-signal model of the amplifier shown in Fig. 21.1(a).

When $\frac{1}{g_{m2}} << r_{o1} \| r_{o2}$, this reduces to

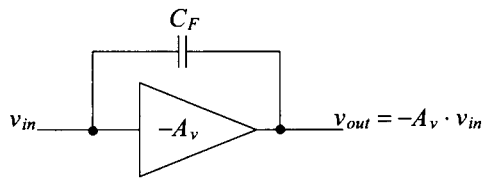
$$A_v = -\frac{\frac{1}{g_{m2}}}{\frac{1}{gm1}} = -\frac{g_{m1}}{g_{m2}} \tag{21.4}$$

which is the same form as Eq. (21.1).

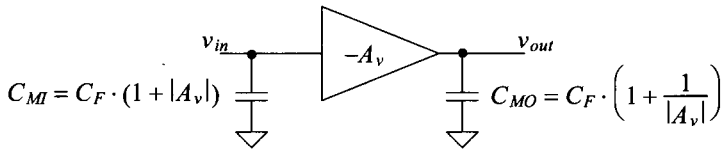
Miller's Theorem

Consider the inverting amplifier seen in Fig. 21.5a with a gain of $-A_v$ and a feedback capacitance between the output and the input of the amplifier. The current supplied by v_{in} or v_{out} to the capacitor is

$$i = \frac{v_{in} - v_{out}}{1/j\omega C_F} = j\omega C_F \cdot (1 + |A_v|) \cdot v_{in} = j\omega C_F \cdot \left(1 + \frac{1}{|A_v|}\right) \cdot v_{out} \tag{21.5}$$



(a)



(b)

Figure 21.5 The derivation of Miller's theorem.

In Fig. 21.5b we replace the feedback capacitor with capacitors on the input and the output of the amplifier to ground. These (adjusted size) capacitors require the same currents from the input source and the output of the amplifier. Note that this substitution, Eq. (21.5), is often called *Miller's theorem,* and the feedback capacitor, C_F, is called the *Miller capacitance.*

Notice that the effective capacitance on the input of the amplifier is multiplied by the gain of the amplifier. For big gains, $|-A_v|$, this means that the input capacitance of the amplifier can be large and can result in slow circuits. Intuitively, this can be understood by realizing that the effective voltage across C_F is $A_v + 1$ times larger than the input signal itself. This large voltage drop across C_F (one side going up by v_{in} while the other side goes down by $A_v \cdot v_{in}$) results in a large displacement current, which makes the capacitor appear larger than it really is.

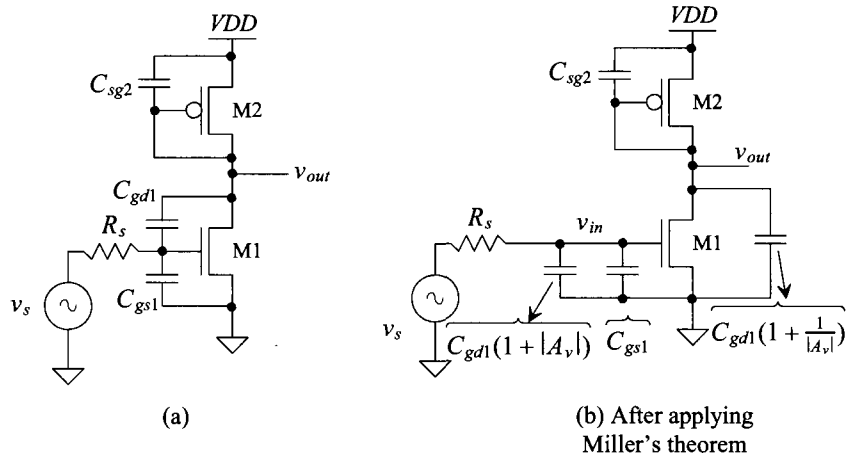
Frequency Response

Now consider the frequency response of the CS amplifier of Fig. 21.1a. The high-frequency (meaning that the device capacitances are included in the circuit) equivalent circuit is shown in Fig. 21.6a. The gate-drain capacitance of M2 isn't drawn because the gate and drain of M2 are shorted together. A source resistance is added to the circuit to model the effects of the driving source impedance. Miller's theorem is used to break C_{gd1} into two parts: a capacitance at the gate of M1 to ground and a capacitance from the drain of M1 to ground, as seen in Fig. 21.6b (note that the low-frequency gain of the amplifier in Fig. 21.1a is $-g_{m1}/g_{m2}$). Two *RC* time constants exist in this circuit: one on the input of the circuit and one on the output of the circuit. The input time constant is given by

$$\tau_{in} = R_s(C_{MI} + C_{gs1}) \tag{21.6}$$

where the Miller capacitance at the input, C_{MI}, is

$$C_{MI} = C_{gd1}\left(1 + \frac{g_{m1}}{g_{m2}}\right) \tag{21.7}$$



(a) (b) After applying Miller's theorem

Figure 21.6 Frequency response of the CS amplifier with gate-drain-connected load.

The output time constant is found in a similar way and is given by

$$\tau_{out} = \frac{1}{g_{m2}} \cdot (C_{sg2} + C_{MO}) \tag{21.8}$$

The Miller capacitance which appears at the output, C_{MO}, now becomes

$$C_{MO} = C_{gd1}(1 + \frac{g_{m2}}{g_{m1}}) \tag{21.9}$$

The frequency response of the amplifier in Fig. 21.1a (Fig. 21.6a) is given by

$$A_v(f) = \frac{-\frac{g_{m1}}{g_{m2}}}{\left(1 + j\frac{f}{f_{in}}\right)\left(1 + j\frac{f}{f_{out}}\right)} \tag{21.10}$$

where the pole associated with the amplifier's input is located at

$$f_{in} = \frac{1}{2\pi\tau_{in}} \tag{21.11}$$

and the pole associated with the amplifier's output is located at

$$f_{out} = \frac{1}{2\pi\tau_{out}} \tag{21.12}$$

The Right-Half Plane Zero

It should be noted that when using Miller's theorem a zero is neglected. If we take a look at Fig. 21.5a, we see that at high frequencies C_F shorts the amplifier's output to its input. Our model in Fig. 21.5b doesn't show this shorting. What this means for the amplifier in Fig. 21.1a or its model in Fig. 21.6a is that C_{gd1} shorts the output to the input at high frequencies.

To characterize this high-frequency effect, where we can't use Miller's theorem, consider the circuit seen in Fig. 21.7. In this figure we model the amplifier in Fig. 21.6 (or Fig. 21.1) with a small-signal resistance on the output of the circuit called $R_o = \frac{1}{g_{m2}} || r_{o2} || r_{o1} \approx \frac{1}{g_{m2}}$ and a capacitance on the output, without including C_{gd1}, of $C_o = C_{sg2}$. We don't concern ourselves with the input time constant but rather just look at the output of the circuit. Summing the currents on the output of the model results in

$$\frac{v_{out} - v_{in}}{1/j\omega C_{gd1}} + \frac{v_{out}}{R_o || 1/j\omega C_o} + g_{m1} \cdot v_{in} = 0 \tag{21.13}$$

Solving for v_{out}/v_{in} gives

$$\frac{v_{out}}{v_{in}} = -g_{m1} R_o \cdot \frac{1 - j\omega\frac{C_{gd1}}{g_{m1}}}{1 + j\omega(C_{gd1} + C_o) \cdot R_o} \tag{21.14}$$

The pole should be recognized as what we wrote in Eq. (21.12) if the gain of the amplifier is small ($A_v = -g_{m1}/g_{m2} \approx 0$). In the numerator we see a right-half plane zero at

$$f_z = \frac{g_{m1}}{2\pi C_{gd1}} \tag{21.15}$$

A zero in the right-half plane (RHP) results in the same magnitude response as a zero in the left-half plane (LHP). However, the phase response is different. A zero in the RHP has the same influence on the phase of a system as a pole in the LHP. Understanding this

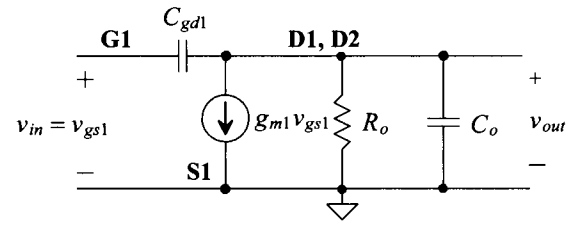


Figure 21.7 Small-signal model used to calculate the RHP zero for amplifiers in Fig. 22.1a–d.

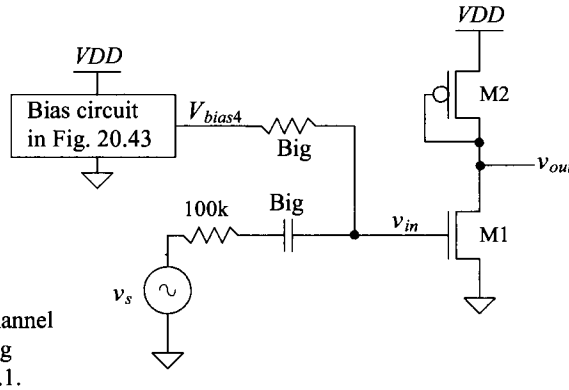
point is important. For the inverting amplifiers (which mean that at low frequencies their phase shift is 180°) in Fig. 21.1, for example, the input feeding directly to the output because of the RHP zero, without the inversion, can result in instability when the amplifier is used with feedback. The output can feed back and add to the input (positive feedback). The result is that the output of the amplifier will grow without limit (and, ultimately, the output of the amplifier will oscillate back and forth between some voltages). The magnitude response of the RHP zero is usually ignored because its value typically places it well beyond the pole frequency. However, in CMOS op-amp design, the phase shift of this RHP zero can, and will, result in stability and/or settling time issues.

Example 21.2

Determine the gain, magnitude, and phase shift of the amplifier shown in Fig. 21.8. Using an AC SPICE simulation, verify your hand calculations.

The bias circuit is used to bias the amplifier at the operating point seen in Table 9.1, that is, at a drain current of 20 μA. The big resistor and capacitor set the DC bias point but don't affect the AC operation of the circuit.

$$A_v = -\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}} = -\frac{g_{m1}}{g_{m2}} = -\frac{150\ \mu A/V}{150\ \mu A/V} = -1$$



Use the long-channel sizes and biasing seen in Table 9.1.

Figure 21.8 Amplifier used in Ex. 21.2.

From Table 9.1, C_{gs1} = 23.3 *f*F and C_{gd1} = 2 *f*F. The Miller input capacitance, because the gain of the amplifier is –1, is then 4 *f*F. The input pole is located at

$$f_{in} = \frac{1}{2\pi \cdot R_s(C_{MI} + C_{gs1})} = \frac{1}{2\pi \cdot 100k \cdot (27.3\,fF)} = 58\ MHz \qquad (21.16)$$

From Table 9.1, C_{sg2} = 70 *f*F. The Miller output capacitance is, again, 4 *f*F. The output pole is located at

$$f_{out} = \frac{1}{2\pi \cdot \frac{1}{g_{m2}} \cdot (C_{MO} + C_{sg2})} = \frac{1}{2\pi \cdot 6.5k \cdot (74\,fF)} = 331\ MHz \qquad (21.17)$$

The zero is located at

$$f_z = \frac{g_{m1}}{2\pi C_{gd1}} = \frac{150\ \mu A/V}{2\pi \cdot 2\,fF} = 11.9\ GHz$$

The transfer function of the amplifier is then

$$A_v(f) = \frac{v_{out}(f)}{v_s(f)} = -\frac{\left(1 - j\frac{f}{11.9\ GHz}\right)}{\left(1 + j\frac{f}{58\ MHz}\right)\left(1 + j\frac{f}{331\ MHz}\right)}$$

Figure 21.9 shows the AC analysis simulation results for the amplifier of Fig. 21.8. What would happen if we used v_{in} instead of v_s? We wouldn't see the input

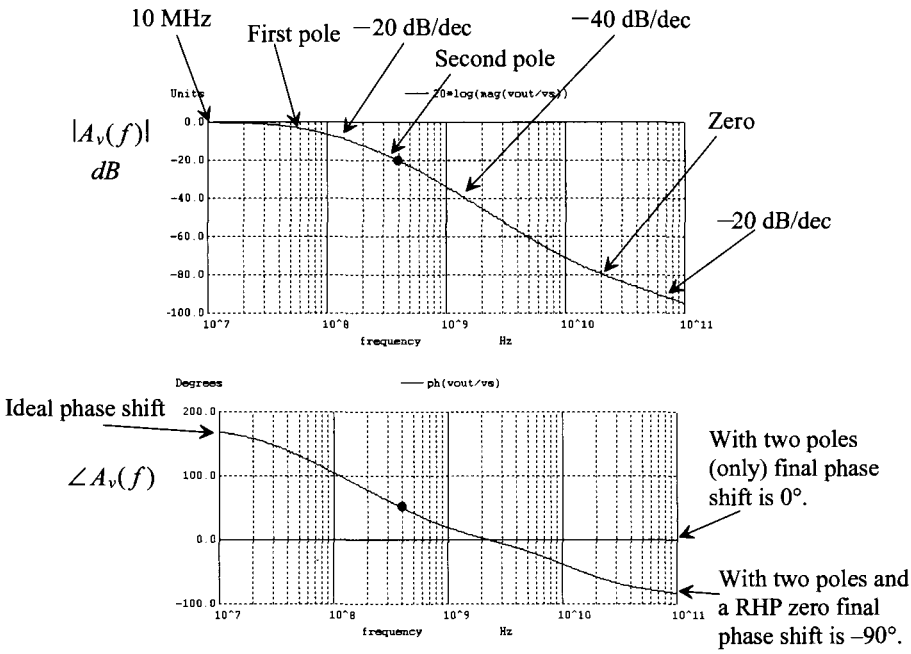


Figure 21.9 Frequency response of the amplifier in Fig. 21.8.

pole's effects on the frequency response. In the magnitude response we see that right after the first pole the gain decreases by a factor of 10 for every increase in frequency by 10 (equivalent to saying –20 dB/decade). We could also say that the gain decreases by 2 for every increase in frequency by 2 (equivalent to saying –6 dB/octave). After the second pole, the gain decreases by 100 for every increase in frequency by 10. The zero causes the frequency response to go back to –20 dB/decade. (The output and input of M1 are shorted together so that all we see are the effects of R_s charging the input capacitance of the amplifier.) It is useful to look at, and understand, the behavior of the amplifier from v_{in} to v_{out} in the simulation.

The effects of the RHP zero occur one decade before f_z. This *excess phase* shift is the problem we discussed earlier. It makes the amplifier appear not like an inverting amplifier (phase shift of –180 degrees) but rather like a noninverting amplifier sooner (at lower frequencies).

Note that magnitude of voltage gains in the neighborhood of 1 are common when using gate-drain-connected loads. At this point it may appear that this amplifier is almost worthless; however, we will see that when this amplifier is used with additional circuitry (e.g., a current source load for a differential pair), it can be very useful. ■

Example 21.3

Determine the magnitude and phase of the time-domain signal v_{out}, at 400 MHz, for the amplifier in Ex. 21.2 based on the frequency plots seen in Fig. 21.9. Verify the results using SPICE.

The magnitude response at 400 MHz is

$$\left|\frac{v_{out}}{v_s}\right| = -20\ dB = 0.1$$

and the phase response is

$$\angle\frac{v_{out}}{v_{in}} = 50° = -310°$$

The positive value means that the output is leading, or occurring earlier in time, than the input. Remembering that phase shift is simply an indication of a time delay at a particular frequency, we can write

$$50° = 360 \cdot \frac{t_d}{T} = 360 \cdot t_d \cdot 400\ MHz \rightarrow t_d \approx 350\ ps$$

for a period of 2.5 ns. We'll use an input voltage of 1 mV to ensure small-signal operation. In the simulation that generated Fig. 21.9 our input AC signal was 1 V. Again, remember that SPICE replaces the active devices with linear models in an AC simulation so any value of amplitude can be used for the input signals. Using 1 V in an AC simulation is convenient because of the ratios often used when calculating gains. Figure 21.10 shows the SPICE simulation results. Notice how the peak amplitude of the input is 1 mV while the peak amplitude of the output (remembering the DC output voltage is $VDD - V_{SG}$ or, from Table 9.1, approximately 3.85 V) is 0.1 mV (–20 db down from the low-frequency value). In

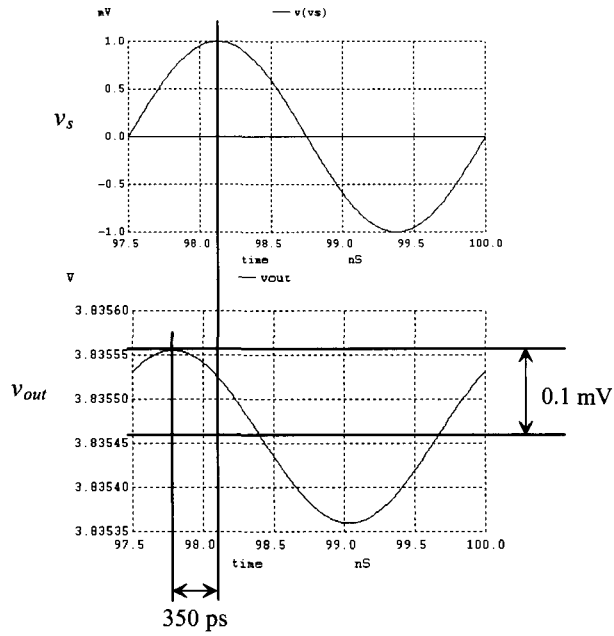


Figure 21.10 Time-domain behavior of the amplifier in Fig. 21.8 at 400 MHz.

a transient simulation we have to wait some time before the circuit settles to a stable operating point. In Fig. 21.10 we've waited 97.5 ns before looking at the output voltage. This gives the bias circuit, for example, time to turn on and generate the bias voltage needed in the amplifier (the value of the big capacitor was also reduced in this transient simulation so that its charging wouldn't increase the simulation time.) ■

A Common-Source Current Amplifier

The previous discussion was centered around CS voltage amplifiers. Next consider the circuit shown in Fig. 21.11. This amplifier can be thought of as a transimpedance amplifier, that is, voltage out and current in. The ideal input impedance of an amplifier with a current input is zero (all of the input current flows into the amplifier with this ideal input impedance). Note that the biasing of the amplifier is controlled by the current mirror formed between M3 and M1 (drawn in a different way to ensure that the reader recognizes the topology when it is seen).

The input impedance of the amplifier in Fig. 21.11 is given by

$$R_{in} = \frac{1}{g_{m3}} || r_{o3} || r_{o4} \approx \frac{1}{g_{m3}} \tag{21.18}$$

The input current, i_{in}, is determined by

$$i_{in} = g_{m3} v_{in} = g_{m3} v_{gs3} = g_{m3} v_{gs1} \tag{21.19}$$

The current through M1, and thus M2, is given by

$$i_d = g_{m1} v_{in} = \frac{g_{m1}}{g_{m3}} \cdot i_{in} \tag{21.20}$$

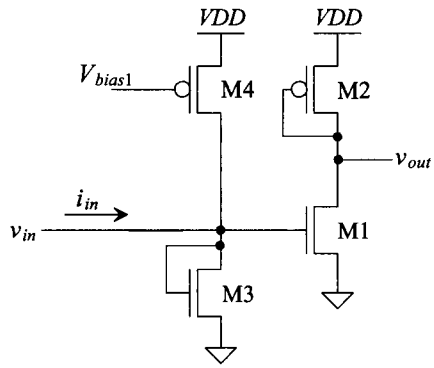


Figure 21.11 A transimpedance amplifier.

This equation can be rewritten, $g_{m3} = \beta_3(V_{GS3} - V_{THN})$ and $g_{m1} = \beta_1(V_{GS3} - V_{THN})$, as

$$\frac{i_d}{i_{in}} = \frac{\beta_1}{\beta_3} = \frac{W_1 L_3}{W_3 L_1} \tag{21.21}$$

That is, we can get a current gain simply by adjusting the size of M1 and M3. The current in M2 can then be mirrored out to a load. The transresistance gain of this configuration is given by

$$A_R = \frac{v_{out}}{i_{in}} = -\frac{i_d \frac{1}{g_{m2}}}{i_d \cdot \frac{g_{m3}}{g_{m1}}} = -\frac{g_{m1}}{g_{m2} g_{m3}} \tag{21.22}$$

Note that adding M3 and thus the resistor of value $\frac{1}{g_{m3}}$ to ground lowers the input time constant and increases the bandwidth of the amplifier.

Common-Source Amplifier with Source Degeneration

The amplifier in Fig. 21.3 is an example of a CS amplifier with source degeneration. The gain of the amplifier is reduced because the effective transconductance of the amplifier becomes

$$\frac{1}{g_{m,eff}} = \frac{1}{g_m} + R_s \tag{21.23}$$

as seen in Ex. 21.1. Adding the source resistance is useful, especially if $R_s >> 1/g_m$, to precisely set the transconductance of an amplifier. Note that we didn't, in Ex. 21.1, include the resistance looking into the drain of M1 when we wrote the "resistance in the drain." *Let's review, or again verify, how to determine the small-signal, low-frequency resistances looking into the drain and source of a MOSFET.* Using this information will greatly aid in our intuitive analysis of CMOS circuits.

Consider the test circuit shown in Fig. 21.12. Here the DC voltages ensure that the MOSFET is operating in the saturation region. We are concerned with the AC current that flows through v_t. This test voltage divided by i_d gives us the small-signal AC resistance looking into the drain of the MOSFET. In other words, this is the resistance connected to ground at the drain node.

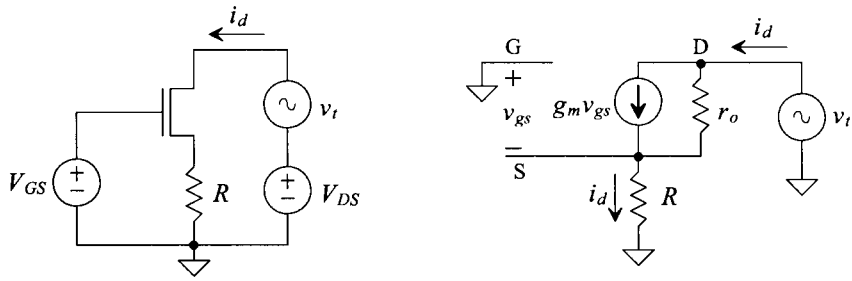


Figure 21.12 Circuit used to determine the resistance looking into the drain of a MOSFET.

Neglecting the body effect, we can write the test voltage as

$$v_t = (i_d - g_m v_{gs}) r_o + i_d R \tag{21.24}$$

where (noting $v_g = 0$ and $v_s = i_d R$)

$$v_{gs} = - i_d R \tag{21.25}$$

The resistance looking into the drain of the MOSFET is then given by

$$R_o = r_d = \frac{v_t}{i_d} = (1 + g_m R) r_o + R \approx (1 + g_m R) r_o \tag{21.26}$$

keeping in mind that $r_o \approx \frac{1}{\lambda I_D}$. For a cascoded MOSFET topology ($R = r_o$), this is approximately, as seen in Eq. (20.53), $g_m r_o^2$. For a *triple cascode*, three MOSFETs in series, ($R = g_m r_o^2$), the output resistance is

$$R_o \approx g_m^2 r_o^3 \tag{21.27}$$

noting that the output resistance goes up with each added MOSFET by the open-circuit gain, $g_m r_o$.

Example 21.4

Repeat Ex. 21.1 without neglecting the loading effects of the output resistances of M1 and M2.

The resistance looking into the drain of M2 is $\frac{1}{g_{m2}} || r_{o2}$, while the resistance looking into the drain of M1 is $r_{o1}(1 + g_{m1} R_s)$. The exact gain of the circuit is

$$A_v = \frac{v_{out}}{v_{in}} = - \frac{\frac{1}{g_{m2}} || r_{o2} || [r_{o1}(1 + g_{m1} R_s)] || R_L}{R_s + \frac{1}{g_{m1}}}$$

or when $r_{o1} || r_{o2} >> \frac{1}{g_{m2}}$, this reduces to

$$A_V = \frac{\frac{1}{g_{m2}} || R_L}{R_s + \frac{1}{g_{m1}}} \quad \blacksquare$$

The resistance in the source of the MOSFET can be found using the circuit shown in Fig. 21.13. Neglecting the body effect and output resistance of the MOSFET gives

$$v_{in} = v_{gs} + i_d R \tag{21.28}$$

Since $g_m v_{gs} = i_d$, this equation can be written as

$$v_{in} = \frac{i_d}{g_m} + i_d R = i_d\left[\frac{1}{g_m} + R\right] \tag{21.29}$$

We can look at this in a simplified manner; that is, $\frac{1}{g_m}$ is the resistance looking into the source of a MOSFET, while R is the resistance connected from the source of the MOSFET to ground.

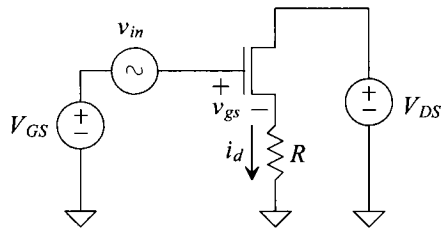


Figure 21.13 Circuit used to determine the resistance looking into the source of a MOSFET.

Noise Performance of the CS Amplifier with Gate-Drain Load

Figure 21.14 shows the CS amplifier of Fig. 21.1a with each MOSFET's model for noise power spectral density included (see Eq. [9.66]). Remembering that we only add the power from each noise source, we can write the output noise power spectral density as

$$V^2_{onoise}(f) = \left(\frac{1}{g_{m2}}\right)^2 \cdot \left(I^2_{M1} + I^2_{M2}\right) \tag{21.30}$$

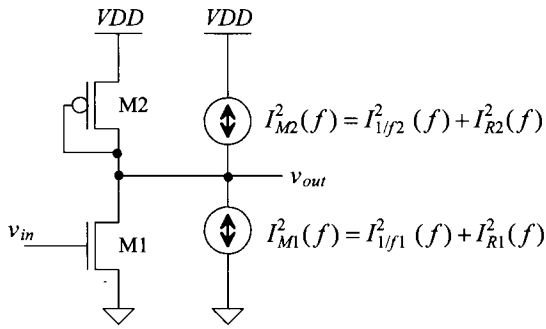


Figure 21.14 Noise modeling in a CS amplifier.

The input-referred noise power spectral density is then

$$V_{inoise}^2(f) = \frac{V_{onoise}^2(f)}{A_v^2} = \left(\frac{g_{m2}}{g_{m1}}\right)^2 \cdot \left(\frac{1}{g_{m2}}\right)^2 \cdot \left(I_{M1}^2 + I_{M2}^2\right) \tag{21.31}$$

Minimizing the input-referred noise is accomplished by making g_{m1} large. Using the expressions in Eq. (9.66), we also see that minimizing g_{m2} reduces the input-referred noise. This is equivalent to saying large A_v results in minimum input-referred noise.

21.1.2 The Source Follower (Common-Drain Amplifier)

Source-follower configurations using a gate-drain-connected load are shown in Fig. 21.15. The drain of the amplifying device, that is, the MOSFET *not* gate-drain-connected (the load), is common to both the input and the output, so this topology is often called a common-drain amplifier. Setting the bias current in this topology can be challenging. In the following we don't concern ourselves with this issue.

A source follower implemented in CMOS has an asymmetric drive capability; that is, the ability of the follower to source current is not equal to the ability to sink current for a given bias condition and AC input signal. The small-signal gain of the NMOS source follower shown in Fig. 21.15 is simply determined by a voltage divider between the resistance looking into the source of M2 ($1/g_{m2}$) with the resistance of the gate-drain-connected load, M1 ($1/g_{m1}$). The gain of the **source follower amplifier** is

$$A_v = \frac{v_{out}}{v_{in}} = \frac{\text{resistance connected to the source}}{\text{resistance connected to the source + resistance looking into the source}} \tag{21.32}$$

or for the NMOS source follower in Fig. 21.15

$$v_{in} = \overbrace{v_{gs2}}^{i_d/g_{m2}} + \overbrace{v_{out}}^{i_d/g_{m1}} \text{ where } (v_{gs1} = v_{out}) \text{ and so } v_{out} = v_{in} \cdot \frac{\frac{1}{g_{m1}}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \tag{21.33}$$

The output resistance of the source follower shown in this figure is

$$R_{out} = \frac{1}{g_{m1}} \| \frac{1}{g_{m2}} \tag{21.34}$$

Note that M2 can only source current, while M1 can only sink current, and the gain of the source follower is always less than one.

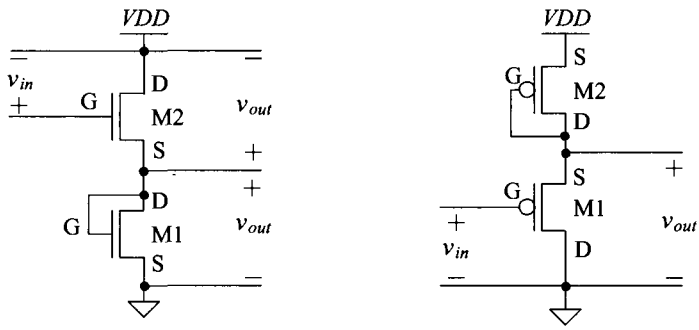


Figure 21.15 Source followers (common drain) using gate-drain loads.

21.1.3 Common Gate Amplifier

The common gate amplifier with gate-drain load is shown in Fig. 21.16. The input resistance of this amplifier is simply the resistance looking into the source of M1, or

$$R_{in} = \frac{1}{g_{m1}} \tag{21.35}$$

The gain of this **common-gate amplifier** is

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-i_d \cdot \frac{1}{g_{m2}}}{-v_{gs1}} = \frac{-i_d \cdot \frac{1}{g_{m2}}}{-i_d \cdot \frac{1}{g_{m1}}} = \frac{\text{resistance in the drain}}{\text{resistance in the source}} = \frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}} \tag{21.36}$$

or noting the positive gain

$$A_v = \frac{g_{m1}}{g_{m2}} = \sqrt{\frac{KP_n}{KP_p} \cdot \frac{W_1 L_2}{W_2 L_1}} \tag{21.37}$$

which is the same form as the gain for the CS amplifier with gate-drain load.

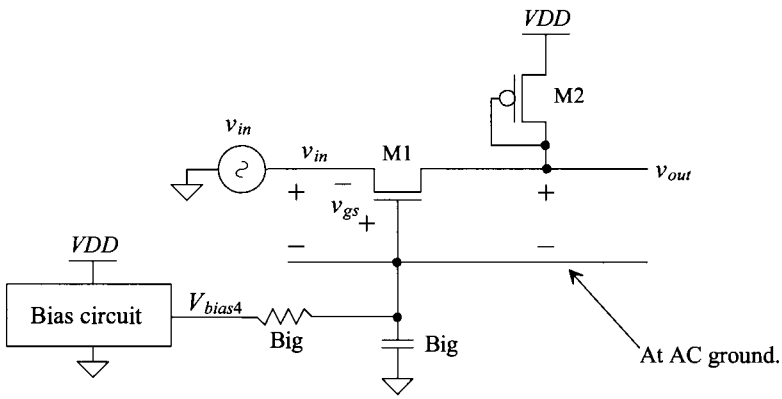


Figure 21.16 The common gate amplifier.

21.2 Current Source Loads

In the last section we talked about the gate-drain MOSFET part of a current mirror. In this section we talk about the current-source side of the mirror. The current source load provides an amplifier with the largest possible load resistance and thus the largest gain.

21.2.1 Common-Source Amplifier

Consider the CS amplifier with current source load shown in Fig. 21.17. The MOSFET M1 is the common-source component of the amplifier, while the MOSFET M2 is the current source load. The DC transfer characteristics are also seen in this figure. The amplifying portion of the curve occurs when the output is not close to *VDD* or ground (both M1 and M2 are saturated). The slope of the line when both transistors are saturated corresponds to the gain of the amplifier.

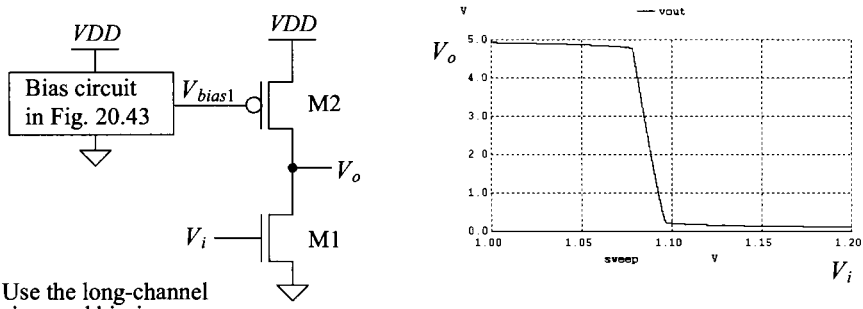


Figure 21.17 Common-source amplifier with current source load.

Class A Operation

We know from Table 9.1, and the bias circuit in Fig. 20.43, that M2 in Fig. 21.17 is biased to behave like a 20 μA current source. This means that if M1 shuts off, the maximum current we can supply to the output is 20 μA: this is important to understand. The CS amplifier in Fig. 21.17 is called a *class A* amplifier because, for proper operation, both MOSFETs are always conducting a current. In a *class B* amplifier, only one MOSFET is conducting a current at a given time. In *class AB* amplifiers (which we'll talk about later), both MOSFETs or a single MOSFET conduct a current at a given time.

Example 21.5

Estimate the maximum rate the load capacitor in Fig. 21.18 can be charged (estimate the slew rate across the load capacitor). Verify the estimate with SPICE.

The maximum current that the amplifier can source is 20 μA. The slew rate across the load is calculated using

$$I = C_L \cdot \frac{dV_{out}}{dt} \text{ or slew rate} = \frac{dV_{out}}{dt} = \frac{I}{C_L} \tag{21.38}$$

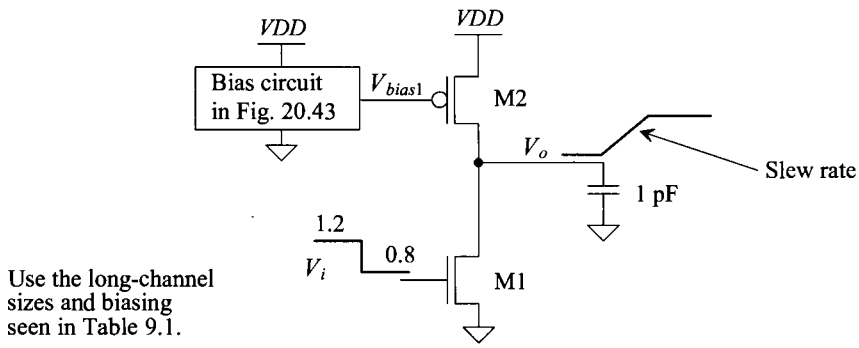


Figure 21.18 Slew rate limitations in a class A amplifier.

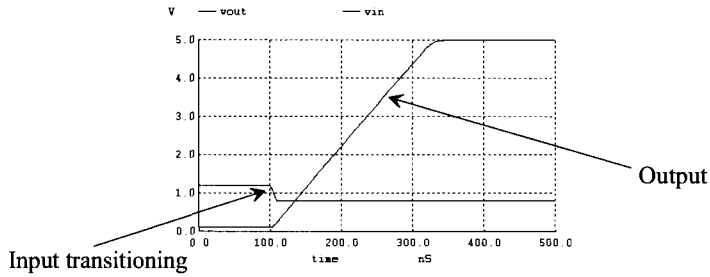


Figure 21.19 Verifying the results in Ex. 21.5

or

$$\frac{dV_{out}}{dt} = \frac{20\ \mu A}{1\ pF} = 20\ V/\mu s$$

For the output to transition 5 V requires 250 ns. ■

Small-Signal Gain

If we follow the intuitive method discussed in the last section, Eq. (21.1), the voltage gain of a common-source amplifier is the total parallel resistance at the drain of M1 divided by the resistance in the source of M1, or

$$A_v = \frac{v_o}{v_i} = -\frac{r_{o1}||r_{o2}}{\frac{1}{g_{m1}}} = -g_{m1}(r_{o1}||r_{o2}) = -\frac{g_{m1}}{g_{o1}+g_{o2}} \qquad (21.39)$$

where $r_{o1} = 1/g_{o1}$.

Open Circuit Gain

The gain of the amplifier can be increased by using a cascode current load in place of M2. The resistance looking into the drain of the cascode current source/load is much larger than the output resistance of M1. This situation is sometimes referred to as the *open circuit gain* of a common-source amplifier (see the specification in Tables 9.1 and 9.2). This specification indicates the maximum possible gain attainable with a single MOSFET (the MOSFET's load is its own output resistance r_o). The open circuit gain of M1 can be written as

$$\text{Open circuit gain} = -\frac{r_{o1}}{\frac{1}{g_{m1}}} = -g_{m1}r_{o1} = -\frac{\sqrt{2\beta_1 I_D}}{I_D\lambda_1} \qquad (21.40)$$

High-Impedance and Low-Impedance Nodes

In Fig. 21.17, the output node at the drains of M1 and M2 is termed a *high-impedance node*, that is, a node with only drain connections. The effective resistance at this node to ground is $r_{o1}||r_{o2}$. A node connected to the source of a MOSFET or a MOSFET with its drain and gate connected is termed a *low-impedance node*. The small-signal resistance looking into the source of a MOSFET and the small-signal resistance of the gate-drain (diode)-connected MOSFET are both $1/g_m$. High-impedance nodes usually have a low-frequency pole associated with them that limits the speed of the amplifier.

Frequency Response

Figure 21.20 shows the AC frequency response circuit for the CS amplifier with current source load in Fig. 21.17. *VDD* in this figure is drawn as an AC ground. The source-gate capacitance of M2 isn't shown because both sides of it are at AC ground (DC voltages), so it doesn't affect the frequency behavior of the circuit. The pole associated with the input node of the circuit is

$$f_{in} = \frac{1}{2\pi(C_{gs1} + C_{gd1}(1 + |A_v|)) \cdot R_s} \tag{21.41}$$

while the pole associated with the output node of the circuit is located at

$$f_{out} = \frac{1}{2\pi\left(C_{dg2} + C_{gd1}\left(1 + \frac{1}{|A_v|}\right)\right) \cdot r_{o1} \| r_{o2}} \tag{21.42}$$

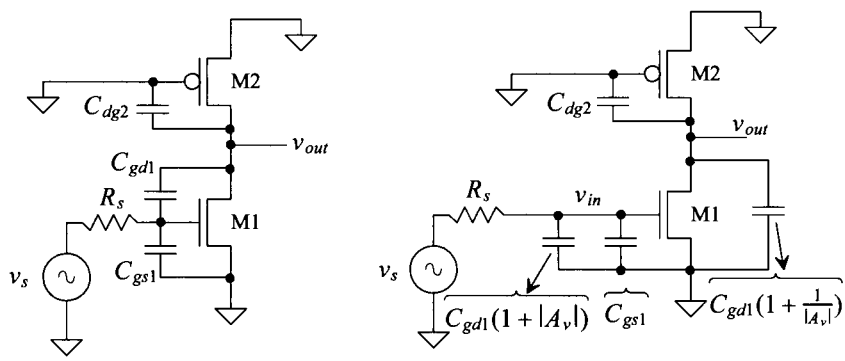
where $A_v = -g_{m1} \cdot r_{o1} \| r_{o2}$ (see Eq. [21.39]). Using Eq. (21.42) to calculate the output pole, results in a *wrong estimate* when A_v is large. As we'll see in a moment, the fact that A_v decreases above f_{in} causes v_{in} to "flatten out" because the Miller capacitance, $C_{gd1}(1 + |A_v|)$, gets smaller. The effect of v_{in} ceasing to decrease causes the output pole to appear much larger than what is predicted by Eq. (21.42). This important phenomenon is called *pole splitting*.

The zero in the transfer function (see Eq. (21.15)) is located at

$$f_z = \frac{g_{m1}}{2\pi C_{gd1}} \tag{21.43}$$

The transfer function of the amplifier is then estimated as

$$A_v(f) = -g_{m1} \cdot (r_{o1} \| r_{o2}) \cdot \frac{\left(1 - j\frac{f}{f_z}\right)}{\left(1 + j\frac{f}{f_{in}}\right)\left(1 + j\frac{f}{f_{out}}\right)} \tag{21.44}$$



(a) (b) After applying Miller's theorem

Figure 21.20 Frequency response of the CS amplifier with current source load.

We can then write the magnitude as

$$|A_v(f)| = \frac{g_{m1} \cdot (r_{o1} || r_{o2}) \cdot \sqrt{1 + \left(\frac{f}{f_z}\right)^2}}{\left(\sqrt{1 + \left(\frac{f}{f_{in}}\right)^2}\right) \cdot \left(\sqrt{1 + \left(\frac{f}{f_{out}}\right)^2}\right)} \tag{21.45}$$

and the phase shift through the amplifier as

$$\angle A_v = 180 - \tan^{-1}\left(\frac{f}{f_z}\right) - \tan^{-1}\left(\frac{f}{f_{in}}\right) - \tan^{-1}\left(\frac{f}{f_{out}}\right) \tag{21.46}$$

Example 21.6

Determine the gain, magnitude, and phase shift of the amplifier shown in Fig. 21.21. Using an AC SPICE simulation, verify your hand calculations.

For the AC small-signal analysis, the big resistor appears like an open and the big capacitor a short. These components are added to ensure that M1 is biased to sink the current supplied by M2.

The low-frequency gain of the circuit is, from Eq. (21.39) and Table 9.1,

$$|A_v| = (150\ \mu A/V) \cdot (5M\Omega || 4M\Omega) = 333\ V/V \rightarrow 50\ dB$$

The input capacitance is

$$C_{in} = (C_{gs1} + C_{gd1}(1 + |A_v|)) = (23.3 + 2 \cdot 333)fF = 691\ fF\ ! \tag{21.47}$$

The output capacitance is

$$C_{out} = \left(C_{dg2} + C_{gd1}\left(1 + \frac{1}{|A_v|}\right)\right) \approx 6 + 2\ fF = 8\ fF \tag{21.48}$$

Using Eqs. (21.41)–(21.43), we get $f_{in} = 2.3$ MHz, $f_{out} = 9$ MHz, and $f_z = 11.9$ GHz. Figure 21.22 shows the simulation results. As the discussion following Eq. (21.42) indicated, the estimate for f_{out} is wrong. To determine the correct value, let's discuss pole splitting (see Eq. [21.62]). ■

Use the long-channel sizes and biasing seen in Table 9.1.

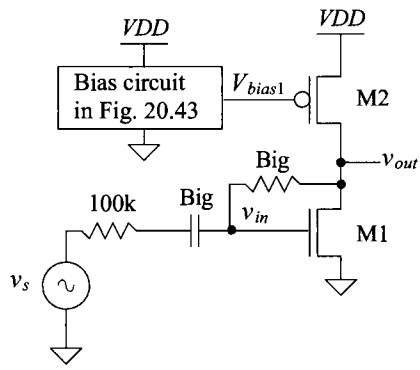


Figure 21.21 Amplifier used in Ex. 21.6.

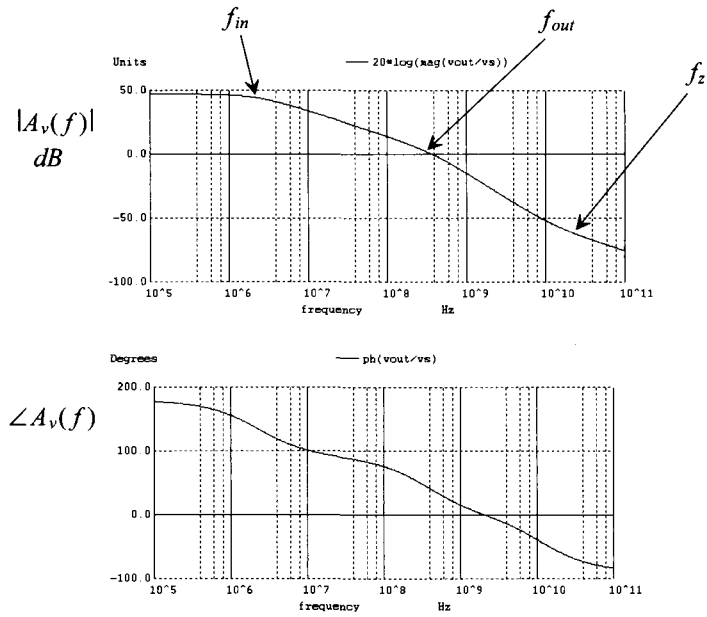


Figure 21.22 Frequency response of the amplifier in Fig. 21.21.

Pole Splitting

As discussed after Eq. (21.42), using Miller's theorem to calculate the location of the output pole when the gain of the amplifier is large results in error. Clearly, as just demonstrated in Ex. 21.6, the calculated value of f_{out} is 9 MHz while the SPICE simulation in Fig. 21.22 shows that f_{out} is approximately 200 MHz. The source of this discrepancy can be traced to the fact that above f_{in} the gain of the amplifier, A_v, decreases causing the effective input capacitance of the amplifier to decrease. As seen in Fig. 21.23, this causes the input voltage to "flatten out" instead of continuing to fall at –20 dB/decade. The result is the second, or output pole, appears to split from (leave) the first,

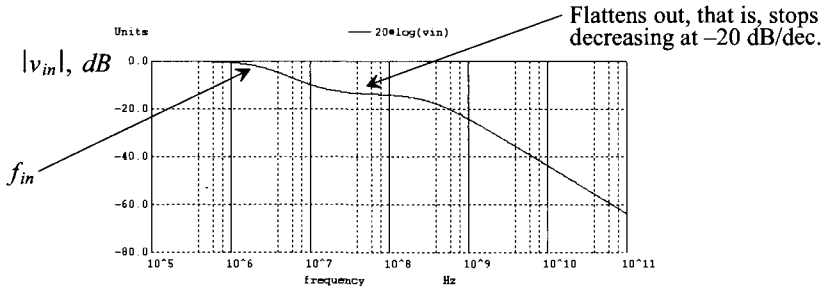


Figure 21.23 Showing how the amplifier's, in Fig. 21.21, input voltage flattens out as the gain decreases.

or input pole, and move to a higher frequency. Note that if we resimulate the amplifier in Fig. 21.21 with the source resistance set to zero ohms (so there isn't an input pole), pole splitting isn't present and Eq. (21.42) can be used to calculate the location of the output pole.

To characterize this effect, let's use the circuit in Fig. 21.7 with the addition of a source resistance, R_s, as seen in Fig. 21.24. In this figure, $R_o = r_{o1} \| r_{o2}$ and $C_o = C_{dg2}$. From Eq. (21.14), we can write

$$\frac{v_{out}}{v_{in}} = -g_{m1} R_o \cdot \frac{1 - j\omega \frac{C_{gd1}}{g_{m1}}}{1 + j\omega (C_{gd1} + C_o) \cdot R_o} \tag{21.49}$$

At the gate of M1, we can write

$$\frac{v_{in} - v_s}{R_s} + \frac{v_{in}}{1/j\omega C_{gs1}} + \frac{v_{in} - v_{out}}{1/j\omega C_{gd1}} = 0 \tag{21.50}$$

or

$$v_{in} = \frac{\frac{v_s}{R_s} + v_{out} \cdot j\omega C_{gd1}}{\frac{1}{R_s} + j\omega C_{gs1} + j\omega C_{gd1}} \tag{21.51}$$

Substituting Eq. (21.51) into Eq. (21.49) gives

$$v_{out} = -g_{m1} R_o \cdot \frac{1 - j\omega \frac{C_{gd1}}{g_{m1}}}{1 + j\omega (C_{gd1} + C_o) \cdot R_o} \cdot \frac{\frac{v_s}{R_s} + v_{out} \cdot j\omega C_{gd1}}{\frac{1}{R_s} + j\omega C_{gs1} + j\omega C_{gd1}} \tag{21.52}$$

or, with $s = j\omega$,

$$\frac{v_{out}}{v_s} =$$

$$\frac{-g_{m1} R_o \cdot \left(1 - s \frac{C_{gd1}}{g_{m1}}\right)}{s^2 [R_o R_s (C_{gd1} C_{gs1} + C_o C_{gs1} + C_o C_{gd1})] + s[(C_{gd1} + C_o) R_o + (C_{gs1} + C_{gd1}) R_s + C_{gd1} g_{m1} R_o R_s] + 1} \tag{21.53}$$

The zero is still, as indicated in Eqs. (21.15) and (21.43), located at

$$f_z = \frac{g_{m1}}{2\pi C_{gd1}} \tag{21.54}$$

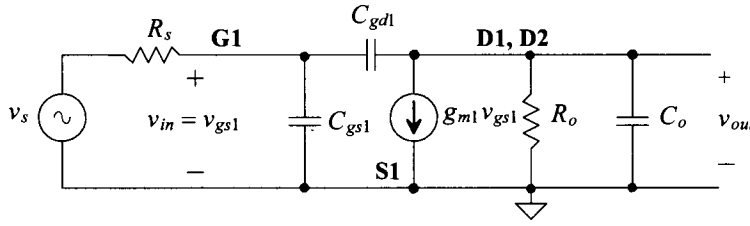


Figure 21.24 Circuit used to calculate the transfer function of the amplifier in Fig. 21.21.

At low frequencies the denominator is approximately (the coefficient of the s^2 term is small)

$$1 + j\omega \cdot [(C_{gd1} + C_o)R_o + (C_{gs1} + C_{gd1})R_s + C_{gd1}g_{m1}R_oR_s] \tag{21.55}$$

and so the low-frequency pole, using $|A_v| = g_{m1}(r_{o1} || r_{o2}) = g_{m1}R_o$, $C_o = C_{dg2}$, is located at

$$f_1 \approx \frac{1}{2\pi[(C_{gd1} + C_{dg2}) \cdot r_{o1} || r_{o2} + (C_{gs1} + C_{gd1}(1 + |A_v|)) \cdot R_s]} \tag{21.56}$$

If $C_{gd1}(1 + |A_v|)$ is much larger than the other capacitances,

$$f_1 \approx \frac{1}{2\pi C_{gd1}(1 + |A_v|) \cdot R_s} \tag{21.57}$$

Notice the similarity to Eq. (21.41), where the pole is associated with the input of the amplifier. Further notice that if we had used this result in Ex. 21.6, the input pole would have changed very little. Also notice that if $R_s = 0$, then

$$f_1 \approx \frac{1}{2\pi(C_{gd1} + C_{dg2}) \cdot r_{o1} || r_{o2}} \tag{21.58}$$

Notice the similarity to Eq. (21.42), where the pole is associated with the output of the amplifier. To determine the location of the second root of the denominator (the second pole location, f_2), let's factor Eq. (21.55) from the denominator of Eq. (21.53) or

$$[1 + s[(C_{gd1} + C_o)R_o + (C_{gs1} + C_{gd1})R_s + C_{gd1}g_{m1}R_oR_s]] \cdot \left(1 + \frac{s^2[R_oR_s(C_{gd1}C_{gs1} + C_oC_{gs1} + C_oC_{gd1})]}{s[(C_{gd1} + C_o)R_o + (C_{gs1} + C_{gd1})R_s + C_{gd1}g_{m1}R_oR_s] + 1}\right) \tag{21.59}$$

where this equation is in the form

$$\left(1 + j \cdot \frac{f}{f_1}\right) \cdot \left(1 + j \cdot \frac{f}{f_2}\right) \tag{21.60}$$

Note again that if $R_s = 0$, the second term in Eq. (21.59) goes to unity. Looking at the second term of Eq. (21.59), let's divide the numerator and denominator by sR_oR_s

$$1 + j \cdot \frac{2\pi f \cdot (C_{gd1}C_{gs1} + C_oC_{gs1} + C_oC_{gd1})}{(C_{gd1} + C_o)/R_s + (C_{gs1} + C_{gd1})/R_o + C_{gd1}g_{m1} + 1/sR_oR_s} \tag{21.61}$$

In any practical MOSFET amplifier, $g_m >> 1/r_o$ (if not, then the magnitude of the open circuit gain, Eq. (21.40), is too small for the MOSFET to be of practical value as an amplifying device). Also, the R_s is assumed to be large (if not, then f_2 is not used), that is, the amplifier's transfer function has a single-pole response, where the pole is associated with the output of the amplifier as seen in Eq. (21.58). We can therefore write

$$f_2 \approx \frac{g_{m1}C_{gd1}}{2\pi \cdot (C_{gd1}C_{gs1} + C_oC_{gs1} + C_oC_{gd1})} \tag{21.62}$$

Calculating the location of the second pole in Ex. 21.6 with this equation results in $f_2 =$ 240 MHz (which is very close to the simulated location).

Why the name pole splitting? If we increase the effective size of C_{gd1} by placing a capacitor, C_c, from the amplifier's input to its output (so that C_c is in parallel with C_{gd1}, that is, the effective value is $C_c + C_{gd1}$), then, as Eq. (21.56) shows, the low-frequency location of the pole, f_1, decreases. At the same time, increasing the effective size of C_{gd1} causes the location of the high-frequency pole f_2, as seen in Eq. (21.62), to increase. Thus the name *pole splitting.*

Pole Splitting Summary

Because of the ubiquity of pole splitting in CMOS amplifier design, let's summarize our discussion using a generic model, Fig. 21.25. In terms of the parameters seen in this figure the location of the zero is now

$$f_z = \frac{g_{m2}}{2\pi \cdot C_c} \tag{21.63}$$

The first pole is located at

$$f_1 \approx \frac{1}{2\pi[(C_c + C_2) \cdot R_2 + (C_1 + C_c(1 + g_{m2}R_2)) \cdot R_1]} \tag{21.64}$$

For large gain, $g_{m2}R_2$, we can simplify this to

$$f_1 \approx \frac{1}{2\pi g_{m2}R_2R_1C_c} \tag{21.65}$$

The second pole is located at

$$f_2 \approx \frac{g_{m2}C_c}{2\pi \cdot (C_cC_1 + C_1C_2 + C_cC_2)} \tag{21.66}$$

The transfer function is then written as

$$A_v(f) = \frac{v_{out}(f)}{v_s(f)} = g_{m1}R_1g_{m2}R_2 \cdot \frac{\left(1 - j \cdot \frac{f}{f_z}\right)}{\left(1 + j \cdot \frac{f}{f_1}\right) \cdot \left(1 + j \cdot \frac{f}{f_2}\right)} \tag{21.67}$$

where $A_v = g_{m1}R_1g_{m2}R_2$ (the gain is now positive because of the defined direction of the current source in Fig. 21.25).

Again note that if C_c is increased, f_1 moves downwards and f_2 moves upwards (pole splitting). Also note that if the capacitor, C_c, is made large (quite common), then f_1 is much lower than the location of the other pole or the zero (the pole associated with f_1 is

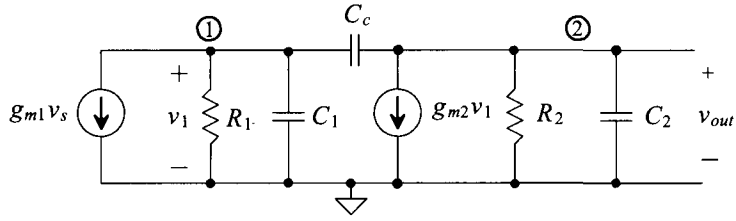


Figure 21.25 Generic model used to estimate bandwidth in a CMOS amplifier.

said to be the *dominant pole*). The amplifier's transfer function, with the help of Eq. (21.65), can be written as

$$A_v(f) = \frac{v_{out}(f)}{v_s(f)} \approx \frac{g_{m1}R_1 g_{m2}R_2}{\left(1 + j \cdot \frac{f}{f_1}\right)} = \frac{g_{m1}R_1 g_{m2}R_2}{(1 + j \cdot 2\pi f \cdot g_{m2}R_2 R_1 C_c)} \tag{21.68}$$

This equation is in the form

$$A_v(f) = \frac{v_{out}(f)}{v_s(f)} = \frac{A_{DC}}{1 + j \cdot \frac{f}{f_{3dB}}} \tag{21.69}$$

where

$$A_{DC} = g_{m1}R_1 g_{m2}R_2 \text{ and } f_{3dB} = \frac{1}{2\pi g_{m2}R_2 R_1 C_c} \tag{21.70}$$

The magnitude and phase responses of a generic CMOS amplifier are seen in Fig. 21.26. Note that at frequencies much larger than the amplifier's 3 dB frequency, that is, $f/f_{3dB} >> 1$, Eq. (21.68) can be written as

$$A_v(f) = \left|\frac{v_{out}(f)}{v_s(f)}\right| \approx \frac{g_{m1}}{2\pi f \cdot C_c} \tag{21.71}$$

To determine the frequency, f_{un}, where the transfer function is unity, we set Eq. (21.71) to one and solve to yield

$$f_{un} = \frac{g_{m1}}{2\pi C_c} \tag{21.72}$$

We've derived some very useful equations, so let's apply them in some examples.

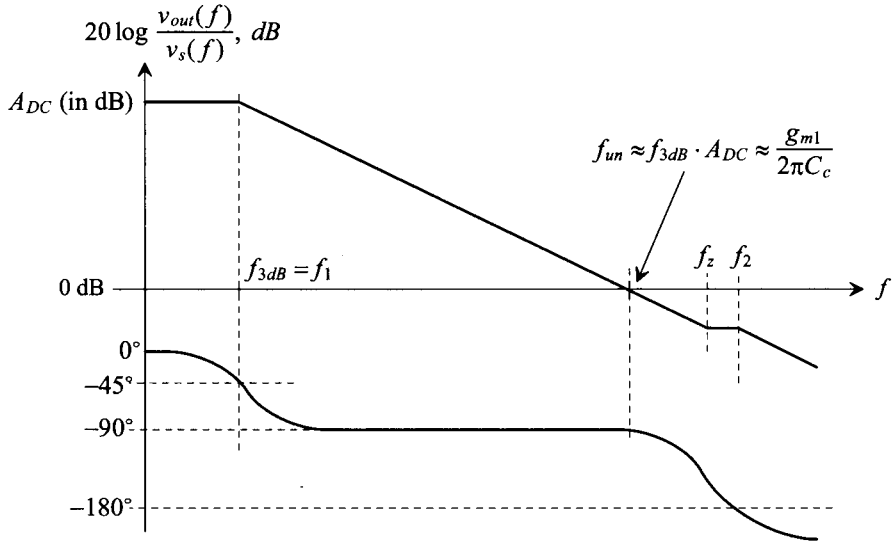


Figure 21.26 Magnitude and phase responses of a generic CMOS amplifier.

Example 21.7

Repeat Ex. 21.6 using the model in Fig. 21.25.

Using the model parameters in Fig. 21.25 and looking at Figs. 21.20a and 21.21, we can write (with the help of Table 9.1)

$$R_1 = R_s = 100\text{k},\ C_1 = C_{gs1} = 23.3\,fF,\ C_c = C_{gd1} = 2\,fF,$$

$$C_2 = C_{dg2} = 6\,fF,\ R_2 = r_{o1} \| r_{o2} = 2.22\ \text{M}\Omega$$

$$g_{m2}\ (\text{in Fig. 21.25}) = g_{m1}\ (\text{in Fig. 21.21}) = 150\ \mu A/V$$

$$g_{m1}\ (\text{in Fig. 21.25}) = 1/R_s\ (\text{in Fig. 21.21}) = 10\ \mu A/V$$

Using Eq. (21.67) or (21.70), we have $|A_v| = 333\ V/V \rightarrow 50\ dB$. Using Eq. (21.63), we get $f_z = 11.9\ GHz$; Eq. (21.65), we get $f_1 = 2.3\ MHz$; and finally using Eq. (21.66), we get $f_2 = 240\ MHz$. These calculations should be compared to the simulation results seen in Fig. 21.22. ■

Example 21.8

Repeat Ex. 21.7 if R_s is zero. Verify the hand calculations using SPICE.

Again we use the model seen in Fig. 21.25. From Ex. 21.7, $g_{m1}R_1$ is unity (and so R_s doesn't affect the gain). Further, the location of the zero doesn't change. Since R_s is zero ($R_1 = 0$ so the current source, $g_{m1}v_s$, and the resistor, R_1 in Fig. 21.25 are replaced with a voltage source, v_s), the location of f_2 is moved to an infinite frequency (as seen in Eq. [21.59]). Using Eq. (21.64), we get

$$f_1 \approx \frac{1}{2\pi(C_{gd1} + C_{dg2}) \cdot r_{o1} \| r_{o2}} = \frac{1}{2\pi(8\,fF) \cdot 2.22M} = 9\ MHz$$

The simulation results are seen in Fig. 21.27. Note the small perturbation in the frequency response above f_1. The response is not perfectly decreasing at −20 dB/decade. This imperfection can be traced to the bias voltage, V_{bias1}, used on the gate of M2. It is not a perfect AC ground as was assumed in our hand calculations. By placing a capacitor on the gate of M2 to ground, the variation in V_{bias1} is reduced and the amplifier behaves as expected. This is an *important point.* It is often a good idea to "bypass" the bias voltages to AC ground to reduce their impedance in practical design. This also keeps circuits that are biased from the same bias circuit from interacting. ■

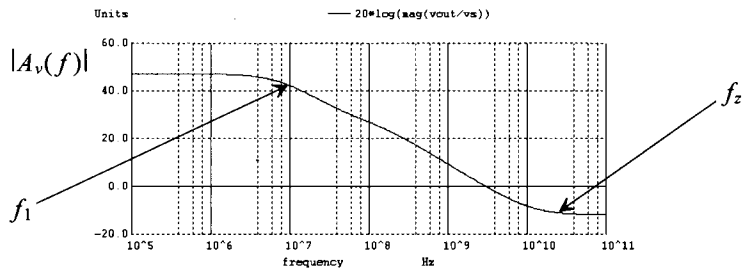


Figure 21.27 Simulation results for Ex. 21.8.

Example 21.9

Determine the frequency response of the amplifier seen in Fig. 21.28. Verify the hand calculations using simulations.

Use the long-channel sizes and biasing seen in Table 9.1.

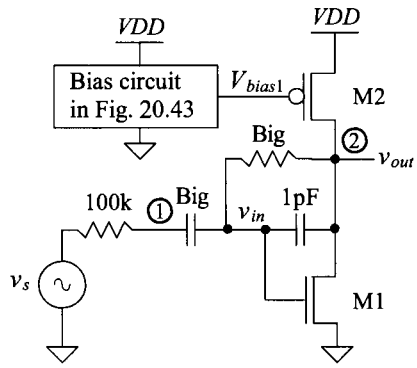


Figure 21.28 Amplifier used in Ex. 21.9.

The only thing that is different between this amplifier and the one in Ex. 21.7 is the value of C_c. In Fig. 21.28

$$C_c = 1\,pF + C_{gd1} \approx 1\,pF$$

We can then write, using Eq. (21.65)

$$f_1 \approx \frac{1}{2\pi \cdot (150\ \mu A/V) \cdot 100k \cdot 2.2MEG \cdot 1pF} = 4.8\ kHz$$

using Eq. (21.66)

$$f_2 \approx \frac{(150\ \mu A/V) \cdot 1p}{2\pi \cdot (1p \cdot 23.3f + 23.3f \cdot 6f + 1p \cdot 6f)} = 811\ MHz$$

At the risk of stating the obvious, these two poles are split apart by a great distance with the addition of the 1 pF capacitor. The zero, from Eq. (21.63), is located at

$$f_z = \frac{150\ \mu A/V}{2\pi \cdot 1p} = 23\ MHz$$

The unity-gain frequency is found using Eq. (21.72) with $R_s = 1/g_{m1}$.

$$f_{un} = \frac{1}{2\pi R_s C_c} = 1.59\ MHz$$

The simulation results are seen in Fig. 21.29. The value of the gain is 47 dB (we calculated 50 dB). The value of the first pole is approximately 6 kHz (we calculated 4.8 kHz). The small discrepancies are most likely the result of differences in the actual circuit parameters compared to the values we used in the formulas. ■

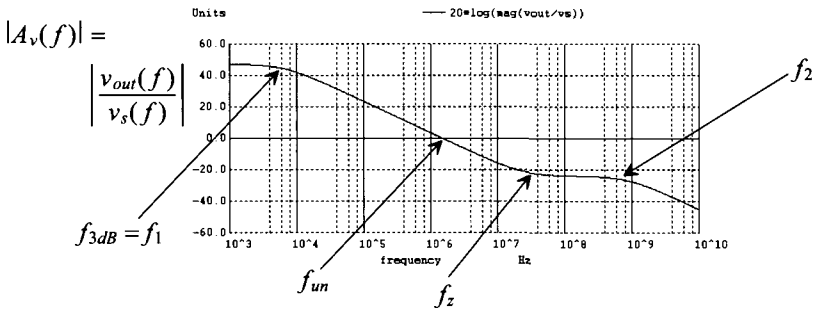


Figure 21.29 Frequency response of the amplifier in Fig. 21.28.

Example 21.10

Estimate the frequency response of the amplifier seen in Fig. 21.30. Verify the estimates with SPICE.

MA's gate and drain, at DC, are at the same potential. This biases MB to sink the right amount of current from MD.

Using the model in Fig. 21.25, we see that the source voltage, v_s, modulates the drain current in MA. We can therefore write

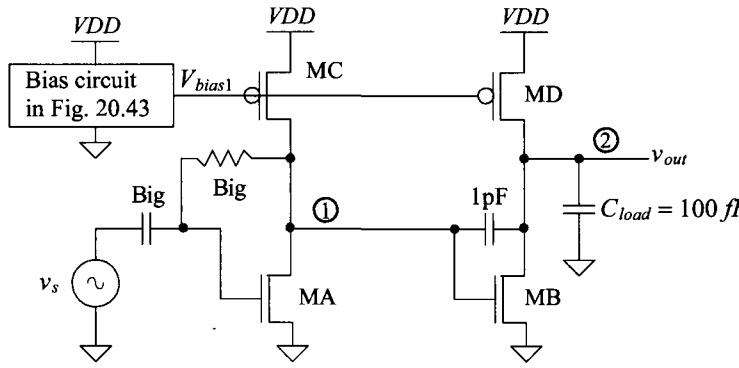
$$g_{mA} v_s = g_{m1} v_s \rightarrow g_{m1} \text{ (in Fig. 21.25)} = g_{mA} \text{ (in Fig. 21.30)} = 150\ \mu A/V$$

$$g_{m2} \text{ (in Fig. 21.25)} = g_{mB} \text{ (in Fig. 21.30)} = 150\ \mu A/V$$

$$R_1 = r_{oA} || r_{oC} = \ R_2 = r_{oB} || r_{oD} = 2.22\ M\Omega$$

To determine the capacitance on nodes 1 and 2, we can use Fig. 21.31. At node 1

$$C_1 = C_{gdA} + C_{dgC} + C_{gsB} = 31.3\,fF$$



Use the long-channel sizes and biasing seen in Table 9.1.

Figure 21.30 Amplifier used in Ex. 21.10.

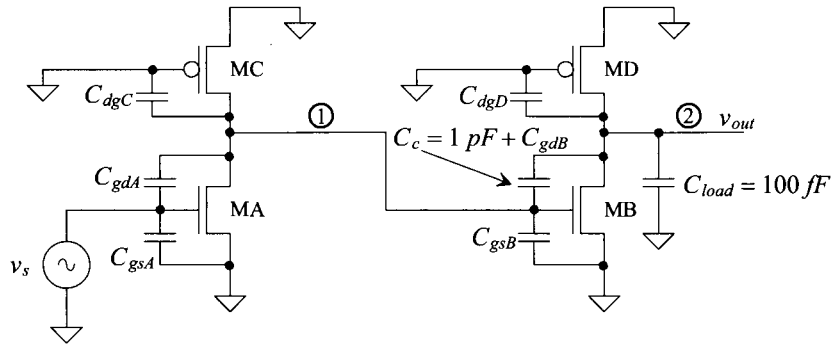


Figure 21.31 The capacitances for the amplifier in Fig. 21.30.

where C_{gdA} is the output Miller capacitance of MA ($C_{gdA} \approx C_{gdA}\left(1+\frac{1}{|A|}\right)$ when the gain of MA is large). At node 2

$$C_2 = C_{load} + C_{dgD} = 106\,fF$$

The value of C_c is

$$C_c = 1\,pF + C_{gdB} \approx 1\,pF \text{ (just the added capacitor)}$$

The gain of the topology is estimated as

$$A_{DC} = g_{m1}R_1 g_{m2}R_2 = (150\ \mu A/V)^2(2.22\ M\Omega)^2 = 110,889\ V/V \rightarrow 101\ dB$$

The poles and zero can be calculated using Eqs. (21.63), (21.65), and (21.66)

$$f_z = \frac{150\ \mu A/V}{2\pi \cdot 1.002\,pF} = 23\ MHz$$

$$f_1 \approx \frac{1}{2\pi \cdot (150\ \mu A/V)(2.22\ M\Omega)^2(1.002\,pF)} = 214\ Hz$$

$$f_2 \approx \frac{(150\ \mu A/V) \cdot 1.002}{2\pi \cdot (1.002 \cdot 0.0313 + 0.0313 \cdot 0.106 + 1.002 \cdot 0.106)\,pF} = 170\ MHz$$

The location of the unity gain frequency is calculated using Eq. (21.72) as 23 MHz. The simulation results are seen in Fig. 21.32. ■

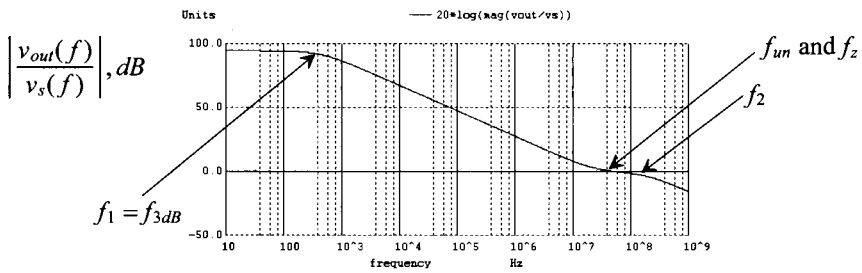


Figure 21.32 Frequency response of the amplifier in Fig. 21.30.

Canceling the RHP Zero

Notice in Ex. 21.10 that the unity-gain frequency (the frequency where the gain is one) is equal to the frequency of the zero. As mentioned earlier, the input of the amplifier feeds directly through C_c to the amplifier's output without the phase inversion. If the gain of the amplifier is larger than one (or even slightly less than one), then the lack of inversion, when the amplifier uses feedback, can result in an unstable amplifier. The amplifier's output signal feeds back and adds to its input signal without the inversion through the amplifier. To avoid this situation, we might add an amplifier in series with C_c that allows the output to feed back to the input through C_c but not vice versa, Fig. 21.33a. A simpler solution is to add a resistor in series with the capacitor, Fig. 21.33b, to attenuate the higher frequency signals (where the zero occurs) and push the zero out to a higher frequency. Adding the resistor moves the zero to a frequency (see Eq. [21.63])

$$f_z = \frac{1}{2\pi \cdot C_c \cdot \frac{1}{g_{m2}}} \xrightarrow{\text{With a resistor}} f_z = \frac{1}{2\pi \cdot C_c \cdot \left(\frac{1}{g_{m2}} - R_z\right)} \qquad (21.73)$$

If $R_z = 1/g_{m2}$, the zero disappears (is pushed to an infinite frequency). If $R_z > 1/g_{m2}$, the zero is pushed back into the LHP (phase shift is opposite from the poles). *Any practical design where pole splitting is used should include the zero-nulling resistor* R_z. Consider the following example.

Figure 21.33 Removing the zero in the amplifier's transfer function.

Example 21.11

Using a zero-nulling resistor, show that the location of the zero in the frequency response of the amplifier in Fig. 21.30 can be eliminated.

In this amplifier, $R_z = 1/g_{m2} = 6.5\ k\Omega$. By adding this resistor in series with the 1 pF capacitor, we get the frequency response seen in Fig. 21.34. Note that the zero is still seen but at a considerably higher frequency. ■

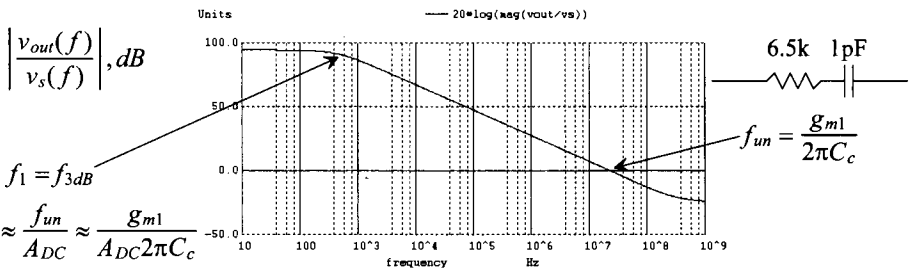


Figure 21.34 Pushing the zero in Fig. 21.32 to a higher frequency.

Noise Performance of the CS Amplifier with Current Source Load

To determine the noise performance of the CS amplifier with current source load, we can use the schematic in Fig. 21.14 with the gate of M2 at AC ground. The output noise power spectral density is then

$$V_{onoise}^2(f) = (r_{o1} \| r_{o2})^2 \cdot \left(I_{M1}^2 + I_{M2}^2\right) \tag{21.74}$$

The input-referred noise is then

$$V_{inoise}^2(f) = \frac{V_{onoise}^2(f)}{A_v^2} = \frac{1}{g_{m1}^2} \cdot \left(I_{M1}^2 + I_{M2}^2\right) \tag{21.75}$$

showing once again that to minimize the input-referred noise we need to make the transconductance of M1 large (or, in other words, make A_v large).

21.2.2 The Cascode Amplifier

Consider a CS amplifier with current source load as seen Fig. 21.17 but implemented using the short-channel CMOS process. Using the parameters in Table 9.2, the gain of the topology, Eq. (21.39), is only 16.7 (it was 333 using the long-channel process). To boost the gain of the single-stage amplifier and to eliminate, or more correctly to reduce, the Miller effect, consider the cascode amplifier seen in Fig. 21.35. The resistance looking into the drain of M3 is $g_{mp} \cdot r_{op}^2$ (see Table 20.1) with a value of 16.6 MΩ. The resistance looking into the drain of M2 is 4.2 MΩ (again from Table 20.1). The gain of the cascode amplifier is the resistance in the drain divided by the resistance in the source of the amplifying device (M1) or

$$\frac{v_{out}}{v_{in}} = -\frac{g_{mn}r_{on}^2 \| g_{mp}r_{op}^2}{1/g_{mn}} = -g_{mn} \cdot R_{ocas} \tag{21.76}$$

Using the bias circuit from Fig. 20.47 and the sizes in Table 9.2 (and thus the small-signal parameters in this table).

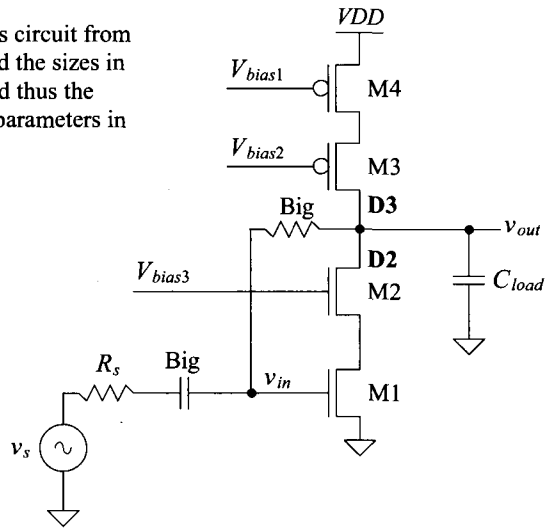


Figure 21.35 A cascode amplifier.

where

$$R_{ocas} = g_{mn} r_{on}^2 || g_{mp} r_{op}^2 \tag{21.77}$$

Using the parameters from Table 9.2, the gain of the cascode amplifier in Fig. 21.35 is, roughly, 500.

Frequency Response

The resistance seen in the drain of M1 is approximately $r_o/2$ (see Fig. 21.37 and Eq. [21.82]). The gain from the gate of M1 (the amplifier's input) to the drain of M1 is then

$$A_{v1} = \frac{v_{d1}}{v_{in}} = \frac{-v_{gs2}}{v_{gs1}} \approx \frac{-i_d \cdot r_o/2}{i_d/g_{m1}} = -g_{m1} \cdot \frac{r_o}{2} \tag{21.78}$$

If we calculate the Miller capacitance, Eq. (21.5), we see that the lower the gain of M1 the less loading (from the Miller capacitance) on the input of the amplifier. From Table 9.2, g_{m1} = 150 μA/V and, from Fig. 9.32 (knowing M1 is biased close to a $V_{DS,sat}$ of 70 mV), r_o is 50k then $A_{v1} = -g_{m1} \cdot \frac{r_o}{2} = -3.75$ (let's use this result in the following example).

Example 21.12

Estimate the frequency response of the cascode amplifier in Fig. 21.35 if R_s is 100k and $C_L = 100\,fF$. Verify the hand calculations with simulations.

The input time constant is calculated as

$$\tau_{in} = R_s \cdot (C_{gs1} + (1 + |A_{v1}|) \cdot C_{gd1})$$

or

$$\tau_{in} = 100k \cdot (4.17\,fF + 4.75 \cdot 1.56\,fF) = 1.16\,ns$$

The pole associated with this input time constant is then

$$f_{in} = \frac{1}{2\pi\tau_{in}} = 137\ MHz$$

Since the load capacitance is large, $C_{load} >> C_{gd2} + C_{dg3}$, we can write

$$\tau_{out} = R_{ocas} \cdot (C_{load} + C_{gd2} + C_{dg3}) \approx g_{mn} r_{on}^2 || g_{mp} r_{op}^2 \cdot C_{load} = 335\,ns$$

and so the pole associated with the output node is located at

$$f_{out} = \frac{1}{2\pi\tau_{out}} = 475\ kHz$$

Again, the gain of the topology is 500 (54 dB). The simulation results are seen in Fig. 21.36. The magnitude response is

$$\left|\frac{v_{out}}{v_s}\right| = \frac{500}{\sqrt{1 + \left(\frac{f}{475kHz}\right)^2} \cdot \sqrt{1 + \left(\frac{f}{137\ MHz}\right)^2}}$$

and the phase response (in degrees) is

$$\angle\frac{v_{out}}{v_{in}} = 180 - \tan^{-1}\frac{f}{475\ kHz} - \tan^{-1}\frac{f}{137\ MHz} \quad \blacksquare$$

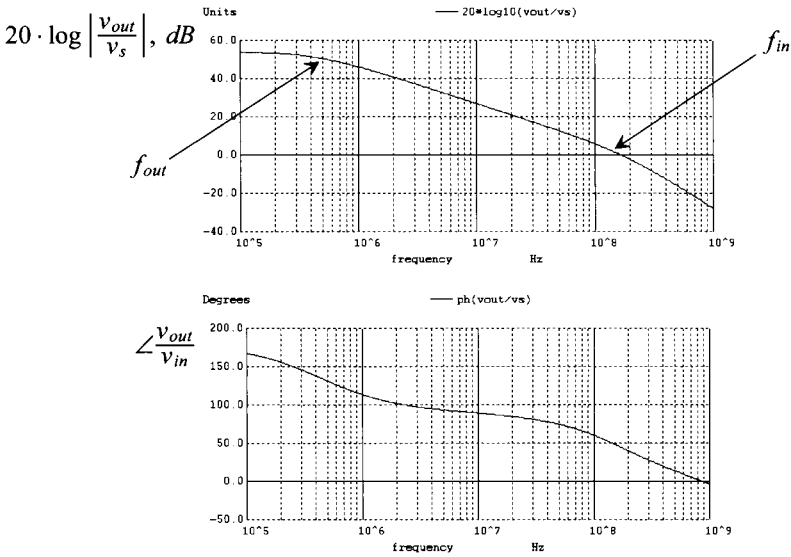


Figure 21.36 The simulation results for Ex. 21.12.

Class A Operation

The cascode amplifier in Fig. 21.35 is another example of a class A amplifier. When the input of the amplifier goes sufficiently negative, M1 shuts off. M3 and M4 are a current source and so the maximum rate that the load capacitance can be charged is given by Eq. (21.38). For the amplifier in Fig. 21.35, this is 10 μA/100 *fF* or 100 mV/ns.

Noise Performance of the Cascode Amplifier

The cascode's output noise power spectral density is given by

$$V_{onoise}^2(f) = \left(g_{mn} r_{on}^2 || g_{mp} r_{op}^2\right)^2 \left(I_{M1}^2 + I_{M4}^2\right) \qquad (21.79)$$

where the noise contributions from M2/M3 are negligible, see Fig. 21.44. The input-referred noise power is then ($g_{m1} = g_{mn}$)

$$V_{inoise}^2(f) = \frac{V_{onoise}^2(f)}{A_v^2} = \frac{\left(I_{M1}^2 + I_{M4}^2\right)}{\left(g_{m1}\right)^2} \qquad (21.80)$$

Again, maximizing the transconductance of the amplifying device (equivalent to saying maximizing the gain of the amplifier) reduces the input-referred noise.

Operation as a Transimpedance Amplifier

Figure 21.37 shows a transimpedance amplifier (current input and voltage output). Note that the AC voltages between the gates and sources of M1 and M4 are zero (both the gates and the sources are at AC ground). From the figure the input resistance is

$$R_{in} = \frac{-v_{in}}{i_{in}} = \frac{1 + \frac{R_{ocasp}}{r_{on}}}{g_{mn} + \frac{2}{r_{on}} + \frac{R_{ocasp}}{r_{on}^2}} \qquad (21.81)$$

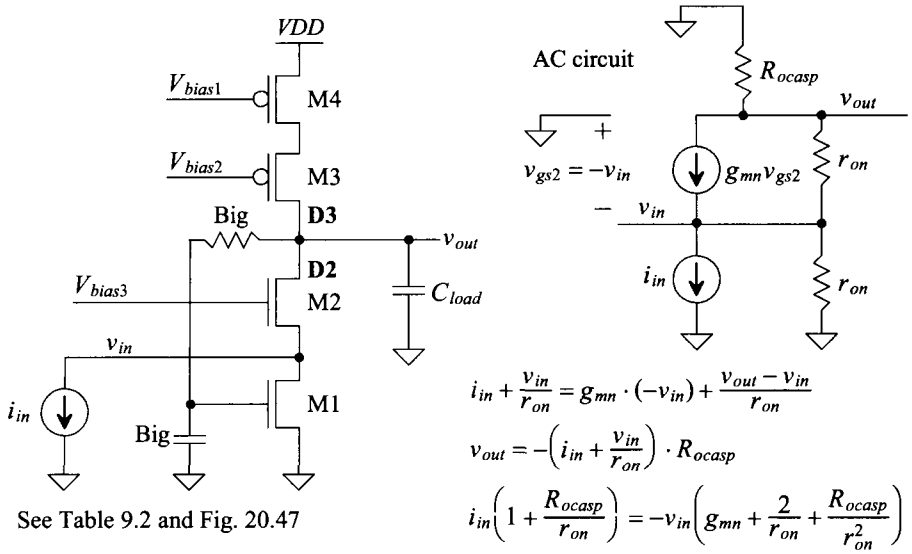


Figure 21.37 A transimpedance amplifier.

noting that if the drain of M2 is at AC ground or a low impedance then R_{in} is approximately $1/g_{mn}$. If $r_{on} \approx r_{op} \approx r_o$, $g_m = g_{mn} \approx g_{mp}$, and $R_{ocasp} \approx R_{ocasn} \approx g_m r_o^2$ then

$$R_{in} \approx \frac{\frac{R_{ocasp}}{r_{on}}}{2g_{mn}} \approx \frac{r_o}{2} \text{ and thus } v_{in} = -\frac{r_o}{2} \cdot i_{in} \tag{21.82}$$

To calculate the gain we can write

$$v_{out} = -\left(i_{in} + \frac{v_{in}}{r_{on}}\right) \cdot R_{ocasp} \rightarrow \frac{v_{out}}{i_{in}} = -\frac{R_{ocasp}}{2} \tag{21.83}$$

In terms of the NMOS and PMOS cascodes we can write

$$\frac{v_{out}}{i_{in}} = -g_{mn}r_{on}^2 \| g_{mp}r_{op}^2 = -R_{ocasn} \| R_{ocasp} \tag{21.84}$$

In other words the output voltage is simply the product of the input current with the cascode amplifier's output resistance.

21.2.3 The Common-Gate Amplifier

M2 in Fig. 21.37 is an example of a common-gate (CG) amplifier. We can redraw this circuit, as seen in Fig. 21.38 with a voltage source input, to show how the gate of the amplifying device, M2, is common to both the input and the output of the amplifier. Though the gate of M2 is at a DC voltage of V_{bias3}, we think of it as being at AC ground. M1 is simply an ordinary current source while M3 and M4 are a cascode current source load. The input resistance of this amplifier is given by Eq. (21.81); however, by connecting the input to a voltage source the output resistance and gain change. The voltage gain can be calculated by first writing

$$\frac{v_{out}}{R_{ocasp}} + g_{mn} \cdot (-v_{in}) + \frac{v_{out} - v_{in}}{r_{on}} = 0 \tag{21.85}$$

See Table 9.2 and Fig. 20.47

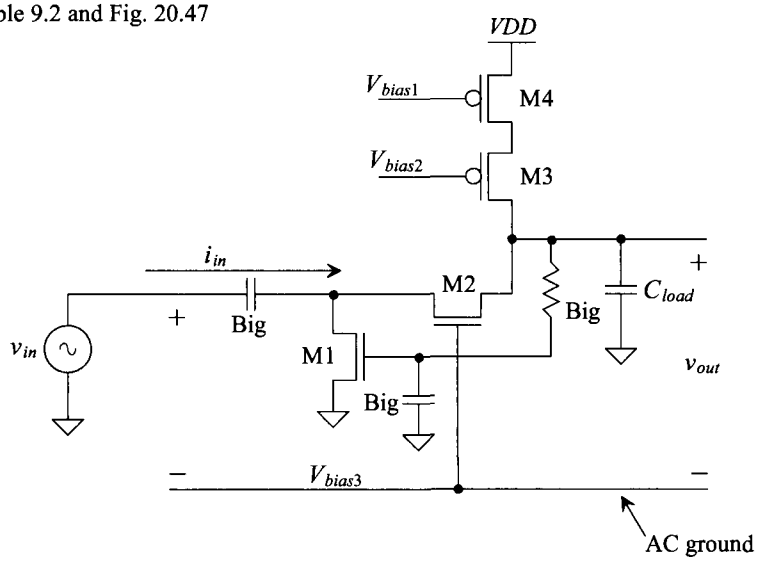


Figure 21.38 A common-gate amplifier.

or

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{mn} + \frac{1}{r_{on}}}{\frac{1}{R_{ocasp}} + \frac{1}{r_{on}}} = \frac{R_{ocasp} || r_{on}}{\frac{1}{g_{mn}} || r_{on}} \approx g_{mn} \cdot r_{on} \tag{21.86}$$

where, because the source of M2 is connected to a voltage source, the amplifier's output resistance is $R_{ocasp} || r_{on} \approx r_{on}$.

21.2.4 The Source Follower (Common-Drain Amplifier)

The source follower (SF) with current source load is seen in Fig. 21.39. Looking at the NMOS SF, we can write, for AC small signals,

$$v_{in} = v_{gs2} + v_{out} \tag{21.87}$$

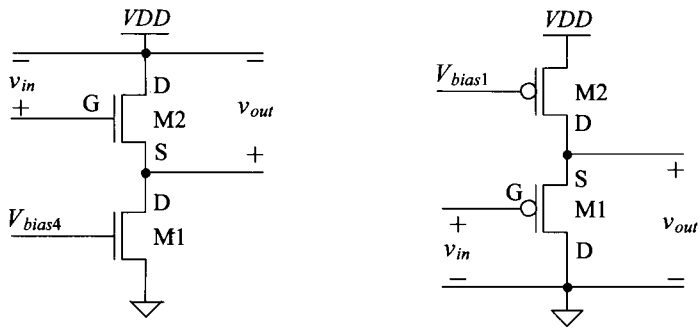


Figure 21.39 Source followers (common drain) using current source loads.

Knowing the resistance looking into the drain of M1 is r_o and the current that flows in M1 is i_d, we can write (neglecting M2's output resistance)

$$v_{out} = i_d \cdot r_o \text{ and } v_{gs2} = \frac{i_d}{g_{m2}} \tag{21.88}$$

Solving for the gain, we get

$$A_v = \frac{v_{out}}{v_{in}} = \frac{r_o}{r_o + 1/g_{m2}} = \frac{g_{m2} r_o}{g_{m2} r_o + 1} \tag{21.89}$$

If we use a current source for the load with a very large small-signal output resistance, the gain goes to one. (Limitations concerning the body effect will be discussed in a moment.) Looking at Eq. (21.89), we see that the gain is a voltage divider between the resistance looking into the source of a MOSFET ($1/g_m$) and the output resistance of the current source (here using the simple, single MOSFET r_o) as seen in Eq. (21.32).

Note that the maximum current the NMOS SF can sink is limited by the size of the current flowing in the current source load M1. The SF is a class A amplifier where, when discharging a load capacitance, the current through M1 limits the rate at which the capacitance can discharge (as indicated in Eq. [21.38]). M2 only sources current and M1 only sinks current. When the SF is sourcing a current, M2 provides the current to both the amplifier's output and to M1. When the SF is sinking a current, the current in M2 decreases while the current in M1 is constant (resulting in a net sinking of current on the amplifier's output). Finally, note that the maximum output voltage of an NMOS SF occurs when the gate of M2 goes to *VDD*. The maximum output voltage then goes to $VDD - V_{GS2}$. The minimum output voltage is set by the minimum voltage across the current source load (to keep the MOSFETs in the saturation region).

Body Effect and Gain

We might think, after looking at Eq. (21.89), that by using a cascode current source load for the source follower we can get an AC small-signal gain very close to unity. However, the body effect ultimately limits the gain of the amplifier. Figure 21.40 shows an SF with an ideal current source load. If we use the AC small-signal model seen in the figure where the output resistance, r_o, is infinite, we see that the AC output voltage, v_{out}, equals the AC source to bulk potential v_{sb}. Further, we can write

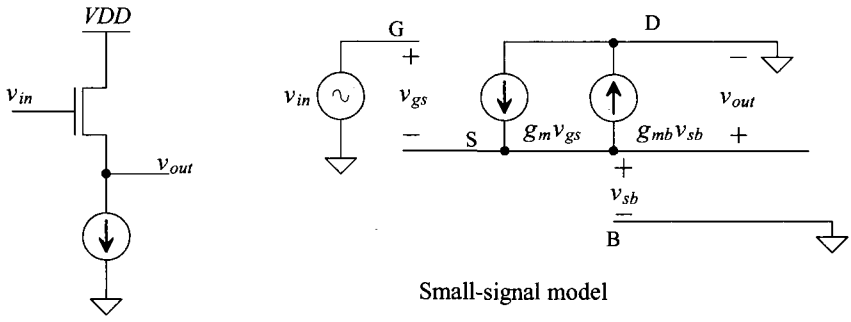


Figure 21.40 SF gain with body effect

$$v_{gs} = v_{in} - v_{out} \tag{21.90}$$

and, summing the currents at the output node,

$$g_m v_{gs} = g_{mb} v_{sb} = g_{mb} v_{out} \tag{21.91}$$

Solving for the gain of the SF with body effect and knowing $g_{mb} = \eta \cdot g_m$ (Eq. (9.28))

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{g_m + g_{mb}} = \frac{1}{1+\eta} \tag{21.92}$$

If $\eta = 0.25$, the gain is 0.8. The obvious way of eliminating the body effect (and thus move the gain closer to one) is to put the common-drain device in its own well, Fig. 21.41.

See Table 9.2 and Fig. 20.47

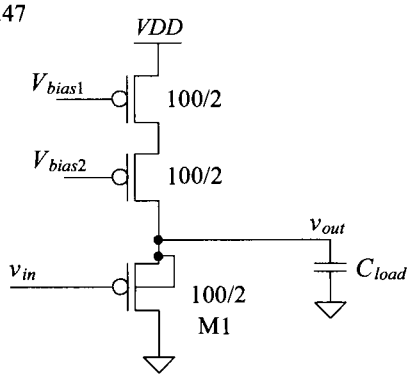


Figure 21.41 PMOS SF without body effect.

Level Shifting

One of the important uses of an SF is to provide a DC level shift to an input voltage. For example, M1 in Fig. 21.41 will remain in saturation as long as

$$v_{SD} = v_{OUT} \geq v_{SG} - V_{THP} = \overbrace{v_{OUT} - v_{IN}}^{v_{SG}} - V_{THP} \tag{21.93}$$

or

$$v_{IN} \geq -V_{THP} \tag{21.94}$$

As long as the input voltage is greater than $-V_{THP}$, M1 operates in the saturation region. This result is practically important. Note the output and input of the SF in Fig. 21.41 are related by

$$v_{OUT} = v_{IN} + V_{SG} \tag{21.95}$$

Using the parameters in Table 9.2 where *VDD* is 1 *V*, V_{SG} = 350 mV, and V_{THP} = 280 mV, the input voltage is shifted upwards, on the output of the amplifier, by 350 mV. The input signal can go down to –280 mV before M1 triodes. The minimum voltage across the current source, as seen in Fig. 20.48, is approximately 150 mV. This means that the range of the input signal is from *VDD* – 150 mV – 350 mV (= 500 mV = $V_{in,max}$) down to – 280 mV. Simulation results are seen in Fig. 21.42.

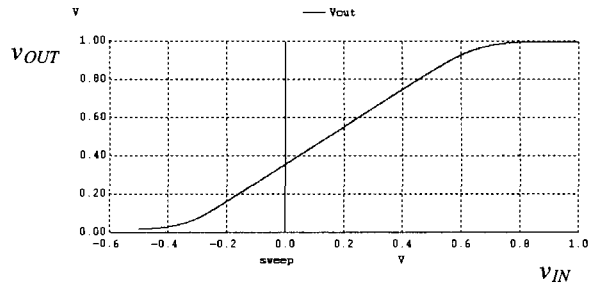


Figure 21.42 How the SF in Fig. 21.41 can shift negative input voltages upwards. This circuit is very useful when input signals are centered around ground.

Input Capacitance

Consider the partial schematic of an SF seen in Fig. 21.43. The capacitance on the input can be determined by looking at how much charge is supplied by the input source for an input voltage change Δv_{IN}

$$Q_{IN} = \Delta v_{IN} \cdot C_{dg} + (\Delta v_{IN} - A_v \cdot \Delta v_{IN}) \cdot C_{sg} \qquad (21.96)$$

where $A_v \leq 1$. The input capacitance of an SF is then

$$C_{IN} = \frac{Q_{IN}}{\Delta v_{IN}} = C_{dg} + C_{sg}(1 - A_v) \approx C_{dg} \qquad (21.97)$$

As the gain, A_v , of the SF approaches one, the input capacitance approaches the drain-gate capacitance of the MOSFET. In other words the source-gate capacitance doesn't affect the input capacitance (unlike the CS amplifier, which can have a very large input capacitance due to the Miller effect; see Ex. 21.6). Intuitively we can understand why C_{sg} doesn't affect the input capacitance by realizing that the displacement current through it is zero when the gate and source potentials move at the same rate. When the input voltage change and the output voltage changes are equal, the current through C_{sg} is zero. The SF is often used on the input of amplifiers that must have low input capacitance (like in charge-amplification applications). Unfortunately, the noise performance of the SF, because it doesn't have gain, is poorer than the CS or CG amplifiers.

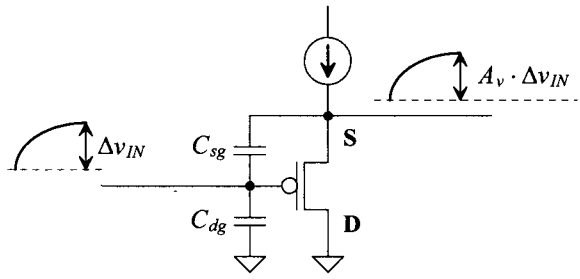


Figure 21.43 Input capacitance of a SF.

Noise Performance of the SF Amplifier

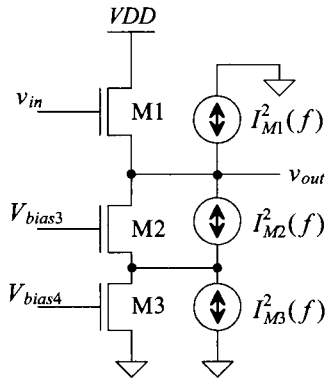
The SF amplifier with MOSFET noise sources is seen in Fig. 21.44. The noise current from M3 flows through M2 to the output node. The resistance on the output node (the output resistance of the SF) is the resistance looking into the source of M1 in parallel with the resistance looking into the drain of M2 or

$$R_{oSF} = \frac{1}{g_{m1}} || R_o \approx \frac{1}{g_{m1}} \tag{21.98}$$

The output noise power spectral density is

$$V_{onoise}^2(f) = \frac{I_{M1}^2(f) + I_{M3}^2(f)}{g_{m1}^2} \tag{21.99}$$

Noting that the SF's gain is close to one, the input-referred noise is nearly equal to the output noise PSD. Again, by using a large value of g_{m1}, we can minimize both the input-referred and output noise.



Neglect noise current from M2 since, $I_{M2}(f) + i_{D2} = 0$. The noise current that leaves the source must equal the noise current that enters the drain, that is, none of M2's noise current flows into the source of M1 and thus varies the output voltage.

Figure 21.44 Noise model of the source follower amplifier.

Frequency Behavior

Using Eq. (21.97), we see that if we drove the SF with an input whose source resistance was R_s, then we would have a pole associated with the input at

$$f_{in} = \frac{1}{2\pi \cdot R_s C_{dg}} \tag{21.100}$$

a very high frequency. On the output of the SF driving a capacitive load, we can write, using Eq. (21.98),

$$f_{out} = \frac{1}{2\pi \cdot R_{oSF} C_{load}} = \frac{g_{m1}}{2\pi C_{load}} \tag{21.101}$$

However, both Eqs. (21.100) and (21.101) assume that the transconductance doesn't vary with frequency. At very high frequencies, the input and output of the SF are shorted together through the gate-source capacitance. To calculate the variation of the transconductance with frequency, consider the circuit seen in Fig. 21.45. We can write

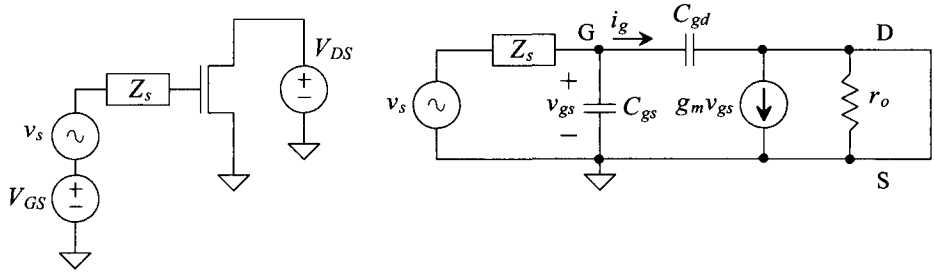


Figure 21.45 Determining the variation of the transconductance with frequency.

$$v_{gs}(f) = v_s \cdot \frac{\frac{1}{j\omega\cdot(C_{gs}+C_{gd})}}{\frac{1}{j\omega\cdot(C_{gs}+C_{gd})}+Z_s} = \frac{v_s}{1+Z_s\cdot j\omega\cdot(C_{gs}+C_{gd})} \tag{21.102}$$

and

$$i_d(f) = g_m \cdot v_{gs}(f) = \frac{g_m v_s}{1+Z_s\cdot j\omega\cdot(C_{gs}+C_{gd})} \tag{21.103}$$

The effective transconductance as a function of frequency is then

$$g_m(f) = \frac{g_m}{1+j\omega\cdot Z_s(C_{gs}+C_{gd})} \tag{21.104}$$

The impedance looking into the source of a MOSFET as a function of frequency is then

$$R_{\text{into source}} = \frac{1}{g_m(f)} = \frac{1}{g_m}\cdot(1+j\omega\cdot Z_s(C_{gs}+C_{gd})) \tag{21.105}$$

We note that at low frequencies the impedance is resistive and has a value of $1/g_m$. However, at higher frequencies and with a resistive source impedance, that is, $Z_s = R_s$, the impedance looking into the source appears to be the series connection of a resistor with a value of $1/g_m$ and an inductor of value

$$L_s = \frac{R_s(C_{gs}+C_{gd})}{g_m} \tag{21.106}$$

An SF driving a capacitive load can exhibit ringing because of the effective RLC circuit formed by its output impedance driving a load capacitance. If the impedance driving an SF is inductive (as we would have in the cascade of two SFs), the output impedance can become negative. For example, if $Z_s = j\omega L$, then substituting into Eq. (21.105), we get

$$R_{\text{into source}} = \frac{1}{g_m} - \omega^2\cdot L\cdot(C_{gs}+C_{gd}) \tag{21.107}$$

A battery or voltage source is an example of a circuit with a negative resistance (any source of power has a negative resistance). At higher frequencies the resistance looking into the source of the MOSFET becomes negative. This means that the circuit will oscillate or simply have a poor step response (the voltage across the capacitive load will ring). Often, to implement a microwave frequency oscillator using a MOSFET, an inductor is added from the gate of the MOSFET to AC ground to create the negative resistance.

SF as an Output Buffer

One of the common uses of an SF is as an output buffer. Connecting a resistive load to a high-impedance node kills the gain of a single-stage CMOS amplifier. A buffer amplifier is often inserted between the high-impedance node and the load resistance to keep the gain high. Consider the following example.

Example 21.13

Suppose that the cascode amplifier in Fig. 21.35, with R_s = 100k, must drive a 1 pF capacitor in parallel with a 10 kΩ resistor. Design an SF buffer to ensure that the 10 kΩ resistor doesn't kill the gain of the amplifier. Estimate the frequency response of the amplifier. Verify your design with SPICE simulations.

Looking at Eq. (21.76) and the associated discussion, we see that the output resistance of the cascode amplifier is in the megaohms region. Connecting a 10 kΩ load resistor on the amplifier's output would cause the cascode gain to drop from 500 to less than 1. The DC output voltage of the cascode amplifier in Fig. 21.35 is the V_{GS} of M1 (which, from Table 9.2 is 350 mV). If we use an NMOS SF, this DC voltage isn't enough to ensure that all of the MOSFETs in the SF operate in the saturation region. Looking at the NMOS SF in Fig. 21.39, a voltage of 350 mV on the gate of M2 would be just enough to turn it on but leave little voltage to drop across the current source M1. We'll use a PMOS source follower in this design. The schematic of the design is seen in Fig. 21.46. The current source (M5 and M6) in the SF must drive 1 V across the resistor of 10 kΩ (100 μA), so we've bumped up their size. Knowing, from Table 9.2, that when using the bias circuit in Fig. 20.47 a 100/2 PMOS conducts 10 μA of current, we increased the widths of M5–M7 so that they conduct 125 μA of current with the same bias voltages (the current source, M5/M6, sources 125 μA of current).

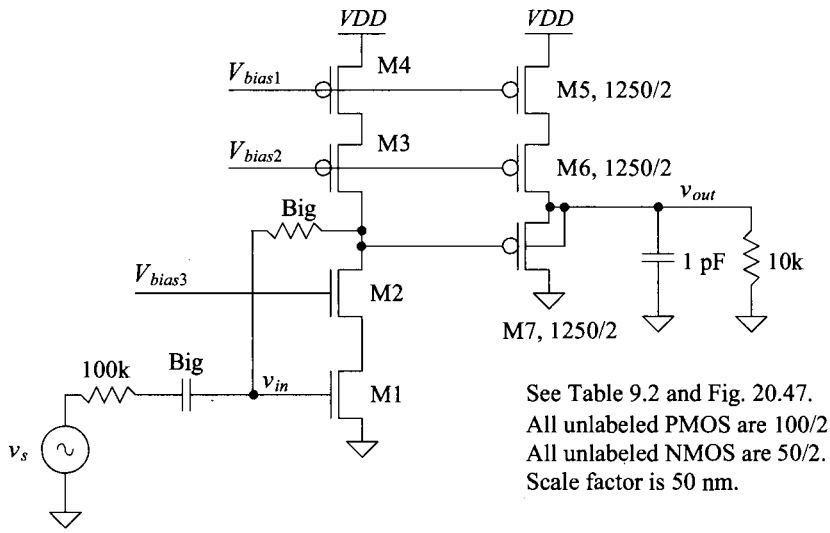


Figure 21.46 A cascode amplifier with SF output buffer.

The location of the input pole, f_{in} , is still (from Ex. 21.12) located at 218 MHz. The SF won't have much affect on the overall frequency response (because of its low input capacitance and small output resistance). However, now the cascode amplifier's load capacitance changes. Using the result in Eq. (21.97) and the data from Table 9.2, we can estimate the capacitance on the output of the cascode amplifier as the gate-drain capacitance of M7 ($3.7fF \cdot 12.5 \approx 50fF$). The factor of 12.5 comes from the increase in the PMOS's width by 12.5. Again, using the results from Ex. 21.12, the output pole, f_{out} , (output of the cascode amplifier) is at approximately 1 MHz (double what it was in Ex. 21.12).

The gain of the cascode amplifier is approximately 500. The transconductance of the wider PMOS devices is estimated using (see Eq. [9.22])

$$g_{m,wide} = K \cdot g_{m,Table\ 9.2} = 1.875\ mA/V \text{ where } K = 12.5 \quad (21.108)$$

The gain of the SF driving a resistive load, see Eq. (21.89), is

$$A_{v,SF} = \frac{R_{load}}{R_{load} + 1/g_{m,wide}} = \frac{10k}{10k + 533} = 0.95 \quad (21.109)$$

The overall gain from the input of the cascode amplifier to the output of the SF is then estimated as $500 \cdot 0.95 = 475 \rightarrow 53.5\ dB$. The simulation results are seen in Fig. 21.47. Note that the bandwidth of this amplifier can be increased by reducing the width of M7. This reduces the input capacitance of the SF output amplifier and thus pushes the pole location out to a higher frequency. ■

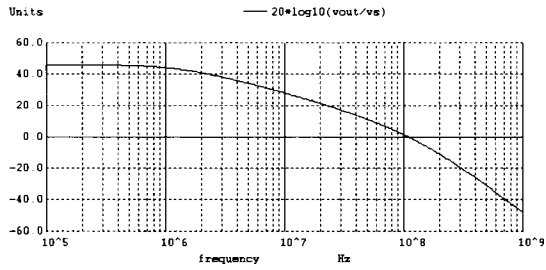


Figure 21.47 Simulating the operation of the amplifier in Fig. 21.46.

A Class AB Output Buffer Using SFs

In order to drive the 10k resistor in the previous example, we had to increase the size of the current source used in the SF. The practical problem with this approach is that as the load resistor gets small, the current source must source a significant current. The current source is sourcing this current all of the time (class A operation) either to the load or, if the load capacitance is being discharged, to the common-drain MOSFET (M7 in Fig. 21.46). What we need, for better drive capability, is for one side of the output buffer to shut off if the other side is supplying a large amount of current. For example, if, in Fig. 21.46, M7 starts to pull a large amount of current from the load, we would want M5 and M6 to turn off so that power wasn't wasted (class AB operation).

A class AB output buffer using SFs is seen in Fig. 21.48. The output buffer is comprised of M1–M4. M5 and M6 form a common-source amplifier with a current source load. When the circuit is in steady state, the AC input, v_{in}, is zero and the gate of M6 is at a DC potential of V_{bias1}. The current through M3 and M4 is mirrored by M1 and M2. This sets the DC current in M1/M2 to a known value (important). As v_{in} goes up, M6 shuts off. However, the current in M5 is constant, so the gates of M3 and M4 move towards ground. This turns M1 on and shuts M2 off (thus the class AB action). Similarly if v_{in} decreases, M6 turns on and pulls the gates of M3 and M4 up. The result is that M2 turns on and M1 shuts off.

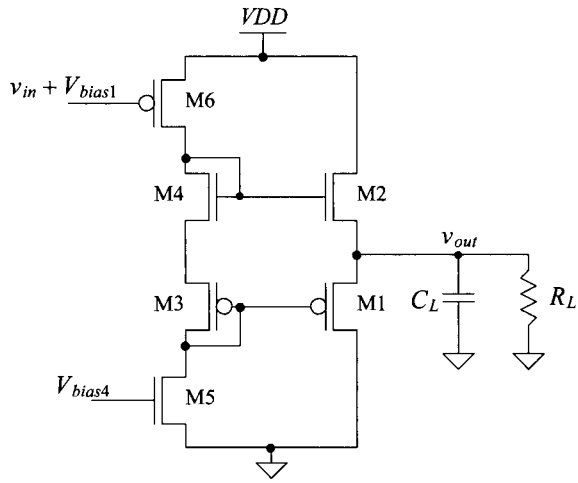


Figure 21.48 Class AB output buffer (M1–M4) using source followers M1 and M2.

The *practical problem* with this buffer is that the output can't swing very close to the power supply voltages (rails). The lowest potential we can get on the gate of M1 is ground, and the highest potential we can get on the gate of M2 is *VDD*. Knowing that M1 has to have a source-to-gate voltage greater than V_{THP} and M2 has to have a gate-source voltage greater than V_{THN}, we can write

$$VDD - V_{THN} \geq v_{out} \geq V_{THP} \tag{21.110}$$

For our short-channel CMOS process (neglecting body effect which will make things worse), the range of output voltages is half the power supply voltage. For example, with *VDD* = 1 V, our output voltage may swing up to (roughly) 750 mV and down to 250 mV. Losing half of the supply voltage often makes this output buffer impractical.

21.3 The Push-Pull Amplifier

What is needed for an output buffer is a topology like an inverter where the output can swing from rail (*VDD*) to rail (ground). Figure 21.49 shows a possible topology with biasing circuitry. The current source, I_{bias}, is a floating current source as seen in Fig. 20.49 of the last chapter. In Fig. 21.49, with zero AC input current, i_{in}, M1 and M2 mirror

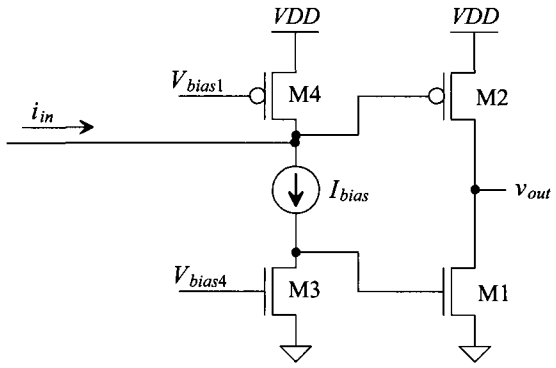


Figure 21.49 Class AB amplifier using an inverter output structure (push-pull).

the current in M3 and M4 (I_{bias}). This precisely sets the current in the output stage (again, important). A positive AC input current causes both the gates of M1 and M2 to go up (shutting M2 off and turning M1 on). M1 and M2 are pushing or pulling a current to/from the output (and so this topology is often called a *push-pull amplifier*). Because the output can swing very close to ground and *VDD* before M1 and M2 triode or shut off, this topology is very useful in modern CMOS output buffer design.

Note that the AC input current can be connected to the gate of M2, as shown in Fig. 21.49, or the gate of M1 (or both).

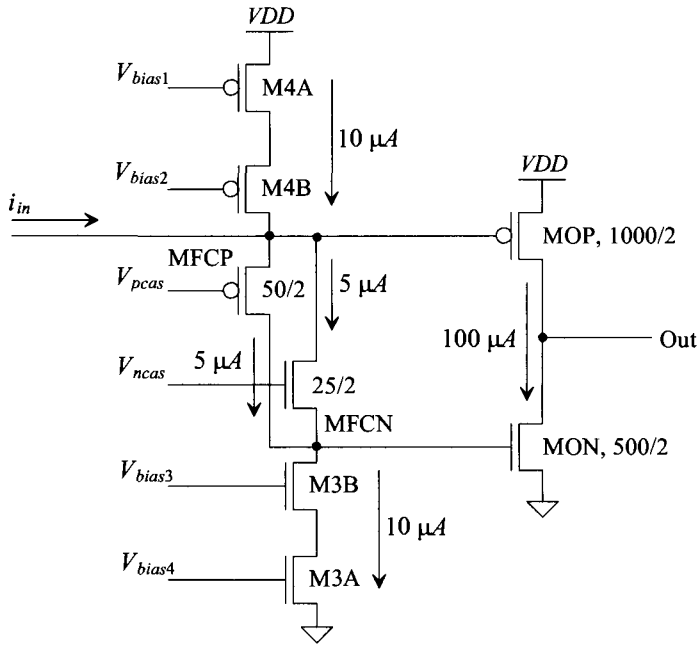
21.3.1 DC Operation and Biasing

The biasing of the push-pull amplifier can be accomplished, as seen in Fig. 21.50 (see also Fig. 20.49). MFCP and MFCN form the floating current source. M3 (A and B) with M4 (A and B) are cascode current sources. If the input current is positive, the gate of MOP is charged up and thus MOP shuts off. At the same time, MFCP turns on (more), causing the gate of MON to go up, turning it on further. If the input current is negative, MOP turns on and MON shuts off.

Figure 21.51 shows the amplifier in Fig. 21.50 with a voltage input (V_{bias4} replaced with an input voltage, V_{in}). M3 and M4 now form a common-source amplifier with a current source load. Shown in Fig. 21.51 is a plot of V_{out} for varying V_{in} with no load. The slope of the curve in this figure is the gain. To show the slope (the gain) as a function of V_{in}, we can take the derivative of the output voltage (also shown in the figure). The gain of this topology (without a load) is roughly 5,000 V/V. If we place a 1k resistor on the output of the amplifier, the gain drops to 1,500 V/V. Using a 100-ohm resistor results in a gain of only 150. The push-pull amplifier, MON/MOP, has a gain less than one when the load resistor is only 100 ohms. If the amplifier did need to drive such a heavy load (small resistance), it would be a good idea to increase the widths of MON and MOP.

Power Conversion Efficiency

The power conversion efficiency (PCE) is defined as the ratio of the power supplied to the load to the power delivered to the amplifier and load by a power supply. In other words, a perfectly efficient amplifier doesn't dissipate any power; rather, all of the power



Bias voltages come from Fig. 20.47 (short-channel parameters in Table 9.2). Unlabeled NMOS are 50/2, while unlabeled PMOS are 100/2.

Figure 21.50 Biasing the push-pull amplifier.

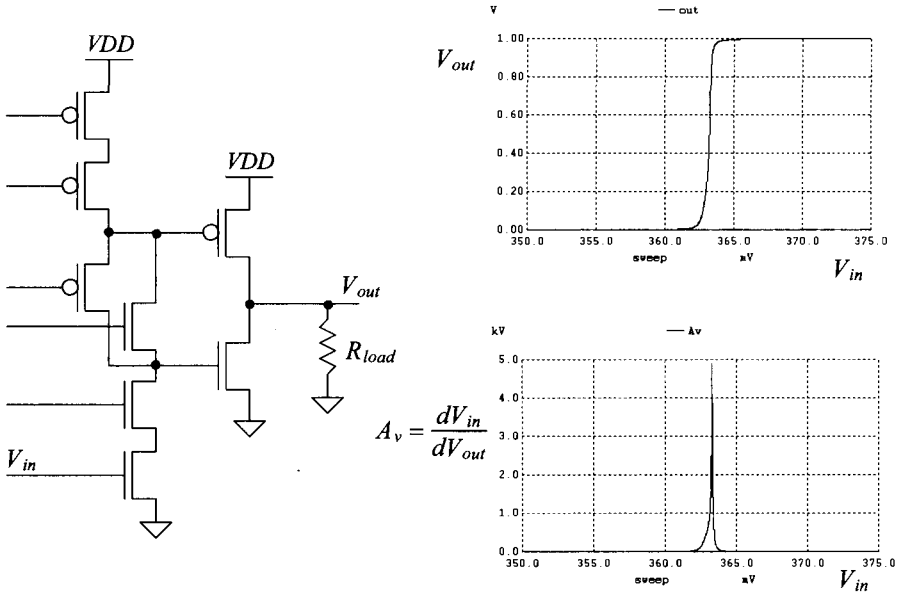


Figure 21.51 Simulating the amplifier in Fig. 21.50 with a voltage input.

from the power supply (*VDD*) is supplied to the load. The PCE is usually written as a percentage

$$\% \text{ PCE} = \frac{\text{Load power, } P_{load}}{\text{Supply power, } P_{supply}} \times 100\ \% \tag{21.111}$$

For example, the source follower seen in Fig. 21.41 (a class A amplifier) pulls a fixed current of I_{bias} (= 10 μA for the sizes seen in this figure and Table 9.2). The power supplied (pulled or delivered) from the power supply is

$$P_{supply} = VDD \cdot I_{bias} \tag{21.112}$$

If the SF is driving a resistive load, R_{load}, the peak value (under ideal conditions) of a sinewave voltage applied to this resistor is *VDD*/2 (the sinewave can go up or down by *VDD*/2). The RMS value of this sinewave is then $VDD/\left(2\sqrt{2}\right)$ and the power supplied to the load is then

$$P_{load} = \frac{\left(VDD/\left(2\sqrt{2}\right)\right)^2}{R_{load}} \tag{21.113}$$

The current source, I_{bias}, when the output voltage goes to *VDD*, drives the load resistor directly (M1 in Fig. 21.41 shuts off), that is

$$VDD = I_{bias} \cdot R_{load} \tag{21.114}$$

This is the best efficiency because no power is wasted in the amplifier (M1 is off and all of the supply power is delivered to the load). Calculating the PCE of the SF gives

$$\% \text{ PCE} = \frac{1}{VDD \cdot I_{bias}} \cdot \frac{\left(VDD/\left(2\sqrt{2}\right)\right)^2}{VDD/I_{bias}} \times 100\ \% \tag{21.115}$$

So the PCE % is, at best, 12.5%. This is the ideal efficiency of a class A amplifier. If the output voltage swing is reduced, the PCE goes down as well.

For the class AB amplifier, the PCE can approach 100%. (Typical values for general designs with low distortion are approximately 75%.) If the current supplied to the load is much larger than the current burned in the amplifier, the PCE is large (much larger than the ideal 12.5% of the class A amplifier). Consider the following example.

Example 21.14

Suppose the amplifier in Figs. 21.50 and 21.51 drives a 1 kΩ load. Using SPICE plot the current supplied to the amplifier and load, the current supplied to only the load, and the current supplied to only the amplifier as a function of the input voltage, V_{in}. Using the results estimate the PCE.

The simulation results are seen in Fig. 21.52. The current supplied to the amplifier includes the bias circuit current. Note how, when the output is 1 V (= *VDD*), the current supplied to the load is 1 mA. The total current supplied by *VDD* is approximately 1.2 mA. At the risk of stating the obvious, the push-pull amplifier is much more power-efficient than the SF (and has a wider output swing).

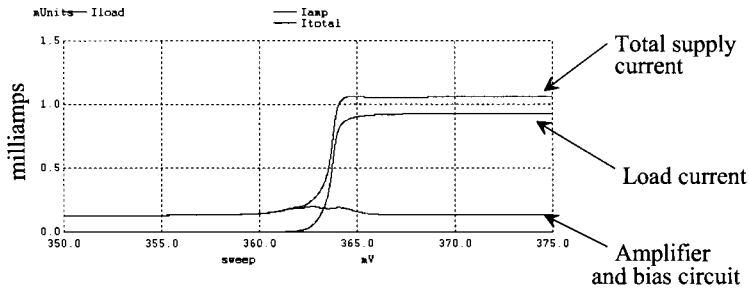


Figure 21.52 Supply, load, and total currents when the amplifier in Fig. 21.51 drives a 1k load resistor.

The PCE efficiency can be estimated by writing the power dissipated by the load

$$P_{load} = \left(\frac{VDD}{2\sqrt{2}}\right)^2 \cdot \frac{1}{R_{load}} = \left(\frac{1}{2\sqrt{2}}\right)^2 \cdot \frac{1}{1k} = 125\ \mu W$$

The power supplied by *VDD* (assuming the amplifier and bias circuit pull a constant 200 μA of current) is then

$$P_{supply} = P_{load} + VDD \cdot 200\ \mu A = 325\ \mu W$$

The PCE is then

$$\%\ \text{PCE} = \frac{125}{325} \times 100\% = 38\%$$

Note that the bias circuit pulls 140 μA. If we recalculate the PCE without the bias circuit current included, we get

$$\%\ \text{PCE} = \frac{125}{185} \times 100\% = 68\% \quad \blacksquare$$

21.3.2 Small-Signal Analysis

The simplified schematic of the push-pull amplifier is seen in Fig. 21.53. The resistance on the output of the amplifier (the drains of MOP and MON) is $r_{op} || r_{on} || R_{load} \approx R_{load}$. The drain current of MON is $g_{mon} v_{in}$ and the drain current of MOP is $-g_{mop} v_{in}$. The output voltage is then

$$v_{out} = -(g_{mon} + g_{mop}) \cdot v_{in} \cdot R_{load} \tag{21.116}$$

Note the "resistance in the source" in this amplifier is the parallel combination of the resistance looking into the sources of MON and MOP (both sources are connected to AC ground). We can rewrite Eq. (21.116) as

$$A_{v,push\text{-}pull} = \frac{v_{out}}{v_{in}} = -\frac{R_{load}}{\frac{1}{g_{mon}} || \frac{1}{g_{mop}}} \tag{21.117}$$

If the load resistance is 1k and the sum of the transconductances (using wider devices than what is indicated in Tables 9.1 or 9.2, as seen in Fig. 21.50) is 1 mA/V, then the gain of the push-pull amplifier is −1 V/V. Note that if the load resistance changes, the gain of the output stage push-pull amplifier changes as well.

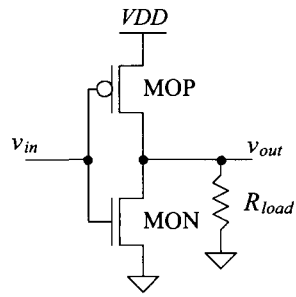


Figure 21.53 Small-signal analysis of the push-pull amplifier.

The gain of the CS amplifier with the cascode load portion of the amplifier in Figs. 21.50 and 21.51 (M3 and M4) is given by Eq. (21.76). The overall small-signal gain of the topology in Fig. 21.51 is given by the product of the two gains or

$$A_v = g_{mn} \cdot \left(g_{mn} r_{on}^2 \| g_{mp} r_{op}^2\right) \cdot (g_{mon} + g_{mop}) \cdot R_{load} \qquad (21.118)$$

We might wonder how the floating current source, MFCP and MFCN, affects the gain. If we look at Fig. 21.50, we see that one or the other has a source connection to the drains of either M3 (gate of MON) or M4 (gate of MOP). Further we might think that this source connection would load the gates with a $1/g_m$ small-signal resistance. However, because MFCP and MFCN form a feedback loop, their addition doesn't reduce the output resistance of the CS amplifier (M3 and M4). Consider the following.

Figure 21.54 shows a test circuit used for determining the small-signal resistance that the PMOS current source (M4) sees on its output. To determine this resistance, we apply a test voltage and look at the current that flows. Looking at the figure and noting the current that flows in $r_{on} \| r_{op}$ is $(i_t - i_{dn} - i_{dp})$, we can write

$$v_t = (i_t - i_{dn} - i_{dp}) \cdot r_{on} \| r_{op} + i_t \cdot R_{ncas} \qquad (21.119)$$

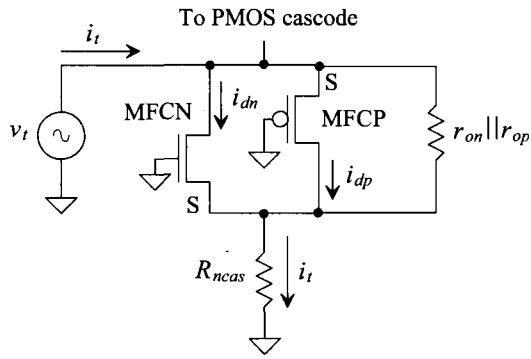


Figure 21.54 Determining the loading affects of the floating current source.

where R_{ncas} is the output resistance of the cascode stack. The gate-source AC voltage of MFCN is $-i_t R_{ncas}$ and so

$$i_{dn} = g_{mn} \cdot (-i_t R_{ncas}) \tag{21.120}$$

Similarly, the drain current through MFCP is

$$i_{dp} = g_{mp} \cdot v_t \tag{21.121}$$

Substituting these equations into Eq. (21.119) gives

$$v_t = (i_t + g_{mn} \cdot i_t R_{ncas} - g_{mp} \cdot v_t) \cdot r_{on} || r_{op} + i_t \cdot R_{ncas} \tag{21.122}$$

or

$$v_t \cdot \overbrace{(1 + g_{mp} \cdot r_{on} || r_{op})}^{\approx g_{mp} \cdot r_{on} || r_{op}} = i_t \cdot \overbrace{(1 + g_{mn} R_{ncas} \cdot r_{on} || r_{op} + R_{ncas})}^{\approx g_{mn} \cdot r_{on} || r_{op} \cdot R_{ncas}} \tag{21.123}$$

The resistance the PMOS cascode sees is then

$$\frac{v_t}{i_t} \approx R_{ncas} \tag{21.124}$$

In other words, the floating current source doesn't load the cascode structure.

21.3.3 Distortion

Small-signal analysis works remarkably well for all of the internal nodes in an op-amp. However, the output buffer must, ideally, swing from rail-to-rail. To illustrate the problem with this, consider the basic gain of a CS amplifier with current source load, Eq. (21.39),

$$|A_v| = g_{m1} \cdot (r_{o1} || r_{o2}) = \frac{\sqrt{2\beta_1 (I_D + i_d)}}{2(\lambda_n + \lambda_p)(I_D + i_d)} \approx \frac{\sqrt{2\beta_1}}{2(\lambda_n + \lambda_p)\sqrt{(I_D + i_d)}} \tag{21.125}$$

Normally, the AC component of the drain current, i_d, is assumed to be much less than the DC component of the drain current, I_D, and the amplifier gain is essentially constant (small-signal approximation). If the AC component is comparable to the DC component, noticeable distortion results. The voltage gain for large inputs depends on the input signal amplitude.

Characterizing an amplifier begins by applying a pure single-tone sinusoid of the form

$$V_{in}(t) = V_p \sin 2\pi f \cdot t \tag{21.126}$$

to the input of the amplifier. The output of the amplifier is a series of tones at an integer multiple of the input tone given by

$$V_{out}(t) = a_1 V_p \sin(\omega t) + a_2 V_p \sin(2\omega t) + \cdots + a_n V_p \sin(n\omega t) \tag{21.127}$$

The magnitude of the fundamental or wanted signal is $a_1 V_p$. Ideally, a_2 through a_n are zero, and the amplifier is free of distortion. The n^{th} term harmonic distortion is given by

$$HD_n = \frac{a_n}{a_1}, \text{ for } n > 1 \tag{21.128}$$

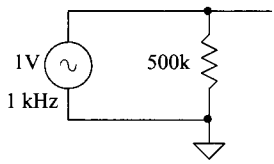
The *total harmonic distortion* (THD) is given by

$$THD = \sqrt{\frac{a_2^2 + a_3^2 + a_4^2 + \cdots + a_n^2}{a_1^2}} \tag{21.129}$$

Again, output buffers, amplifiers used to drive a large load capacitance or low resistance, are examples of amplifiers where low THD is important. If the output amplifier is biased so that the DC component of the drain current is large compared to the transient or time-varying current, the buffer will dissipate too much power for most applications. Therefore, in almost all situations, the biasing current in an output buffer is comparable, or even smaller for class B operation, than the time-varying current. We reduce the distortion by employing feedback around the amplifier. If the open-loop gain of an op-amp varies from 1,000 to 10,000 depending on the amplitude of the input signal, then the feedback around the amplifier reduces the gain sensitivity. In fact, it is nearly impossible to design a linear output amplifier with low distortion without using feedback.

Modeling Distortion with SPICE

SPICE can be used to simulate distortion using a transient analysis and the .FOUR (Fourier) statement. The general form of this statement is .FOUR FREQ OV1 <OV2 OV1 . . . where FREQ is the frequency of the fundamental and OV1 . . . are the outputs of the circuit (the voltage or current outputs for which SPICE will calculate distortion). As a simple example, consider the circuit and netlist shown in Fig. 21.55. The input sine wave must have at least one full period for the .FOUR statement to calculate distortion. In the case where there's more than one period, SPICE uses the output over the last full period. Also, the maximum transient step size should be less than the period of the input divided by 100. For the example of Fig. 21.55 with a 1 kHz input (a period of 1 ms), the maximum print size should be 10 μs.




```
*** SPICE Fourier Analysis Example ***
.four 1k Vinout
R1 Vinout 0 500k
Vinout Vinout 0 DC 0 AC 0 0 SIN(0 1 1khz 0 0)
.tran 10u 2m 0 10u
.end
```

Figure 21.55 Simple circuit to demonstrate the use of the .FOUR statement.

The resulting simulation output follows.

```
Fourier analysis for vinout:
  No. Harmonics: 10, THD: 3.17012e-06 %, Gridsize: 200, Interpolation Degree: 1

Harmonic  Frequency     Magnitude     Phase         Norm. Mag     Norm. Phase
--------  ------------  ------------  ------------  ------------  ------------
0         0.000000e+00  -5.60197e-09  0.000000e+00  0.000000e+00  0.000000e+00
1         1.000000e+03  9.996317e-01  -9.39744e-06  1.000000e+00  0.000000e+00
2         2.000000e+03  1.120393e-08  -8.64000e+01  1.120806e-08  -8.64000e+01
3         3.000000e+03  1.120393e-08  -8.46000e+01  1.120806e-08  -8.46000e+01
4         4.000000e+03  1.120394e-08  -8.28000e+01  1.120806e-08  -8.28000e+01
5         5.000000e+03  1.120394e-08  -8.10000e+01  1.120806e-08  -8.10000e+01
6         6.000000e+03  1.120394e-08  -7.92000e+01  1.120806e-08  -7.92000e+01
```

```
7    7.000000e+03    1.120393e-08  -7.74000e+01    1.120806e-08  -7.74000e+01
8    8.000000e+03    1.120393e-08  -7.56000e+01    1.120806e-08  -7.56000e+01
9    9.000000e+03    1.120393e-08  -7.38000e+01    1.120806e-08  -7.38000e+01
```

Notice that, as we would expect, the output of this circuit doesn't show any harmonic distortion. SPICE calculates the magnitude and phase of the first nine harmonics and DC. Also note that SPICE automatically calculates the THD for a circuit.

As a more practical example, consider the push-pull amplifier shown in Fig. 21.56. The SPICE netlist for simulating the distortion performance of this output amplifier is shown below. Note that to avoid a long start-up transient we started the big capacitors at the DC bias voltages (V_{bias1} for the PMOS and V_{bias4} for the NMOS). When the input sinewave has an amplitude of 2 mV, the THD is 0.6%. When the input drops to 100 μV (small-signal approximation is more valid), the THD drops to 0.046%. If the input amplitude increases to 10 mV (so the output of the push-pull amplifier swings close to the rails), the THD increases to 9.2%.

```
*** Figure 21.56 CMOS: Circuit Design, Layout, and Simulation ***

.option scale=50n
.tran 10n 2u UIC
.four 1MEG Vout
VDD   VDD    0      DC    1
Vin   Vin    0      DC    0      sin 0 2m 1MEG
RL    out    0      1k
Rbigp Vbias1 vgp    1G
Cbigp vgp    vin    1 IC=0.643
Rbign Vout   vgn    1G
Cbign Vgn    vin    1 IC=0.362
Xbias VDD Vbias1 Vbias2 Vbias3 Vbias4 Vhigh Vlow Vncas Vpcas bias
MON   Vout   vgn    0      0      NMOS L=2 W=500
MOP   Vout   vgp    VDD    VDD    PMOS L=2 W=1000
(subcircuit and SPICE models not shown)
```

Note that another useful SPICE tool to evaluate the distortion introduced into a signal by a circuit is a Discrete Fourier Transform (DFT). The spec command is used in SPICE (spectral analysis) to determine the output spectrum of an amplifier. Using this command is covered in depth in the book entitled, *CMOS Mixed Signal Circuit Design.*

Bias circuit from Fig. 20.47 (Table 9.2).

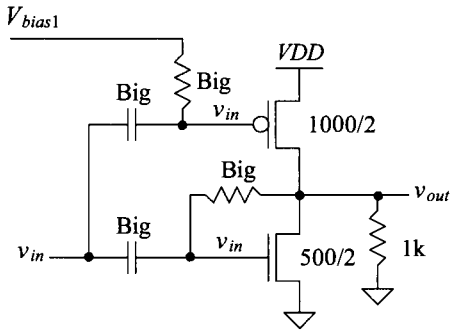


Figure 21.56 Simulating the distortion in a push-pull amplifier.

ADDITIONAL READING

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PROBLEMS

21.1 Using simulations, show that the small-signal resistance of a gate-drain-connected PMOS device, Fig. 21.57, behaves like a resistor with a value of $1/g_m$.

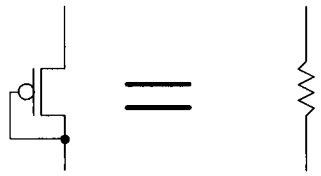
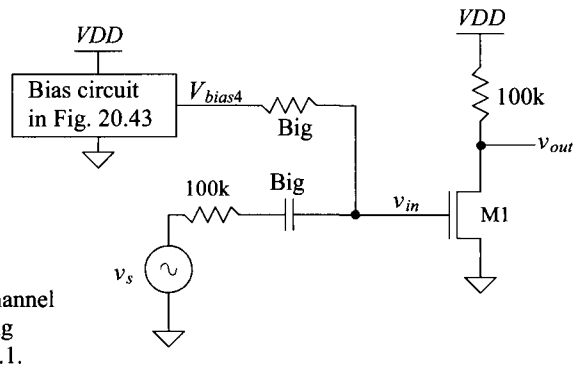


Figure 21.57 The small-signal behavior of a diode-connected MOSFET.

21.2 Estimate the frequency response of the circuit seen in Fig. 21.58. Verify your hand calculations using SPICE.



Use the long-channel sizes and biasing seen in Table 9.1.

Figure 21.58 Amplifier used in Problem 21.2.

21.3 Repeat problem 21.2 if the amplifier drives a 100 *fF* load capacitance.

21.4 For the circuit in Fig. 21.12, estimate the effective transconductance of the circuit, g_{meff}, that relates the MOSFET drain current to the AC input voltage, v_{in}. Verify your solution with SPICE.

21.5 Simulate the operation of the common-gate amplifier in Fig. 21.16 using the bias circuit in Fig. 20.43 and the device sizes seen in Table 9.1. Compare the simulation results to hand calculations.

21.6 Estimate the transfer function of the amplifier in Ex. 21.6 if it drives a 100 fF load. Verify your hand calculations using simulations.

21.7 Determine the frequency response of the amplifier seen in Fig. 21.59. Verify your hand calculations using simulations.

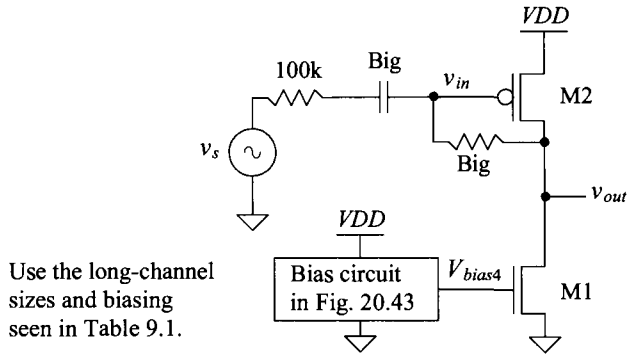


Figure 21.59 Amplifier for Problem 21.7.

21.8 Repeat Ex. 21.9 using the biasing circuit from Fig. 20.47 and the sizes in Table 9.2.

21.9 Repeat Ex. 21.10 using the biasing circuit from Fig. 20.47 and the sizes in Table 9.2.

21.10 Repeat Ex. 21.12 using the biasing circuit from Fig. 20.43 and the sizes in Table 9.1.

21.11 Show, using SPICE simulations and an ideal current source of 10 μA (device size from Table 9.2), the difference in the voltage gains with and without body effect for the circuit seen in Fig. 21.60.

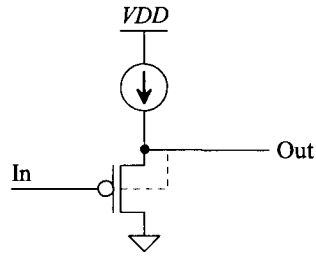


Figure 21.60 Gain of an SF with and without body effect for Problem 21.11.

21.12 Does the SF in Fig. 21.46 exhibit slew-rate limitations if it needs to discharge the 1-pF load capacitance quickly? Why or why not? Verify your answer using simulations.

21.13 Simulate the operation of the class AB output buffer in Fig. 21.48 using the bias circuit from Fig. 20.47 and the sizes in Table 9.2. If the buffer is driving a load resistor of 10k, plot v_{in} against v_{out}. What is the linear output range?

21.14 In the class AB output buffer in Fig. 21.50 or 21.51, a load resistor connected to ground causes the PMOS device to conduct more current then the NMOS. Why? Resimulate the buffer in Fig. 21.51 if it drives a 1k resistor and MON is reduced in size to 50/2. Is this a better design? Why or why not?

21.15 Using simulations, show the problem of using an inverter output buffer without a floating current source as seen in Fig. 21.53. (The quiescent current that flows in the MOSFETs is huge and not accurately controlled as it is in Fig. 21.50.)

21.16 Is the distortion the output buffer in Fig. 21.56 introduces into a signal a function of the load resistance? Verify your answer with simulations and show some time-domain waveforms with and without distortion.