Chapter
22

Differential Amplifiers

In the last chapter big resistors and capacitors were used to bias the circuits to the correct operating point, as seen in Fig. 21.21. The DC operating voltage on the gate of M1 (in Figs. 21.17 or 21.21) is extremely important when biasing the amplifier. If it's not at precisely the correct value, then the current sourced by M2 won't equal the current in M1 when both MOSFETs are operating in the saturation region.

The differential amplifier (*diff-amp*) is used on the input of an amplifier to allow input voltages to move around so that biasing of the gain stages isn't affected (that is, so it isn't a function of the input voltage). The diff-amp is a fundamental building block in CMOS analog integrated circuit design, and an understanding of its operation and design is extremely important. In this chapter we discuss three basic types of differential amplifiers: the source-coupled pair, the source cross-coupled pair, and the current differential amplifier.

22.1 The Source-Coupled Pair

The source-coupled pair comprised of M1 and M2 is shown in Fig. 22.1. When M1 and M2 are used in this configuration they are sometimes called a *diff-pair*.

22.1.1 DC Operation

The diff-pair in Fig. 22.1 is biased with a current source so that

$$I_{SS} = i_{D1} + i_{D2} \tag{22.1}$$

If we label the input voltages at the gates of M1 and M2 as v_{I1} and v_{I2}, we can write the input difference as

$$v_{DI} = v_{I1} - v_{I2} = v_{GS1} - v_{GS2} \tag{22.2}$$

or in terms of the AC and DC components of the differential input voltage, v_{DI},

$$v_{DI} = V_{GS1} + v_{gs1} - V_{GS2} - v_{gs2} \tag{22.3}$$

When the gate potentials of M1 and M2 are equal, then (assuming both are operating in the saturation region)

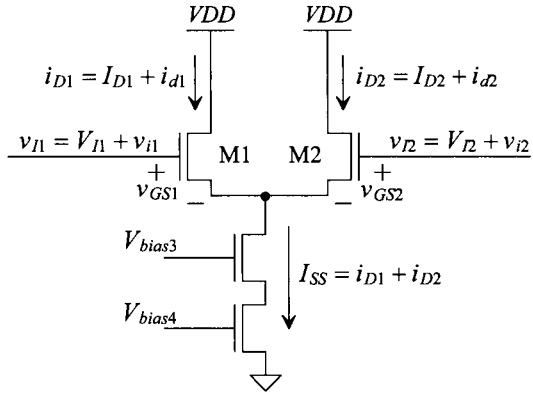


Figure 22.1 A basic NMOS source-connected pair made using the diff-pair M1 and M2.

$$I_{D1} = I_{D2} = \frac{I_{SS}}{2} \tag{22.4}$$

Maximum and Minimum Differential Input Voltage

Since we know that a saturated MOSFET follows the relation

$$i_D = \frac{\beta_n}{2}(v_{GS} - V_{THN})^2 \tag{22.5}$$

the difference in the input voltages may be written as

$$v_{DI} = \sqrt{\frac{2}{\beta_n}}\left(\sqrt{i_{D1}} - \sqrt{i_{D2}}\right) \tag{22.6}$$

The maximum difference in the input voltages, v_{DIMAX} (maximum differential input voltage), is found by setting i_{D1} to I_{SS} (M1 conducting all of the tail bias current) and i_{D2} to 0 (M2 off)

$$v_{DIMAX} < v_{I1} - v_{I2} = \sqrt{\frac{2 \cdot L \cdot I_{SS}}{KP_n \cdot W}} \tag{22.7}$$

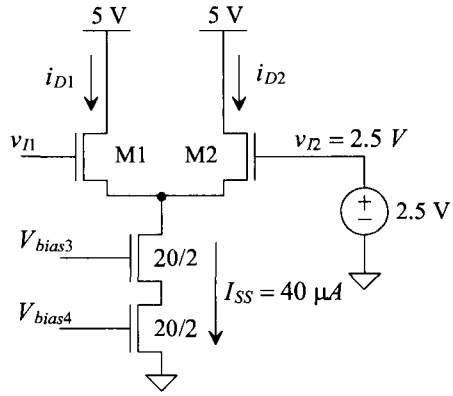
The minimum differential input voltage, v_{DIMIN}, is found by setting i_{D2} to I_{SS} and i_{D1} to 0

$$v_{DIMIN} = -v_{DIMAX} = -(v_{I1} - v_{I2}) = -\sqrt{\frac{2 \cdot L \cdot I_{SS}}{KP_n \cdot W}} \tag{22.8}$$

Example 22.1

Estimate the maximum and minimum voltage on the gate of M1 in Fig. 22.2 that ensures that neither M1 or M2 shut off. Verify your hand calculations with SPICE simulations.

Note that the diff-amp tail current, I_{SS}, is 40 μA (the widths of the MOSFETs were doubled from the sizes indicated in Table 9.1). When $v_{I1} = v_{I2} = 2.5$ V, the differential input voltage, v_{DI}, is 0 and the current flowing in M1 and M2 is 20 μA ($= i_{D1} = i_{D2}$).



Parameters from Table 9.1
Bias circuit from Fig. 20.43

Figure 22.2 Diff-amp used in Ex. 22.1.

Using Eq. (22.7), we can estimate the maximum voltage on the gate of M1 as

$$v_{I1MAX} = \sqrt{\frac{2 \cdot L \cdot I_{SS}}{KP_n \cdot W}} + v_{I2} = \sqrt{\frac{2 \cdot 2 \cdot 40}{120 \cdot 10}} + 2.5 = 2.865\ V$$

or v_{I1} is 365 mV above v_{I2}. The minimum voltage allowed on the gate of M1 (to keep some current flowing in M1) is then 365 mV below v_{I2} or 2.135 V. The simulation results are seen in Fig. 22.3. Notice how, when the inputs are equal (both are 2.5 V), the currents in M1 and M2 are equal and approximately 20 μA ($= I_{SS}/2$). ■

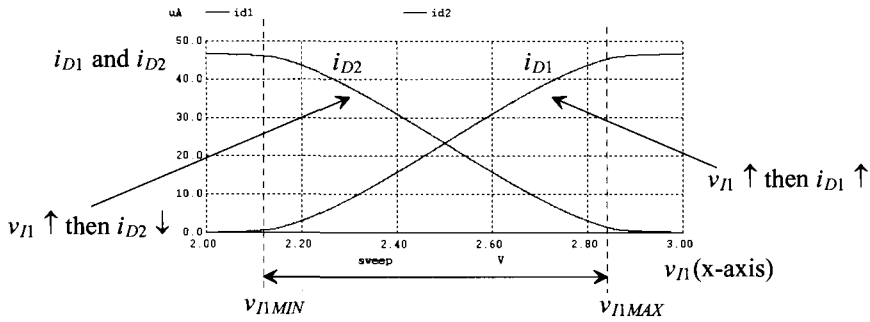


Figure 22.3 Simulating the operation of the diff-amp in Fig. 22.2.

Maximum and Minimum Common-Mode Input Voltage

When the diff-amp is used on the input of an op-amp, the inputs are forced, via feedback around the op-amp, to the same values (or very nearly the same values). This value (or more precisely the average of the two inputs) is called the *common-mode voltage*. Figure 22.4 shows the diff-amp with both inputs tied together. We're interested in the maximum and minimum voltage that will keep both M1 and M2 operating in the saturation region

(that is, not off or in the triode region). We'll call the maximum common-mode voltage, v_{CMMAX} and the minimum common-mode voltage, v_{CMMIN}. Note that when the common-mode voltage (the potential on the gates of M1 and M2) is too high, both M1 and M2 triode (behave like resistors). When the common-mode voltage is too low, M1 and M2 shut off.

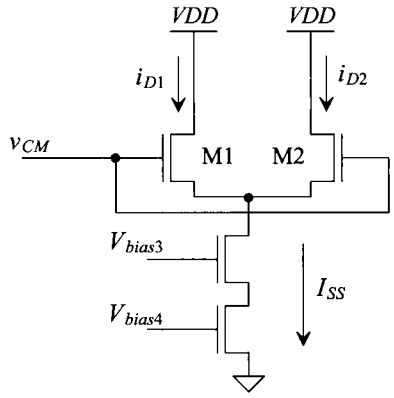


Figure 22.4 Diff-amp used to calculate the minimum and maximum diff-amp input voltages.

To determine the maximum input voltage, we know that for M1 and M2 to remain in the saturation region

$$V_{DS} \geq V_{GS} - V_{THN} \rightarrow V_D \geq V_G - V_{THN} \tag{22.9}$$

Because $V_D = VDD$, we can write

$$V_{CMMAX} = VDD + V_{THN} \tag{22.10}$$

The input common-mode voltage can actually be higher than VDD before M1/M2 move into the triode region.

For the minimum input voltage, we can write

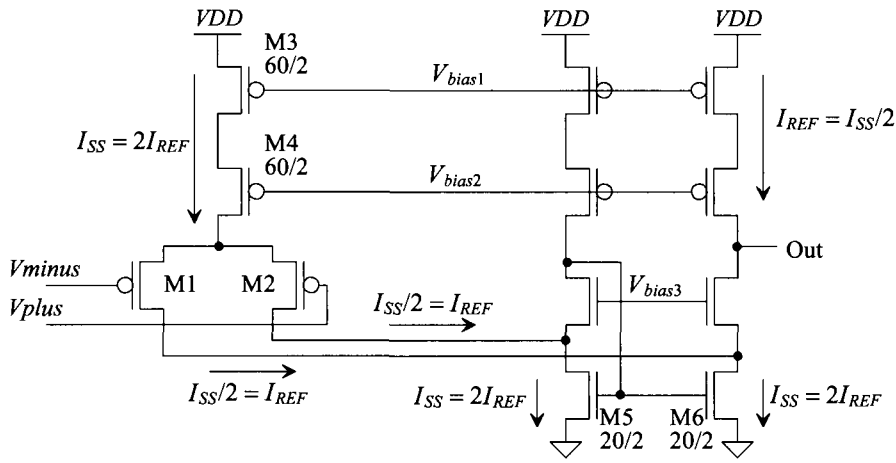
$$V_{CMMIN} = V_{GS1,2} + 2 \cdot V_{DS,sat} \tag{22.11}$$

where the minimum voltage across the current source is assumed to be $2V_{DS,sat}$. For the long-channel process, from Table 9.1, the minimum input voltage for an NMOS diff-amp is 1.55 V.

Example 22.2

Figure 22.5 shows a folded cascode amplifier (see Fig. 20.45). Assuming that all MOSFETs are operating in the saturation region, estimate the minimum and maximum input voltage of the amplifier.

Note how the widths of M5–M6 are doubled to sink the additional current from the diff-amp. It's important to understand how the sizes of the MOSFETs are adjusted in the current mirrors so that the currents sum correctly. The currents, as seen in Fig. 22.5, are labeled assuming *Vplus* = *Vminus*.



Parameters from Table 9.1
Unlabeled PMOS are 30/2
Unlabeled NMOS are 10/2
Bias circuit from Fig. 20.43

Figure 22.5 Folded cascode amplifier.

The maximum allowable input common-mode voltage is determined by

$$V_{CMMAX} = VDD - V_{SG} - 2V_{SD,sat} = 5 - 1.15 - 0.5 = 3.35\ V$$

The minimum input common-mode voltage is determined by noting the drain voltage of M5 and M6 (or M1 and M2) is a $V_{DS,sat}$

$$V_{SD} \geq V_{SG} - V_{THP} \rightarrow V_D \leq V_G + V_{THP}$$

and so

$$V_{CMMIN} = V_D - V_{THP} = 0.25 - 0.9 = -0.65$$

In other words, the input common-mode voltage can actually be below ground and the amplifier will still function correctly. This result is *very useful.* The folded-cascode amplifier with PMOS diff-amp can be used when the input voltage swings around ground. Note, however, that the output voltage of the amplifier will not swing below ground but is, rather, limited to $2V_{DS,sat}$ above ground and $2V_{SD,sat}$ below *VDD* if the MOSFETs are to remain in saturation (the high-gain region of operation). ■

Current Mirror Load

The previous uses of the diff-amp have exploited the fact that the output of the diff-amp is a current controlled by a differential input voltage, v_{Df}. In some applications, it is desirable to have a diff-amp with a voltage output. Towards this goal, consider the diff-amp with a current mirror load, as seen in Fig. 22.6. An imbalance in the drain currents of M1 and M2 causes the output of the diff-amp to swing either towards *VDD* or

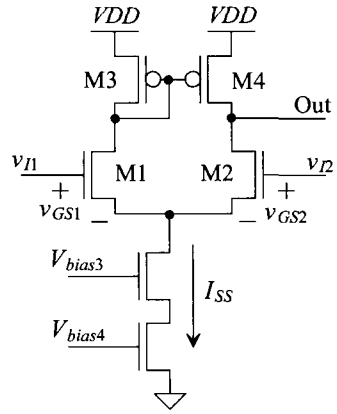


Figure 22.6 Diff-amp with a current mirror load.

ground. The minimum input common mode voltage is, once again, given by Eq. 22.11. The maximum input common mode voltage is determined knowing that the drain voltage of M2 is the same as the drain voltage of M1 (when both diff-amp inputs are the same potential), that is, $VDD-V_{SG}$ of the PMOS. We can therefore write

$$V_{DS} \geq V_{GS} - V_{THN} \rightarrow V_D \geq V_G - V_{THN} \rightarrow V_{CMMAX} = VDD - V_{SG} + V_{THN} \quad (22.12)$$

For the parameters in Table 9.1, $V_{CMMAX} = 5 - 1.15 + 0.8 = 4.65\ V$.

The voltage output swing can be determined by noting that the maximum voltage output is limited by keeping M4 in saturation. Therefore,

$$V_{OUTMAX} = VDD - V_{SD,sat} \quad (22.13)$$

The minimum output voltage is determined by the voltage on the gate of M2 (M2 must remain in saturation).

$$V_D \geq V_G - V_{THN} \rightarrow V_{OUTMIN} = V_{I2} - V_{THN} \quad (22.14)$$

Example 22.3

Suppose the diff-amp in Fig. 22.6 is implemented with the sizes and bias currents seen in Table 9.1 (I_{SS} = 40 μA). If the gate of M2 is held at 4 V, estimate the diff-amp's output swing. Verify the answers with SPICE.

From Eq. (22.13), the output can swing up to 4.75 V before M4 triodes. From Eq. (22.14), the output can swing down to 4–0.8 or 3.2 V before M2 triodes. The simulation results are seen in Fig. 22.7. Looking at the results, we see the output goes down to approximately 2.8 V or 400 mV less than what we predicted. This can be attributed to the body effect in M1 and M2. With body effect, the threshold voltage is 1.2 V (instead of 0.8 V). ■

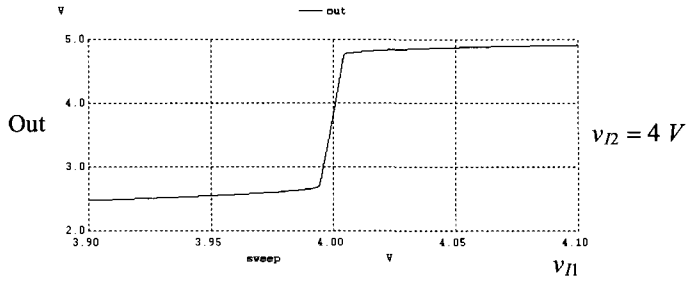


Figure 22.7 Simulation results for Ex. 22.3

Biasing from the Current Mirror Load

Consider the connection of the common-source amplifier, M7, to the output of the diff-amp in Fig. 22.8. When the inputs to the diff-amp are at the same potential, the currents that flow in M3 and M4 are equal (= $I_{SS}/2$). We know from Ch. 20 that the drain of M4 is then at the same potential as its gate. This means, for biasing purposes, that the gate of M7 can be treated as if it were tied to the gate of M3 (M4).

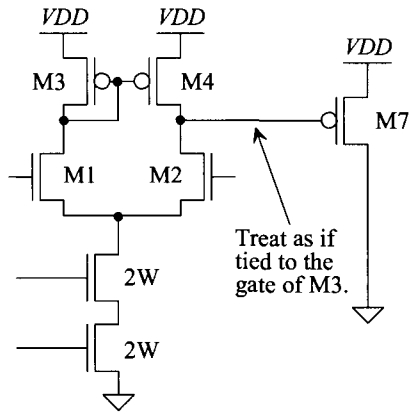


Figure 22.8 Using a diff-amp to bias the next stage amplifier.

Minimum Power Supply Voltage

Looking at the diff-amp in Fig. 22.6, we can estimate the minimum allowable power supply voltage, VDD_{min}, as

$$VDD_{\min} = V_{SG3} + \overbrace{V_{DS,sat1}}^{\text{minimum voltage across M1}} + \overbrace{2V_{DS,sat}}^{\text{minimum voltage across Iss}} \qquad (22.15)$$

Looking at this equation, we see that the V_{SG} of M3 is the "weak link" in the minimum power supply voltage. Using the parameters from Table 9.2 (the short-channel devices with a *VDD* of 1 V), we get a VDD_{min} of 500 mV. We can lower this value by using a single MOSFET to bias the diff-amp (instead of a cascode circuit).

22.1.2 AC Operation

To describe the AC small-signal operation of the diff-amp in Fig. 22.1, consider the AC schematic seen in Fig. 22.9. We've replaced the current source with an open and the DC supply (*VDD*) with a short (to ground). In the following discussion, it's important to remember that a negative AC current simply means that the overall current (AC + DC) is decreasing (see Ex. 9.5 in Ch. 9). We can write

$$v_{di} = v_{i1} - v_{i2} = v_{gs1} - v_{gs2} = \frac{i_{d1}}{g_m} - \frac{i_{d2}}{g_m} \tag{22.16}$$

Reviewing Fig. 22.9, we see that

$$i_{d1} = -i_{d2} = i_d \tag{22.17}$$

and thus

$$v_{gs1} = -v_{gs2} = \frac{v_{di}}{2} \tag{22.18}$$

so finally

$$g_m v_{gs1} = g_m(-v_{gs2}) = i_d = g_m \cdot \frac{v_{di}}{2} \tag{22.19}$$

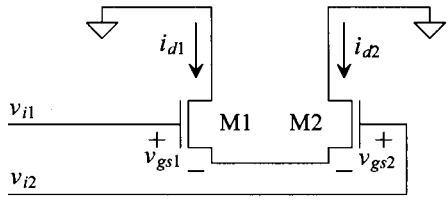


Figure 22.9 AC circuit for a diff-amp.

Example 22.4
Estimate the AC components of the drain currents of M1 and M2 for the circuit in Fig. 22.2 if $v_{I1} = 2.5 + 1mV \cdot \sin(2\pi \cdot 1kHz \cdot t)$. Verify your hand calculations using SPICE.

From Table 9.1 we know the g_m of the NMOS devices used in the diff-pair is 150 $\mu A/V$. The AC component of v_{I2} is zero so we know

$$v_{gs1} = -v_{gs2} = 0.5\ mV$$

and thus

$$i_d = g_m v_{gs} = (150 \times 10^{-6})(500 \times 10^{-6}) = 75\ nA$$

This is the AC component of the drain currents. When i_{d1} = 75 nA, then i_{d2} = –75 nA. The overall drain currents are written as

$$i_{D1} = 20\ \mu A + (75\ nA) \cdot \sin(2\pi 1k \cdot t) \text{ and } i_{D2} = 20\ \mu A - (75\ nA) \cdot \sin(2\pi 1k \cdot t)$$

The simulation results are seen in Fig. 22.10. ■

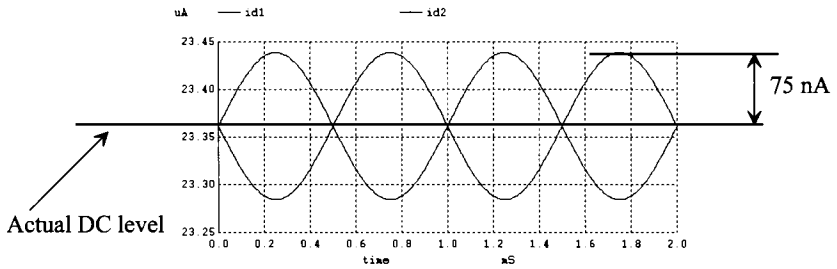


Figure 22.10 Simulation results for Ex. 22.4.

AC Gain with a Current Mirror Load

To determine the AC gain of the diff-amp with a current mirror load, Fig. 22.6, consider the small signal model seen in Fig. 22.11. We've replaced the diode-connected MOSFET, M3, with a $1/g_{m3}$ resistor. Also the resistance looking into the drain of M4 (r_{o4}) and the resistance looking into the drain of M2 (r_{o2}) are drawn explicitly. We assumed that the small-signal resistance looking into the drain of M2 is simply r_{o2} (for all practical design cases this is a good assumption). Note how, because of the current mirror action, the AC current flowing in M4 is i_{d1}. The current in M3 is mirrored by M4. The output voltage can be written as

$$v_{out} = (i_{d1} - i_{d2}) \cdot (r_{o2} || r_{o4}) \tag{22.20}$$

Knowing $i_{d1} = -i_{d2} = i_d$

$$v_{out} = 2i_d \cdot (r_{o2} || r_{o4}) \tag{22.21}$$

The differential mode gain is then written with the help of Eq. (22.19) as

$$A_d = \frac{v_{out}}{v_{di}} = \frac{v_{out}}{v_{i1} - v_{i2}} = g_m \cdot (r_{o2} || r_{o4}) \tag{22.22}$$

Notice that as the voltage on the gate of M1 increases, the current in M1 (and M3/M4) increases. This causes the output voltage to increase. When the gate potential of M2 increases, so does its drain current, causing the output voltage to decrease. Sometimes the gate potential of M1 is called the *noninverting* input and the gate potential of M2 is called the *inverting* input.

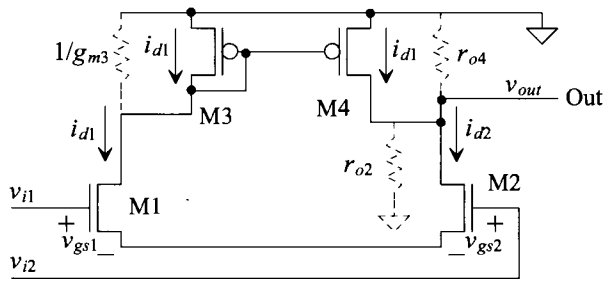


Figure 22.11 AC circuit of the diff-amp with a current-source load.

Example 22.5

Determine the output voltage for the diff-amp seen in Fig. 22.12. Verify your hand calculations using SPICE.

The tail current of the diff-amp conducts 20 μA so M1 and M2, when the inputs are equal, each conduct 10 μA. Using the parameters from Table 9.2 and Eq. (22.22), the gain of the diff-amp is

$$A_d = g_m \cdot (r_{on} || r_{op}) = (150 \times 10^{-6}) \cdot \left(\frac{167 \cdot 333}{167 + 333} \times 10^3 \right) = 16.7 \; V/V$$

This means that the 1 mV AC input will appear as a 16.7 mV AC output. The DC level on the output is $VDD - V_{SG} = 650 \; mV$. The output voltage is then

$$v_{out}(t) = 0.65 + (16.7 \; mV) \cdot \sin(2\pi 10 MHz \cdot t)$$

The simulation results are seen in Fig. 22.13. ■

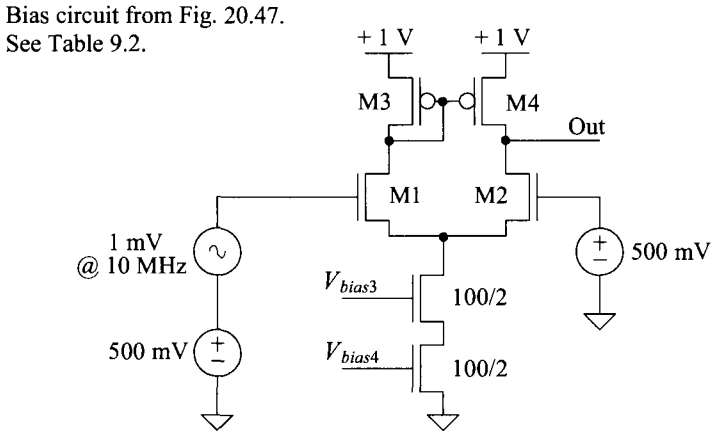


Figure 22.12 Circuit used in Ex. 22.5.

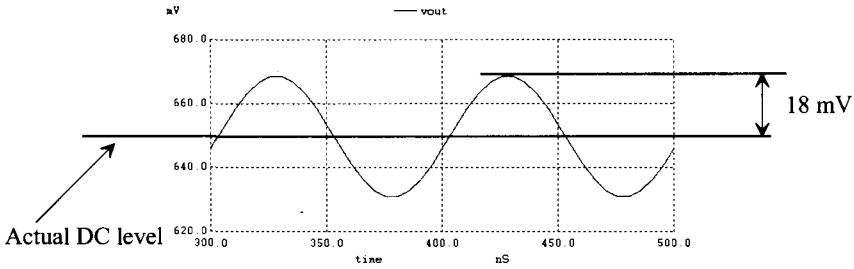


Figure 22.13 The output of the circuit in Fig. 22.12. Note that the transient analysis doesn't show the beginning of the simulation where the reference circuit is starting up.

Example 22.6

Estimate the f_{3dB} of the diff-amp in Ex. 22.5 if it drives a load capacitance of 1 pF. Verify your hand calculations with SPICE.

The resistance on the output node is $r_{o2} || r_{o4} = 111\ k\Omega$; therefore, since this is the *high-impedance node*, we can estimate the circuit's 3-dB frequency in the circuit as

$$f_{3dB} = \frac{1}{2\pi \cdot 111k \cdot 1\,pF} = 1.4\ MHz$$

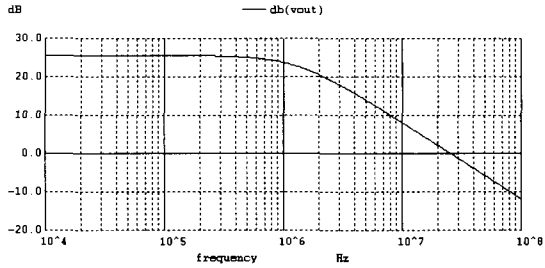


Figure 22.14 The AC response of the diff-amp in Fig. 22.12 when driving a 1 pF load capacitance.

The simulation results are seen in Fig. 22.14. ■

22.1.3 Common-Mode Rejection Ratio

An important aspect of the differential amplifier is its ability to reject a common signal applied to both inputs. Often, in analog systems, signals are transmitted differentially, and the ability of an amplifier to reject coupled noise into each line is very desirable. Consider the amplifier shown in Fig. 22.15. The bias current at the sources of M1/M2 has been replaced with its small-signal output resistance. The common-mode signal (the "noise" labeled in the figure) on both inputs is, ideally, rejected by the diff-amp. The diff-amp's output voltage doesn't vary. The noise causes the source potentials of M1/M2 to vary (the voltage across the tail current source).

If we apply an AC signal, v_c, to the gates of M1/M2, equivalent to saying that a common signal is applied to the input of the differential amplifier, we can calculate the common-mode gain. We begin by writing the AC small-signal, common-mode input voltage, v_c, as

$$v_c = v_{gs1,2} + 2i_d R_o \tag{22.23}$$

The MOSFETs M1 and M2 each source a current, i_d, through the output resistance of the current source, R_o (hence the factor of two in this equation). This equation may be rewritten as

$$v_c = i_d\left(\frac{1}{g_m} + 2R_o\right) \approx i_d 2R_o \tag{22.24}$$

The output voltage, because of the symmetry of the circuit, is given by

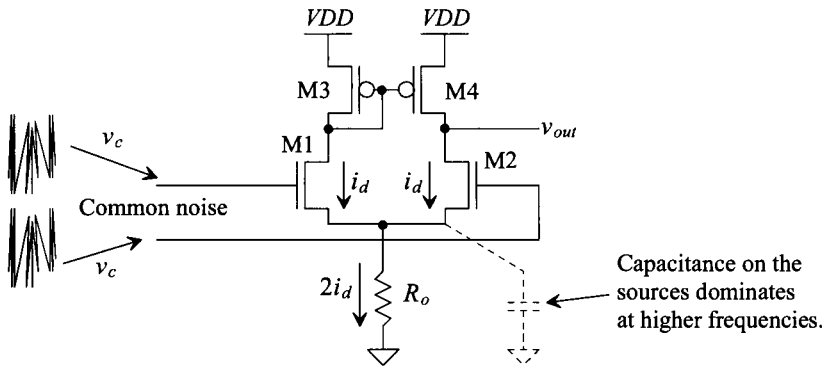


Figure 22.15 Calculating the CMRR of a diff-amp.

$$v_{out} = -i_d \cdot \frac{1}{g_{m3}} = -i_d \cdot \frac{1}{g_{m4}} \tag{22.25}$$

The common-mode gain is then

$$A_c = \frac{v_{out}}{v_c} = \frac{-1/g_{m3,4}}{2R_o} = -\frac{1}{2g_{m3,4}R_o} \tag{22.26}$$

Notice that by increasing the output resistance of the biasing current source, the common-mode gain drops. (This is good because we don't want any common signal to be amplified by the diff-amp.) The common-mode rejection ratio (*CMRR*), in dB, of a diff-amp with a current mirror load is given by

$$CMRR = 20 \cdot \log\left|\frac{A_d}{A_c}\right| = 20 \cdot \log[g_{m1,2}(r_{o2} \| r_{o4}) \cdot 2g_{m3,4}R_o] \tag{22.27}$$

The larger the *CMRR*, the better the performance of the diff-amp. For the diff-amp in Fig. 22.12, Eq. (22.27) evaluates to 86 dB. As the frequency of the input common-mode signal, v_c, increases, the *CMRR* goes down. This is the result of the impedance of the capacitance to ground on the sources of the diff-pair becoming much smaller than R_o.

Example 22.7

Simulate the *CMRR* of the diff-amp in Fig. 22.12. Show that the *CMRR* falls with increasing frequency.

As mentioned above, the (low-frequency) calculated *CMRR* is 86 dB. To simulate the *CMRR*, we perform AC simulations on two of the diff-amps in Fig. 22.12 so we can simultaneously determine A_d and A_c. The ratio of these gains is the *CMRR*. Figure 22.16 shows the simulation results. The common-mode gain, A_c, depends on the DC common-mode voltage. The results seen in Fig. 22.16 are with a common-mode (DC) voltage of 700 mV. Dropping the common-mode voltage down to 500 mV causes the low-frequency *CMRR* to drop down to 50 dB. The reason for this is that, with higher DC common-mode voltages, the voltage across the tail current source is higher, so its output resistance is larger. ■

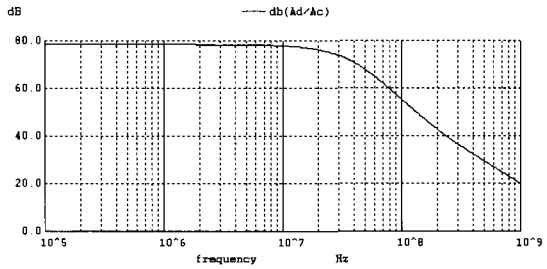


Figure 22.16 The simulated CMRR for the diff-amp in Fig. 22.12.

Input-Referred Offset from Finite CMRR

It's important we understand, in Eq. (22.26), why large R_o reduces A_c. Looking at Fig. 22.15, notice that as v_c varies so too will the voltage across the biasing current source (represented in this figure as R_o). As seen in Ch. 20, Fig. 20.4, variations in the voltage across a current source changes the output of the current source (unless its output resistance is infinite). This variation in current causes the current in M1 and M2 to change with variations in v_c. Changes in the drain current of M1/M2 (and thus M3/M4) causes the output voltage to change. Figure 22.17 shows how the output voltage changes as a function of the DC common-mode voltage. Understanding this circuit is *very important.* If we wanted to hold the diff-amp output voltage constant while varying the common mode voltage, we would have to apply a small voltage difference between the gates of M1 and M2 (*an offset voltage*). We'll revisit this important topic when we discuss op-amp *CMRR.*

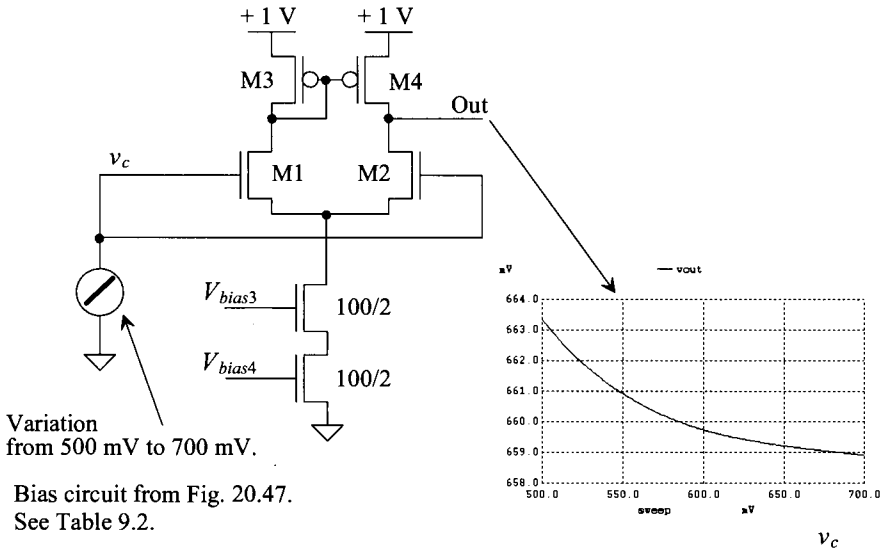


Figure 22.17 How variation in common-mode voltage affects the output voltage.

22.1.4 Matching Considerations

The fact that performance depends on the matching of devices is another important aspect of differential amplifiers. Layout techniques can be used to minimize the first-order effects of mismatch due to oxide gradients and other process variations. Figure 22.18 shows how the diff-pair would be laid out in a *common-centroid* configuration (see Ch. 5). Common-centroid layout, as the name implies, constructs two devices symmetrically about a common center in the layout. This allows the two devices to cancel process gradients in both the x and y directions and exposes both devices to heat sources in an identical manner. Note how we've attempted to match the parasitic capacitances of the pair (on the gates and drains) and how we've minimized the capacitance at the sources (to keep the *CMRR* high at higher frequencies).

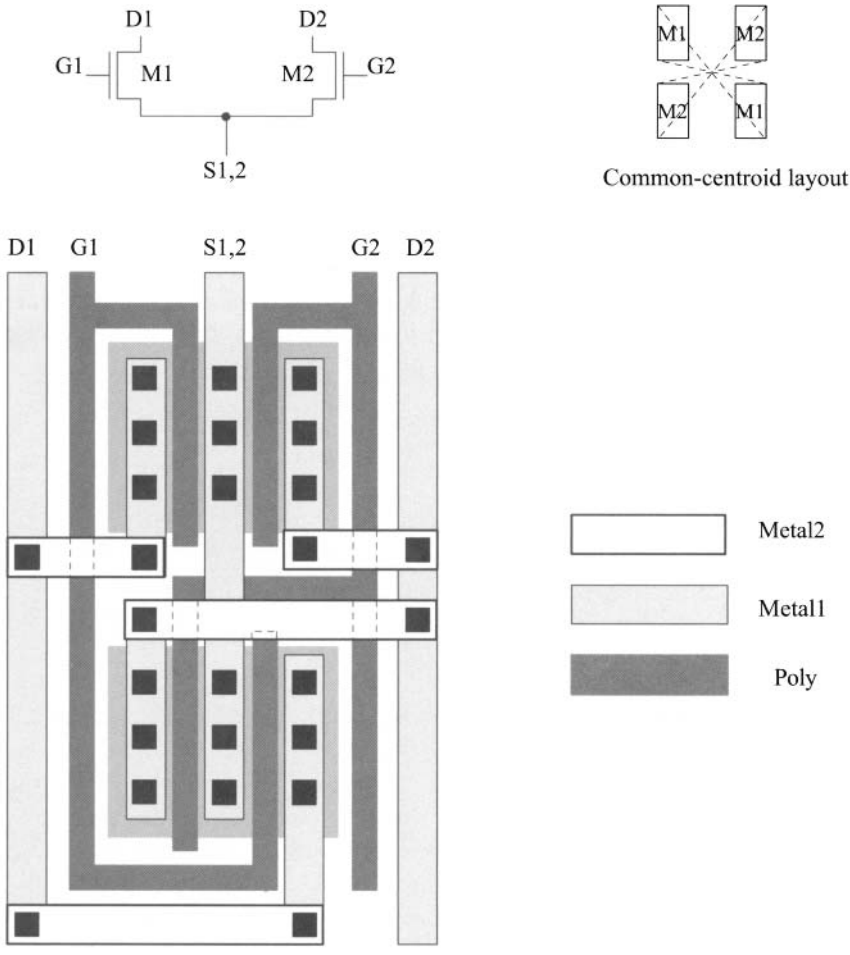


Figure 22.18 Common-centroid layout of a diff-pair.

The input-referred offset voltage of a diff-pair, resulting from mismatches in threshold voltage, geometries, and load resistances, can be determined with the help of Fig. 22.19. When the diff-pair is offset-free, connecting the diff-amp's inputs together causes the drain currents and drain voltages of M1 and M2 to be equal ($V_o = 0$). When the load resistors or M1 and M2 are mismatched, V_o is not zero. (We have mismatch and thus V_o is offset from its ideal value.). To drive V_o to zero, we apply a voltage difference between the gates of M1 and M2 (an input-referred offset).

$$V_{OS} = V_{GS1} - V_{GS2} = V_{THN1} + \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{THN2} - \sqrt{\frac{2I_{D2}}{\beta_2}} \qquad (22.28)$$

We can define the differences and averages of the threshold voltage, load resistance, and geometry as ΔV_{THN} (V_{THN1}–V_{THN2}), V_{THN} (average of V_{THN1} and V_{THN2}), ΔR_L (R_{L1}–R_{L2}), R_L (average of R_{L1} and R_{L2}), $\Delta(W/L)$ [(W_1/L_1)–(W_2/L_2)] and (W/L) [average of (W_1/L_1) and (W_2/L_2)]. Thus, we can make the appropriate substitutions into Eq. (22.28), requiring $I_{D1}R_{L1} = I_{D2}R_{L2}$, with the result:

$$V_{OS} = \Delta V_{THN} + \frac{V_{GS} - V_{THN}}{2} \cdot \left[\frac{-\Delta R_L}{R_L} - \frac{\Delta(W/L)}{(W/L)} \right] \qquad (22.29)$$

The threshold voltage mismatch must be reduced using layout techniques. Mismatches resulting from unequal geometry and differences in the load resistance can be reduced by designing with a small V_{GS} (V_{GS} close to V_{THN}). This should be compared with Eq. (20.8), which shows that using a small V_{GS} in a current mirror results in a large mirrored current difference.

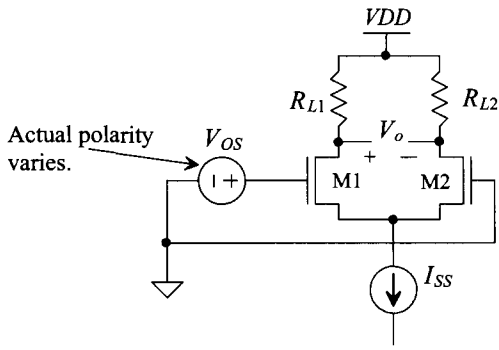


Figure 22.19 Determining diff-amp input offset voltage.

Input-Referred Offset with a Current Mirror Load

Suppose the diff-amp with current mirror load, Fig. 22.12, has an offset (the devices aren't perfectly matched). What this means is that the drain potential of M4 (M2) is not equal to the drain potential of M3 (M1 and most likely the drain currents in M1 and M2 aren't equal as well). The input-referred offset would then be the voltage difference on the gates of M1 and M2 needed to drive the output voltage to the correct value. Using Eq. (22.22), we can write the input-referred offset in terms of the difference-mode gain as

$$|V_{OS}| = \frac{V_{o,ideal}}{|A_d|} = \frac{V_{o,ideal}}{g_m \cdot (r_{o2} || r_{o4})} \tag{22.30}$$

which indicates that to reduce the input-referred offset voltage we simply need to design the diff-amp with large gain. This is the same result as that of Eq. (22.29), if we pause and think about it. To reduce the offset, we said we design with a small V_{GS}. If we hold the diff-amp's bias current constant and reduce V_{GS} (by increasing the widths of M1 and M2), we are increasing g_m.

Finally, although not clearly indicated by Eq. (22.30) as it is in Eq. (22.29), a mismatch in the diff-pair's threshold voltage can only be reduced by layout techniques (e.g., using common-centroid layout). Using large devices (larger-width MOSFETs), reduces variation in device characteristics and leads to better matching.

22.1.5 Noise Performance

The diff-amp with noise sources is seen in Fig. 22.20. The noise from M6 feeds equally into M1 and M2 (see Fig. 21.44 for comments about noise contributions from M5) and thus, because of the current mirror action in M3 and M4, ideally doesn't affect the output voltage. Therefore, we will ignore noise from M6 in the following discussion.

The diff-amp's output noise power spectral density (PSD) is given by

$$V_{onoise}^2(f) = \left(I_{M1}^2(f) + I_{M2}^2(f) + I_{M3}^2(f) + I_{M4}^2(f)\right) \cdot (r_{o2} || r_{o4})^2 \tag{22.31}$$

The input-referred noise PSD is then

$$V_{inoise}^2(f) = \frac{V_{onoise}^2(f)}{A_d^2} \tag{22.32}$$

Substituting in the difference-mode gain of the diff-amp, Eq. (22.22), we get

$$V_{inoise}^2(f) = \frac{I_{M1}^2(f) + I_{M2}^2(f) + I_{M3}^2(f) + I_{M4}^2(f)}{g_m^2} \tag{22.33}$$

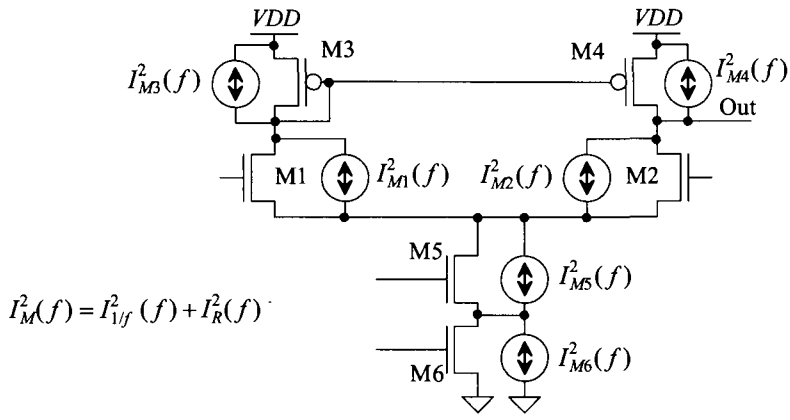


Figure 22.20 Noise model for the diff-amp.

By maximizing the transconductance, g_m, of the diff-pair, we can reduce the input-referred noise. This statement alone is a little misleading. As we saw in Eqs. (9.63)–(9.65), increasing the drain current increases the noise PSD. So to reduce the input-referred noise, we would want to maximize the transconductance by increasing the diff-pair's width (make M1 and M2 wide), not by increasing I_{SS}.

22.1.6 Slew-Rate Limitations

Like the class A amplifiers studied in the last chapter, the basic diff-pair also exhibits slew-rate limitations. As seen in Fig. 22.21, when either M1 or M2 turns off, the total current available to charge a load capacitance is I_{SS}. The slew-rate is then (see also Eq. (21.38))

$$\text{slew rate} = \frac{dV_{out}}{dt} = \frac{I_{SS}}{C_L} \tag{22.34}$$

For high-speed, we need a large bias current. However, this causes excess power dissipation. Once again, to get high-speed (large current drive capability) with low quiescent power dissipation, let's look at a class AB configuration.

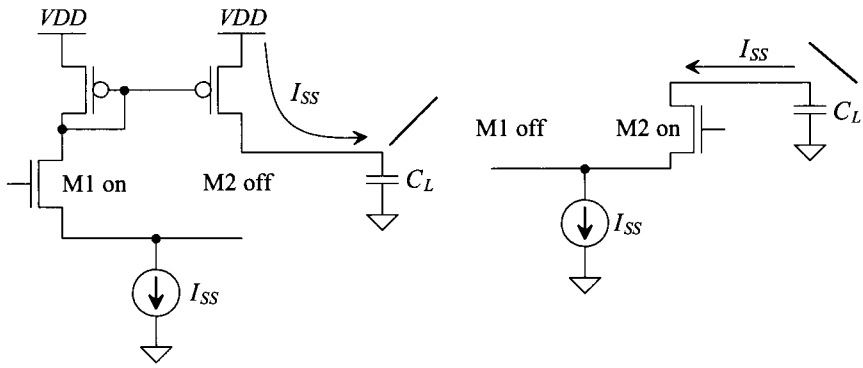


Figure 22.21 Slew-rate limitations in diff-amps.

22.2 The Source Cross-Coupled Pair

The source cross-coupled pair is shown in Fig. 22.22. This configuration is very useful in practical circuit design because it can eliminate slew-rate limitations. A diff-amp built with the source cross-coupled pair can operate in the class AB mode with significant output drive current. Assuming that both inputs to the pair are connected to a (the same) voltage within the pair's common-mode input range and that all NMOS are sized the same and that all PMOS are sized the same, a current I_{SS} flows in all the MOSFETs in the circuit. Note that M11, M21, M31, and M41 are simply behaving as biasing batteries. Their gate-source voltages are mirrored by M1–M4 to set the DC operating current. Using the parameters in Table 9.1 with the gates of M1 and M2 (v_{I1} and v_{I2}) at 3.5 V and I_{SS} of 20 μA, the gate of M3 is at a constant potential that we will label v_{I2}–V_{bias} (or $V_{bias} = V_{GS21} + V_{SG31} = 2.2$ V neglecting body effect).

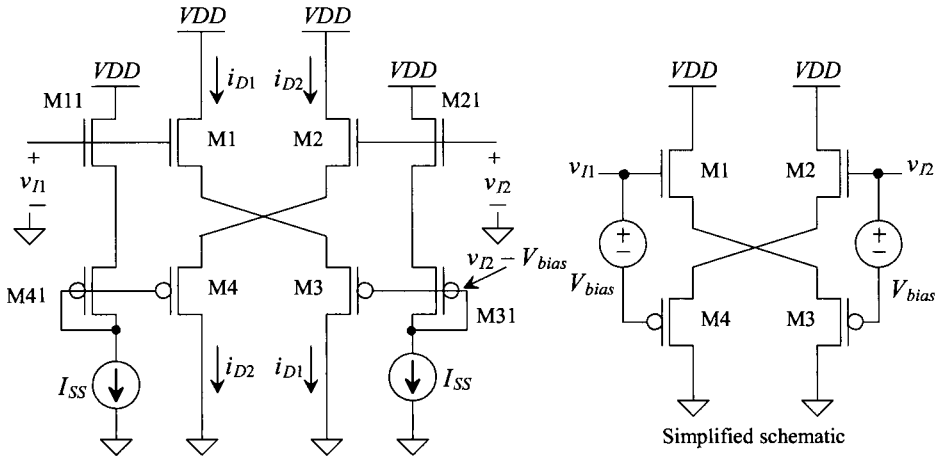


Figure 22.22 Source cross-coupled differential amplifier with NMOS input devices.

Operation of the Diff-Amp

An important characteristic of the source cross-coupled differential amplifier is that as v_{DI} is increased, i_{D1} continues to increase and i_{D2} shuts off, while the opposite is true when v_{DI} decreases. In other words, the amplifier is operating class AB where neither of the output currents is zero as long as their magnitudes remain less than I_{SS}. Looking at the simplified schematic in Fig. 22.22, if v_{I1} increases, then M1 turns on. Because the gate potential of M3 is constant, it turns on as well. In other words, an increase in v_{I1} causes the gate-source voltages of both M1 and M3 to increase (i_{D1} increases). At the same time, the gate potential of M4 increases. This cause both M4 and M2 to shut off (i_{D2} shuts off).

Example 22.8

Simulate the operation of the diff-amp in Fig. 22.22 using the parameters from Table 9.1.

The simulation results are seen in Fig. 22.23. Note that when both inputs are at 3.5 V, the output currents are equal. This figure should be compared to Fig. 22.3.

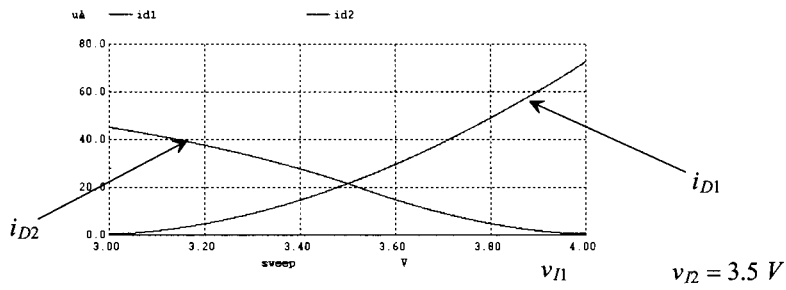


Figure 22.23 The output currents of the diff-amp in Fig. 22.22.

Note how in Fig. 22.3, the output currents flatten out above a maximum input voltage. Here the current continues to increase. ■

After looking at the results of this example, we might wonder: why use such a complicated diff-amp if the output current is only three times more than what we get with the basic diff-amp discussed in the first section? We can always just scale up the current in a basic diff-amp to get more drive. The benefits of the source cross-coupled diff-amp are seen in special-purpose, *low-power* design. In low-power design, the gate source voltages are close to the threshold voltages (and so low power equates to low speed, see Eq. [9.36]). Consider the amplifier and simulation results seen in Fig. 22.24. Here we've increased the widths of the amplifying devices and reduced their bias current (by sizing up the lengths of the biasing current sources as seen in the figure). When the two inputs are the same voltage, the quiescent current that flows in the diff-amp is a few microamps. However, if one input gets a little larger than the other input, the drain-current increases dramatically. In a low-power design, this topology would be useful to quickly charge a capacitor while burning little quiescent power.

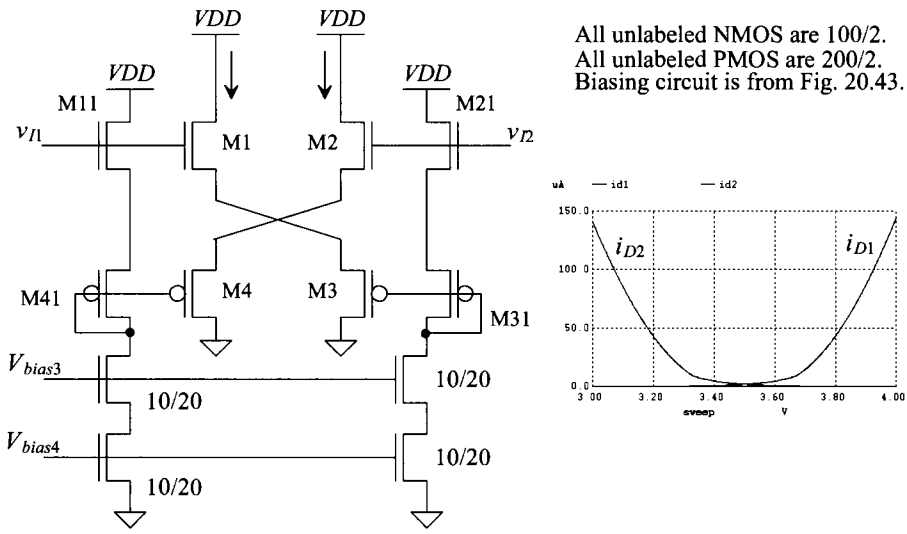


Figure 22.24 Lowering the power in the source cross-coupled diff-amp.

Input Signal Range

The drawback of the source cross-coupled diff-amp is the limited input range. The PMOS version of the source cross-coupled differential amplifier is shown in Fig. 22.25. Normally the version (PMOS or NMOS) of this differential amplifier depends on the input signal range. The NMOS version has the best positive input signal range, while the PMOS version has the best negative input signal range. For centering the input signal range the topology seen in Fig. 22.26 can be used. Again, both an NMOS V_{GS} and a PMOS V_{SG} are used to bias the cross-coupled diff-amp. Note that the biasing devices

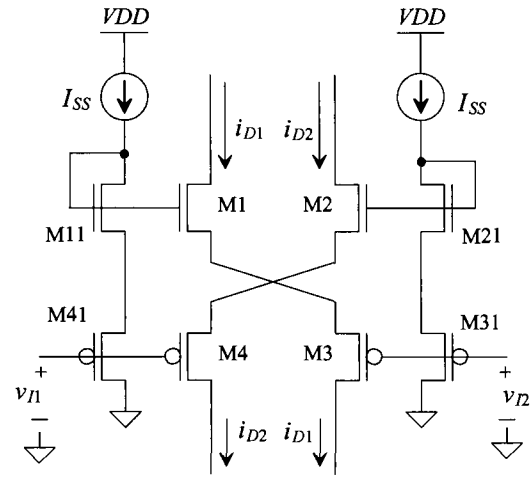


Figure 22.25 Source cross-coupled differential amplifier, PMOS.

(M11, M21, M31, and M41) experience body effect differently than M1–M4. This causes the currents in M1–M4 to be less than the current in the biasing devices. If possible, place M1–M4 and the biasing devices in their own wells to eliminate the body effect. Note that when very low currents are used, the constant current sources driving the gates of M1–M4 can cause slew-rate limitations. To eliminate this problem, capacitors can be placed between the gates of M1/M4 and M2/M3 to make the biasing appear more battery-like.

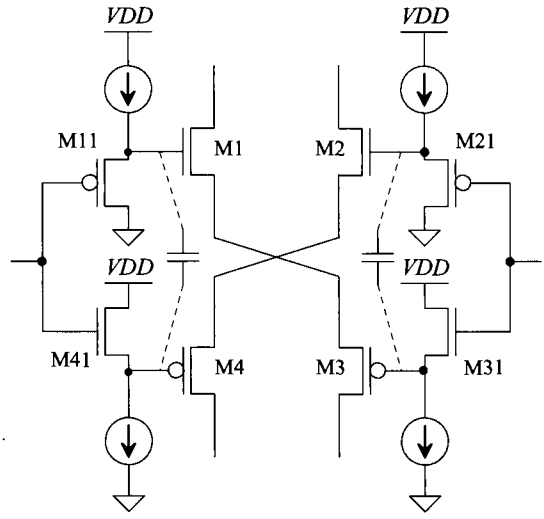


Figure 22.26 Biasing scheme used to shift input common-mode range. Note that the body effect affects the biasing, causing the current in M1–M4 to decrease.

22.2.1 Current Source Load

The source cross-coupled differential amplifier with active loads is shown in Fig. 22.27. Note that we could have also added a pair of active loads in series with the drains of M1 and M4 to obtain a differential output amplifier (two complementary amplifier outputs). Superposition can be used to find the AC small-signal gain from the output back to each input. First, determine the small-signal gain, $\frac{v_o}{v_{i1}}$, with v_{i2} at AC ground. Neglecting the bulk effect, we can see that the voltage gain from the gate of M1 to the source of M1 is simply a common drain amplifier of the form

$$\frac{v_{s1}}{v_{i1}} = \frac{g_{m1}R_{Leq}}{1+g_{m1}R_{Leq}} \text{ V/V} \tag{22.35}$$

where R_{Leq} is simply the load seen by the source of M1. This can be found by using a test source (as seen in Fig. 22.28) to determine the effective impedance seen looking into the source of M3. This results in

$$R_{Leq} = \frac{v_t}{i_t} = \frac{1+\frac{1}{g_{m5}r_{o3}}}{g_{m3}+\frac{1}{r_{o3}}} \approx \frac{1}{g_{m3}} \tag{22.36}$$

Therefore, the voltage gain from v_{i1} to the source of M1 becomes

$$\frac{v_{s1}}{v_{i1}} = \frac{g_{m1}\frac{1}{g_{m3}}}{1+g_{m1}\frac{1}{g_{m3}}} \tag{22.37}$$

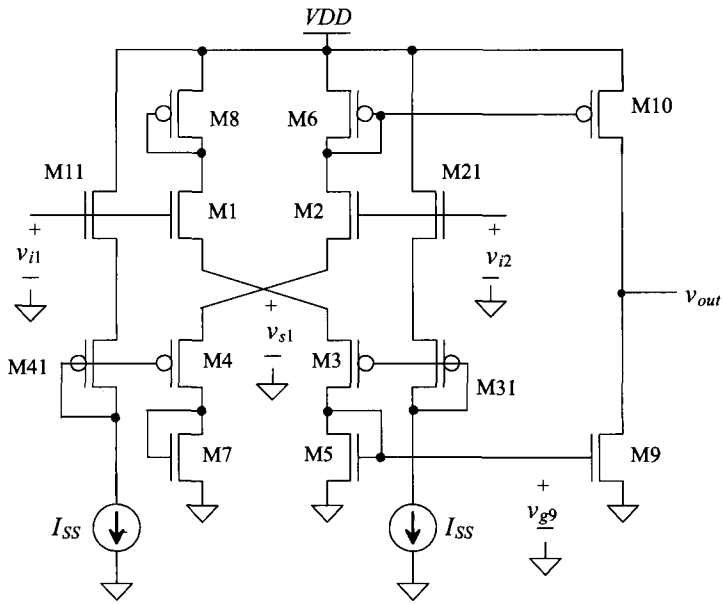


Figure 22.27 Source cross-coupled differential amplifier, with current source loads.

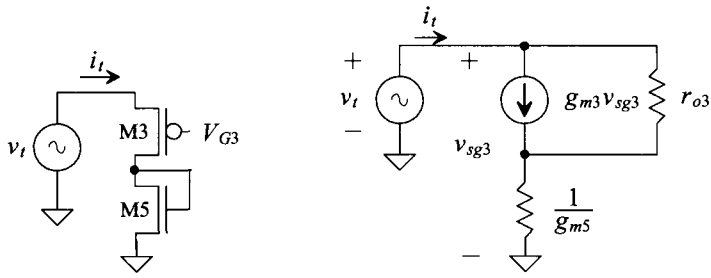


Figure 22.28 (a) Simplified schematic and (b) small-signal model.

The voltage gain from v_{s1} to v_{g9} is the same form as a common gate amplifier. This gain is

$$\frac{v_{g9}}{v_{s1}} = g_{m3}\frac{1}{g_{m5}} \tag{22.38}$$

And finally, the gain from the gate of M9 to the output is simply $-g_{m9}(r_{o9}||r_{o10})$, and

$$\frac{v_o}{v_{i1}} = -\frac{g_{m1}\frac{1}{g_{m5}}}{1+g_{m1}\frac{1}{gm3}}g_{m9}(r_{o9}||r_{o10}) \text{ for } v_{i2}=0 \tag{22.39}$$

Using the same type of analysis, we find that the expression from v_{i2} to the output is

$$\frac{v_o}{v_{i2}} = \frac{g_{m2}\frac{1}{g_{m6}}}{1+g_{m2}\frac{1}{gm4}}g_{m10}(r_{o9}||r_{o10}) \text{ for } v_{i1}=0 \tag{22.40}$$

Superposition can now be used to determine the total effect of each input on the output. Therefore, if M1 and M2 are matched, as are M3 and M4, and if M5 and M6 are designed so that their g_ms are equal as are M7 and M8 (respectively), then the differential gain can be expressed as

$$v_o = (v_{i2}-v_{i1})\frac{2\cdot g_{m1,2}\frac{1}{g_{m5,6}}}{1+g_{m1,2}\frac{1}{gm3,4}}g_{m9,10}(r_{o9}||r_{o10}) \Rightarrow \frac{v_o}{v_{di}} = \frac{2\cdot g_{m1,2}\frac{1}{g_{m5,6}}}{1+g_{m1,2}\frac{1}{gm3,4}}g_{m9,10}(r_{o9}||r_{o10}) \tag{22.41}$$

Input Signal Range

The positive-input, common-mode range (CMR) is determined in exactly the same manner as in the source coupled diff-amp of the first section. The positive CMR is given by

$$v_{CMMAX} \approx VDD - \sqrt{\frac{2I_{SS}}{\beta_6}} = VDD - V_{DS,sat} \tag{22.42}$$

while the negative CMR is given by

$$v_{CMMIN} = \overbrace{\sqrt{\frac{2I_{SS}}{\beta_1}} + V_{THN}}^{V_{GS1}} + \overbrace{\sqrt{\frac{2I_{SS}}{\beta_3}}}^{V_{DS3}} + \overbrace{\sqrt{\frac{2I_{SS}}{\beta_5}} + V_{THN}}^{V_{GS5}} \tag{22.43}$$

An alternative current source (current mirror) load configuration is shown in Fig 22.29. The gain of this configuration is given by

$$A_d = \frac{v_{out}}{v_{i1} - v_{i2}} = 2 \cdot \frac{r_{o2} || r_{o6}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}}} \tag{22.44}$$

assuming $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$.

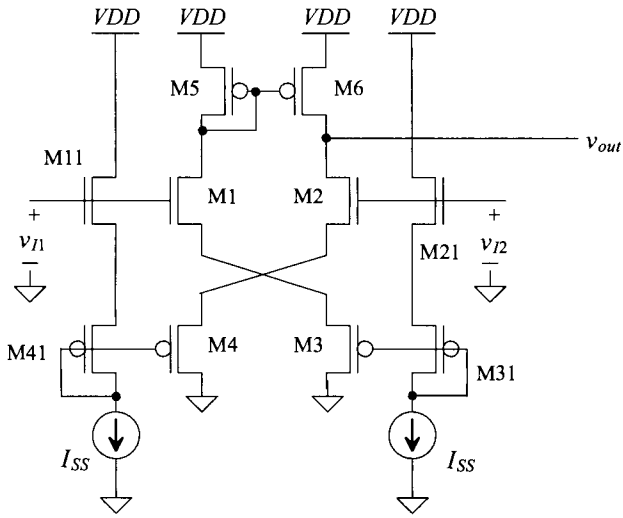


Figure 22.29 Alternative current source load configuration.

22.3 Cascode Loads (The Telescopic Diff-Amp)

The differential amplifier with current source load of Fig. 22.6 gave a voltage gain of $g_m(r_{o2} || r_{o4})$. For many applications, this gain may be too low. Using a cascode current source load in place of M3/M4, results in a gain of approximately $g_m r_{o2}$ (the output resistance of the load becomes much larger than the resistance looking into the drain of M2). This modest improvement in gain can be increased by also cascoding M1 and M2. Figure 22.30 shows the resulting circuit configuration (sometimes called a *telescopic diff-amp*). The MOSFET M6 is selected so that its V_{GS} keeps M1/M2 and MC1/MC2 in the saturation region. The gain of this configuration is given by

$$A_d = g_{m1} \cdot (R_{into\ DC2} || R_{into\ DC4}) \tag{22.45}$$

The resistance looking into the drain of MC2, assuming M2 and MC2 are the same size, is given by

$$R_{into\ DC2} \approx g_{m2} \cdot r_{o2}^2 \tag{22.46}$$

and the resistance looking into the drain of MC4, again assuming MC4 and M4 are the same size, is given by

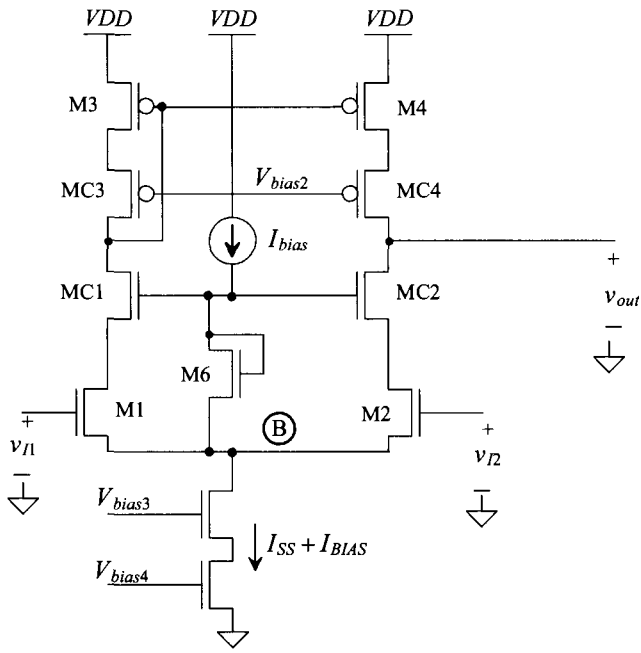


Figure 22.30 Cascode differential amplifier.

$$R_{into\ DC4} \approx g_{m4} \cdot r_{o4}^2 \tag{22.47}$$

The gain of the cascode differential amplifier may be written as

$$A_d = g_{m1}\left(g_{m2}r_{o2}^2 \| g_{m4}r_{o4}^2\right) \tag{22.48}$$

The main drawback of using the cascode differential amplifier is the reduction in positive common-mode range. In the negative direction, V_{CMMIN} is identical to the source-coupled diff-amp discussed in Sec. 22.1. The positive common-mode signal is limited by the additional circuitry required by the cascode loads. Notice that V_{CMMAX} in this case is limited by the amount of voltage necessary to keep M1, MC1, MC3, and M3 in their respective saturation regions.

An interesting issue concerning this circuit is the DC feedback through M6. Because the current through M6 is constant, V_{GS6} will be constant. Normally, an increase in the common-mode voltage on the gates of M1 and M2 causes their drain voltages to decrease. However, because the currents through M1 and M2 are constant, the common source node, marked as node B in Fig. 22.30, increases with the increasing input voltage. This causes the gate potential of MC1 and MC2 to increase. The result is that the drain voltages of M1 and M2 go up (since the gate-source voltages of MC1 and MC2 are constant). This feedback action attempts to keep M1 and M2 from going into nonsaturation. The maximum common-mode voltage, V_{CMMAX}, will be limited by the output voltage and by MC1/MC2 going into nonsaturation.

Example 22.9

Determine the minimum and maximum input common-mode voltage for the diff-amp seen in Fig. 22.31. Note that the voltage across M6 is $V_{GS} + V_{DS,sat}$, where V_{GS} is the gate-source voltage of the other NMOS devices in this figure (see Fig. 20.32 and the associated discussion).

Parameters from Table 9.1
Unlabeled PMOS are 30/2.
Unlabeled NMOS are 10/2.
Bias circuit from Fig. 20.43.

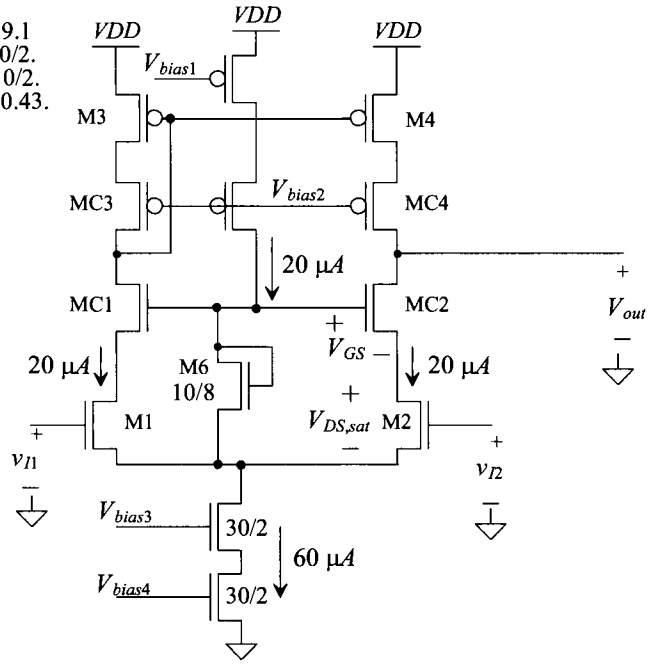


Figure 22.31 Cascode differential amplifier.

The minimum input common-mode voltage is given by

$$V_{CMMIN} = V_{GS1,2} + 2V_{DS,sat} = 1.05 + 0.5 = 1.55\ V$$

As mentioned a moment ago, MC1 and MC2 must be kept in the saturation region. If we assume that the drains of MC1 and MC2 are at $VDD - V_{SG}$ (= 3.85 V), then when MC1 and MC2 are on the verge of trioding (their drain-source voltages are $V_{DS,sat}$), the drains of M1 and M2 are at

$$V_{D1,2} = VDD - V_{SG} - V_{DS,sat} = 3.6\ V$$

We know for an NMOS device (M1 or M2) to be in saturation

$$V_D \geq V_G - V_{THN} \text{ and so } V_{D1,2} \geq V_{CMMAX} - V_{THN}$$

giving a $V_{CMMAX} = 4.4\ V$. In terms of an arbitrary output voltage, we can write

$$V_{CMMAX} = V_{out} - V_{DS,sat} + V_{THN}$$

so if V_{out} is 2.45 V, then $V_{CMMAX} = 3\ V$. ■

22.4 Wide-Swing Differential Amplifiers

An increasingly important concern with the advent of low-voltage design is the need for improved common-mode range. A technique for extending the allowable input swing of a diff-amp is to use two complementary diff-amp stages in parallel, as shown in Fig. 22.32. To understand the operation of this circuit, consider the case when the DC component of the input signal, v_{in}, is such that both diff-amps are on (and the AC component is small compared to the DC). The current through the diff-pairs M1/M2 and M9/M10 is I, while the current through the summing MOSFETs M4 and M12 is $2I$. If M5 is the same size as M4 and if M7 is the same size as M12, then a current $2I$ flows in the output transistors. The small-signal voltage gain, assuming $g_{m1} = g_{m2}$ and $g_{m9} = g_{m10}$, is given by

$$A_v = (g_{m1} + g_{m9})[r_{o7}(2I) \| r_{o5}(2I)] = \frac{(g_{m1} + g_{m9})}{\lambda_7 2I + \lambda_5 2I} = \frac{\sqrt{2\beta_1 I} + \sqrt{2\beta_9 I}}{2I(\lambda_7 + \lambda_5)} \tag{22.49}$$

If the input is such that the p-channel diff-amp is on and the n-channel diff-amp is off, then a current I flows in the summing MOSFETs M4 and M12 and zero current flows in M1, M2, M3, and M6. The current that flows in M5 and M7 is now I. The small-signal voltage gain is

$$A_v = g_{m9}[r_{o7}(I) \| r_{o5}(I)] = \frac{\sqrt{2\beta_9 I}}{I(\lambda_7 + \lambda_5)} \tag{22.50}$$

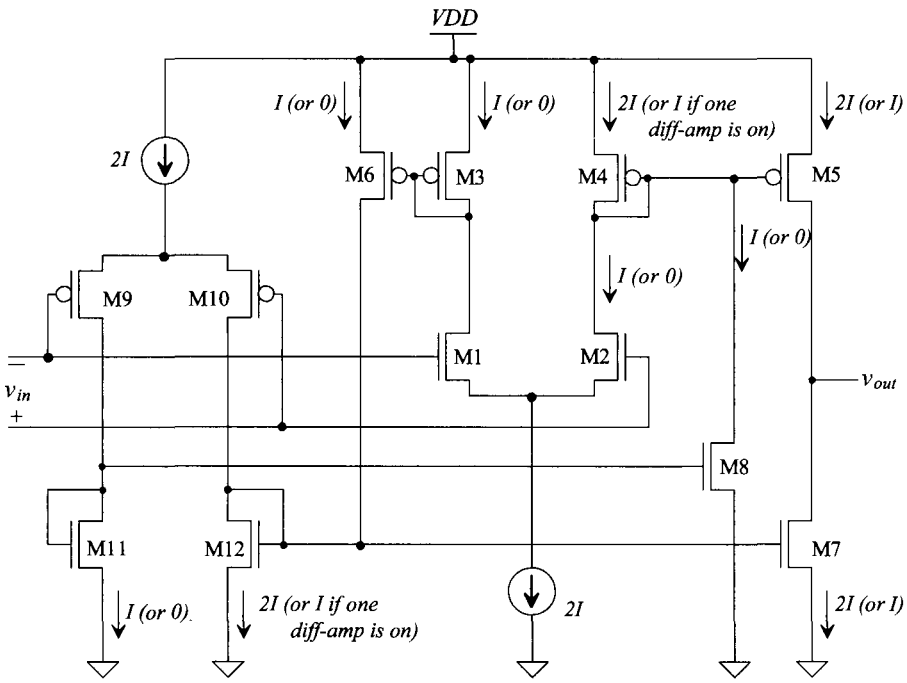


Figure 22.32 Two parallel differential amplifiers used to increase input swing.

The small-signal gain when the p-channel diff-amp is off and the n-channel diff-amp on is given by

$$A_v = g_{m1}[r_{o7}(I) \| r_{o5}(I)] = \frac{\sqrt{2\beta_1 I}}{I(\lambda_7 + \lambda_5)} \tag{22.51}$$

It is desirable to transition smoothly from having a single diff-amp on to having both diff-amps on. If we require

$$\beta_1 = \beta_9 = \beta \Rightarrow G_m = \sqrt{2\beta I} \tag{22.52}$$

then Eqs. (22.49) through (22.51) can be rewritten as

$$A_v = G_m \cdot [r_{o7}(I) \| r_{o5}(I)] \tag{22.53}$$

For low distortion, a constant gain is important. Also, for a stable amplifier, it is important that the amplifier can be compensated to ensure stability. An amplifier whose gain depends on the input signal amplitude may be more challenging to compensate for.

22.4.1 Current Differential Amplifier

Another wide-swing, differential amplifier is the current differencing amplifier. The current diff-amp is shown schematically in Fig. 22.33. In the following discussion, let's assume that M1 through M4 are the same size. If both i_1 and i_2 are zero, then a current I_{SS} flows in all MOSFETs in the circuit. Now assume that i_1 is increased above zero, but less than I_{SS}. This causes the current in both M1 and M2 to increase. As a result, the drain current in M3 decreases to keep $i_{D2} + i_{D3} = 2I_{SS}$. The decrease in M3 drain current is mirrored in M4, forcing the current i_1 out of the diff-amp. A similar argument can be made for increasing i_2; that is, it causes the output of the differential amplifier to sink a current equal to i_2. The sizes of M1–M4 can be ratioed to give the diff-amp a gain or to scale the input currents.

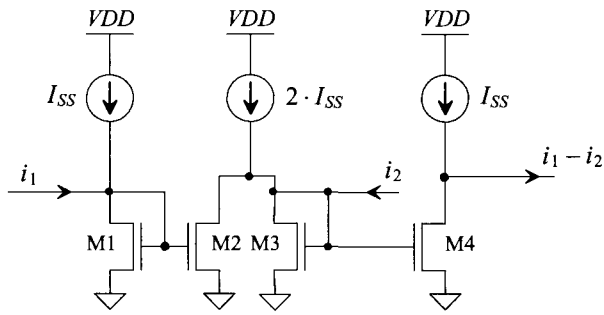


Figure 22.33 Current differential amplifier.

The input impedance of the current differential amplifier is simply the small-signal resistance of a diode-connected MOSFET, or

$$R_{in} = \frac{1}{g_m} \tag{22.54}$$

This configuration finds applications in both low-power and high-speed circuit design.

22.4.2 Constant Transconductance Diff-Amp

A rail-to-rail differential amplifier made using n- and p-channel diff-amps is shown in Fig. 22.34. It is desirable, for good distortion and proper compensation, that the overall transconductance of the diff-amp remain constant independent of the region of operation, that is, operation with both n- and p-channel diff-amps on or only a single diff-amp on. A constant g_m is guaranteed over the input range if

$$g_m = g_{mn} + g_{mp} = \sqrt{2\beta_n I_n} + \sqrt{2\beta_p I_p} = \text{constant} \tag{22.55}$$

where g_{mn} and g_{mp} are the transconductances of the n- and p-channel diff-amps and g_m is the overall transconductance of the input stage. Since β_n and β_p are constant and can be made equal, Eq. (22.55) can be rewritten as (assuming both diff-amps are operating),

$$\sqrt{I_n} + \sqrt{I_p} = \text{constant} \tag{22.56}$$

This equation always holds if both differential amplifiers are on. The problem with nonconstant transconductance occurs if only one diff-amp is on. If, for example, the common-mode input (common input voltage on the + and – inputs of the differential amplifier) is large enough to shut the p-channel diff-amp off, then $I_p = 0$ and the transconductance of the overall input diff-amp changes.

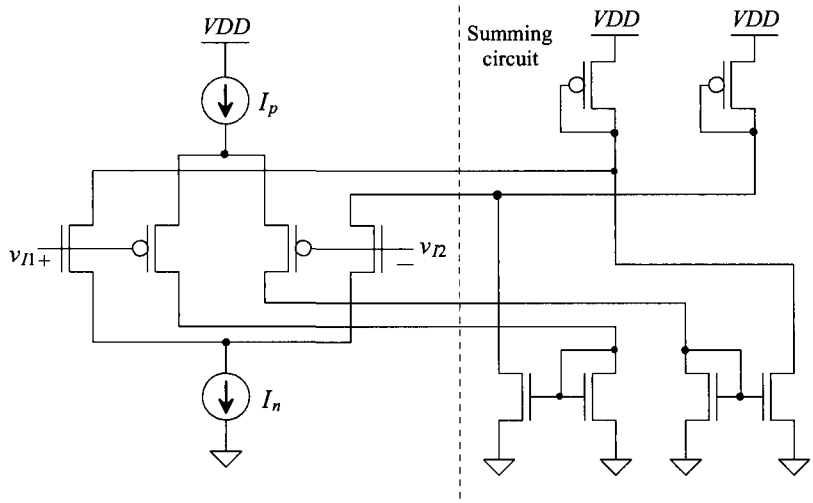


Figure 22.34 Rail-to-rail differential amplifier.

The solution to the problem of non-constant g_m begins by making

$$I_n = I_p = I_o \tag{22.57}$$

When both diff-amps are on (keeping in mind that we have already set the requirement that $\beta_n = \beta_p$), Eq. (22.56) reduces to

$$2\sqrt{I_o} = \text{constant} \tag{22.58}$$

If we add a current of $3I_o$ to I_n (or to I_p) when the p-channel diff-pair (n-channel diff-pair) is off, the transconductance of the pair is constant, or

$$\overbrace{2\sqrt{I_o}}^{\text{both on}} = \overbrace{\sqrt{3I_o + I_n}}^{\text{n diff-amp on}} = \overbrace{\sqrt{3I_o + I_p}}^{\text{p diff-amp on}} \text{ if } I_o = I_p = I_n \qquad (22.59)$$

An example of a constant-g_m , rail-to-rail input stage is shown in Fig. 22.35. The summing circuit of Fig. 22.34 is not shown in this figure. MOSFETs M1–M4 make up the p- and n-channel diff-pairs, while MP1 and MN1 source the constant current I_o when both diff-pairs are on. (MP1 and MN1 represent the constant current sources shown in Fig. 22.28.) When both diff-pairs are on, the current out of each current diff-amp is approximately 0. (The drain current of M6 and M7 is approximately 0.) If the common-mode input voltage becomes large enough to shut the p-channel diff-pair off, then MOSFETs MS1 and MS2 are off as well. This causes the current in M5 to become I_o. The current in M6 mirrors the current in M5. Since M6 is three times larger than M5, the current in M6 becomes $3I_o$.

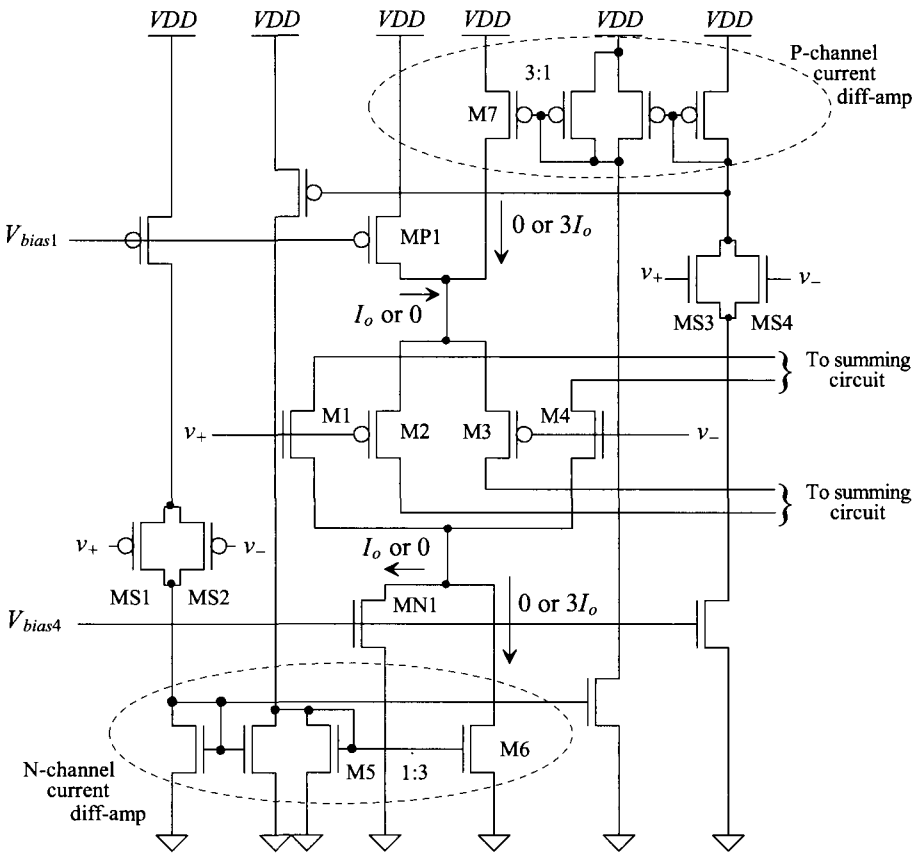


Figure 22.35 A wide-swing diff-amp with constant gm.

Discussion

In general, the constant-g_m diff-amp is used in an op-amp to prevent overcompensation of the op-amp and to avoid distortion when the op-amp is used with large signals where the diff-amps, on the input of the op-amp, are turning on and off with variations in the input signal. Several practical problems exist with these uses of the constant-g_m diff-amp. Because the value of g_m may vary with shifts in the process, we may still overcompensate an op-amp design. Using the constant-g_m stage to avoid overcompensation is useful, but since we may overcompensate (or undercompensate) the op-amp with process variations, the added complexity and power draw may not justify the additional circuitry. Using the constant-g_m stage to avoid distortion is based on keeping the unity gain frequency of an op-amp, f_{un}, a constant independent of the common-mode input voltage. In practice, mismatches (threshold voltage and geometry) in the input diff-pair and changes in DC biasing conditions, resulting from the diff-amps turning off and on, can cause distortion. In some cases, this distortion can be worse than the distortion resulting from the nonconstant f_{un} (which we get with the nonconstant g_m diff-amp). The distortion resulting from mismatches can be modeled as an offset-voltage that is dependent on the input common-mode voltage. Since the DC currents sourced or sunk from a constant-g_m diff-amp are not constant, the DC operating point of the circuit summing the currents changes with the input signal's amplitude. The result is a change in the low-frequency gain and added distortion.

ADDITIONAL READING

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[4] J. H. Botma, R. F. Wassenaar, and R. J. Wiegerink, "A Low-Voltage CMOS Op Amp with a Rail-to-Rail Constant-g_m Input Stage and a Class AB Rail-to-Rail Output Stage," *Proceedings of the 1993 IEEE ISCAS,* p. 1314.

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PROBLEMS

22.1 Determine the drain current of M1 as a function of the input voltage, $v_{I1} - v_{I2}$, for the diff-amp shown in Fig. 22.36. Neglect body effect. What does your derivation give for i_{D1} when v_{I1} is much larger than v_{I2}?

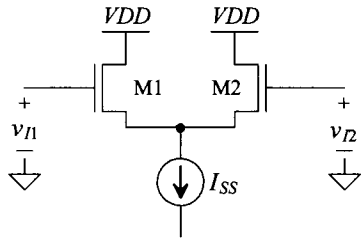

Figure 22.36 Diff-amp used in Problem 22.1

22.2 Repeat Ex. 22.1 if the widths of M1 and M2 are increased from 10 to 100. Determine the transconductance of the diff-amp. Write i_{d2} as a product of g_m (= g_{m1} = g_{m2}) and v_{I1} (with v_{I2} = AC ground), v_{I2} (with v_{I1} = AC ground), and $v_{I1} - v_{I2}$.

22.3 Determine the maximum and minimum common mode voltages for the PMOS version of the diff-amp seen in Fig. 22.4.

22.4 Determine the AC currents flowing in the circuit of Fig. 22.5 if the gate of M1 is grounded and the gate of M2 is an AC signal of 1 mV. Verify your answers with an AC SPICE simulation.

22.5 Determine the small-signal gain and the input common-mode-range (CMR) for the diff-amps shown in Fig. 22.37. Verify your answers with SPICE.

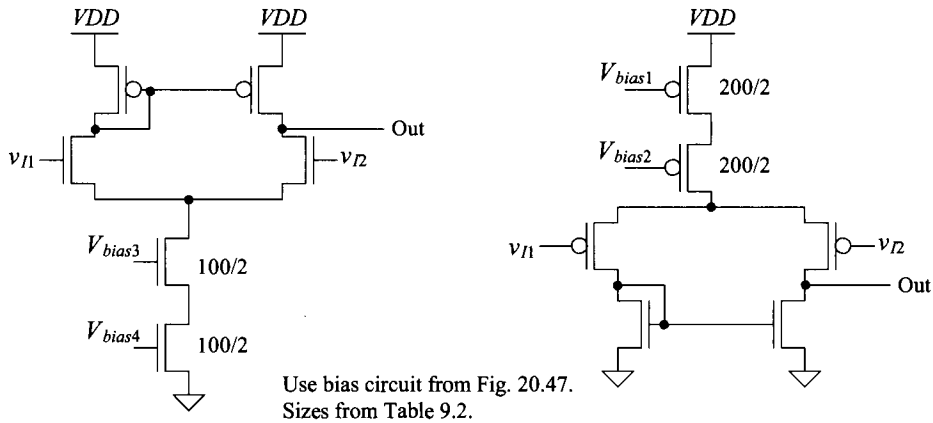

Figure 22.37 Diff-amps for Problem 22.5.

22.6 Show that the capacitance on the sources of M1/M2 in Ex. 22.6 causes the *CMRR* to roll off quicker with increasing frequency. (Add a capacitance to the sources of M1/M2 in a simulation and show that *CMRR* decreases at a lower frequency.)

22.7 Estimate the slew-rate limitations in charging and discharging a 1 pF capacitor tied to the outputs of the diff-amps shown in Fig. 22.37. Verify with SPICE.

22.8 For the n-channel diff-pair shown in Fig. 22.38, show that the following relationships are valid if the body effect is included in the analysis of the transconductance.

$$i_{d1} = \frac{g_m}{2}\left[v_{i1}\left(2 - \frac{g_m}{g_m + g_{mb}}\right) - v_{i2} \cdot \frac{g_m}{g_m + g_{mb}}\right] - \frac{g_m \cdot g_{mb}}{g_m + g_{mb}} \cdot \frac{[v_{i1} + v_{i2}]}{2}$$

and

$$i_{d2} = \frac{g_m}{2}\left[v_{i2}\left(2 - \frac{g_m}{g_m + g_{mb}}\right) - v_{i1} \cdot \frac{g_m}{g_m + g_{mb}}\right] - \frac{g_m \cdot g_{mb}}{g_m + g_{mb}} \cdot \frac{[v_{i1} + v_{i2}]}{2}$$

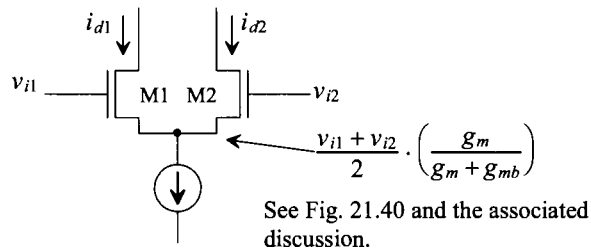

Figure 22.38 How body effect changes the AC behavior of the diff-amp.

22.9 The diff-amp configuration shown in Fig. 22.39 is useful in situations where a truly differential output signal is needed. Determine the following: (a) the transconductance of the diff-amp, (b) the AC small-signal drain currents of all MOSFETs in terms of the input voltages and g_{mn} (the transconductance of an n-channel MOSFET), and (c) the small-signal voltage gain, $(v_{O+} - v_{O-})/(v_{I+} - v_{I-})$. Verify your answers with SPICE.

22.10 Using the diff-amp topology in Fig. 22.24 and a current mirror load, show how quickly (or slowly) the diff-amp can drive a 1 pF load. Does this diff-amp exhibit slew-rate limitations? Verify your answers with SPICE.

22.11 Using the topology seen in Fig. 22.26 with the long-channel process (Table 9.1) without body effect (all MOSFET's bodies tied to their respective sources), show that the currents in M1–M4 match the biasing currents used in the source followers. Show how the currents become mismatched when the bodies of the NMOS are tied to ground and the bodies of PMOS are tied to *VDD*.

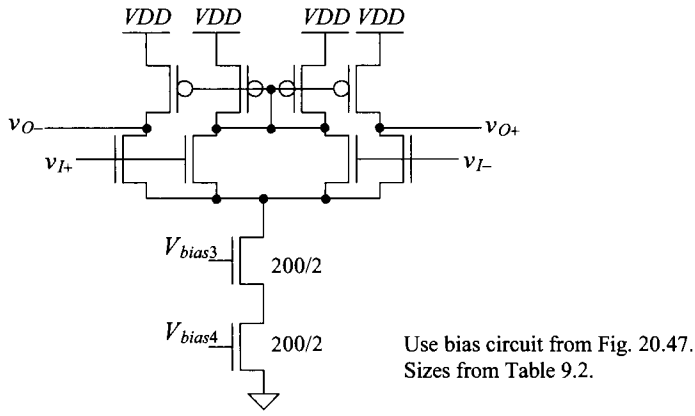

Figure 22.39 Fully differential diff-amp used in Problem 22.9.

22.12 Simulate the operation of the diff-amp seen in Fig. 22.31. Use a common-mode voltage of 2.5 V and an AC input voltage of 100 μV at 1 kHz. Compare the simulation results to your hand calculations.

22.13 Using SPICE with current sources for inputs, show the operation of the diff-amp in Fig. 22.33.

22.14 The circuit seen in Fig. 22.40 is an another example of a circuit that sums the currents from NMOS and PMOS diff-amps (so the input common-mode range can extend from beyond the power supply rails). Describe and simulate the operation of this circuit using the short-channel parameters in Table 9.2 and the bias circuit from Fig. 20.47.

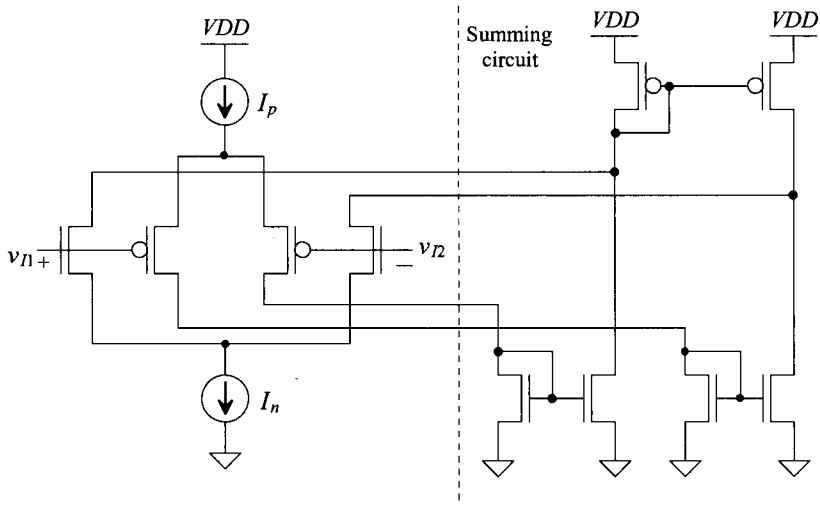

Figure 22.40 Summing circuit for Problem 22.14.

22.15 Using symbolic analysis, determine the small-signal gain of the self-biased diff-amp seen in Fig. 22.41 (see also Fig. 18.17).

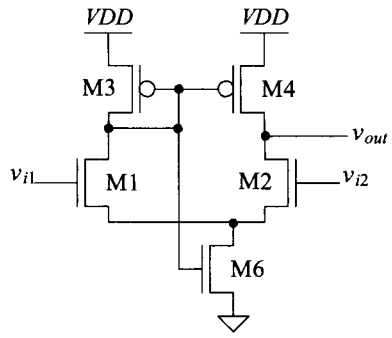

Figure 22.41 A self-biased NMOS diff-amp.