Chapter

23

# Voltage References

A general-use (ideal) voltage reference is a circuit used to generate a fixed voltage, $V_{REF}$, that is independent of the power supply voltage *VDD* (where $V_{REF} < VDD$), temperature, and process variations. In other words, the ideal reference voltage is independent of PVT. In some cases, we want to design a reference that varies with temperature. For example, if $V_{REF}$ increases with temperature, Fig. 23.1a, we say that the reference voltage is *proportional to absolute temperature* or PTAT. If the reference voltage decreases with increasing temperature, Fig. 23.1b, the reference is said to be *complementary to absolute temperature* or CTAT. The PTAT and CTAT references can be used to design a voltage reference that changes very little with temperature called a *bandgap* reference. Unfortunately, the generation of PTAT and CTAT reference voltages requires using parasitic diodes. In a CMOS process, the electrical characteristics of the parasitic pn junctions are not monitored and controlled (like, say, the threshold voltage) during manufacturing. Therefore, if possible, the implementation of a reference voltage using MOSFET-resistor circuits is desirable.

This chapter is split into two sections. The first section covers the design of voltage references using MOSFETs and resistors, while the second section covers the design of voltage references using parasitic diodes. The first section also offers some overview material common to all voltage references.

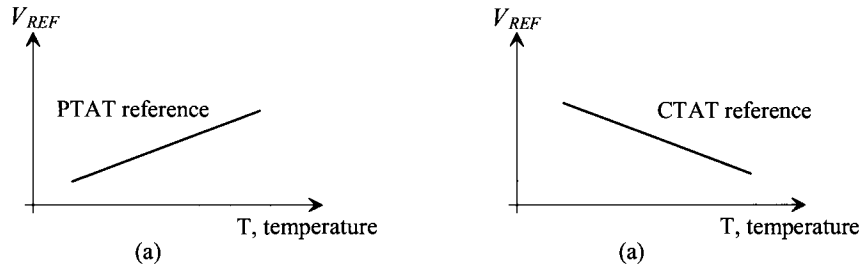



**Figure 23.1** (a) PTAT and (b) CTAT voltage references.

## 23.1 MOSFET-Resistor Voltage References

We can derive reference voltages from the power supplies using the resistor and the MOSFET, as seen in Fig. 23.2. The voltage divider formed with two resistors has the advantage of simplicity, temperature insensitivity (as was shown in Ch. 5), and process insensitivity; that is, changes in the sheet resistance have no effect on the voltage division. The main problem with this circuit is that in order to reduce the power dissipation (i.e., the current through the resistors), the resistors must be made large. Since large resistors require a large area on the die, this voltage divider may not be practical in many cases. One situation where we will use this simple voltage divider is in generating a voltage halfway between *VDD* and ground, *VDD*/2, (sometimes called the *common-mode* voltage of an analog circuit or system).

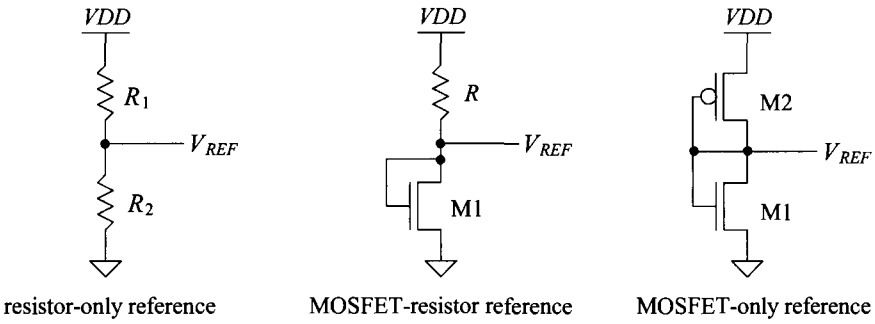



**Figure 23.2** Voltage dividers implemented in CMOS.

The voltage divider formed between the resistor and the MOSFET can be recognized as the same circuit we used for a bias in the current mirror back in Ch. 20 (see Fig. 20.2 and Eqs. (20.26)–(20.31)). The final reference, a voltage divider between NMOS and PMOS devices, has the advantage that the layout can be small (see Fig. 20.13 and Eqs. (20.12)–(20.19)). In the following two subsections, we analyze the behavior of these last two voltage dividers.

### 23.1.1 The Resistor-MOSFET Divider

The reference voltage used in the resistor-MOSFET divider is equal to the $V_{GS}$ of the MOSFET. We can write for this circuit

$$I_D = \frac{VDD - V_{REF}}{R} = \frac{\beta_1}{2}(V_{REF} - V_{THN})^2 \tag{23.1}$$

or

$$V_{REF} = V_{THN} + \sqrt{\frac{2I_D}{\beta_1}} = V_{THN} + \sqrt{\frac{2(VDD - V_{REF})}{R \cdot \beta_1}} \tag{23.2}$$

If $V_{REF}$ is designed so that it is close to $V_{THN}$, then the reference voltage will be insensitive to changes in *VDD* and its temperature behavior will follow the threshold voltage (see

Eqs. (9.43)–(9.48)). However, for the general case, the temperature coefficient of the resistor-MOSFET voltage divider is determined using

$$TCV_{REF} = \frac{1}{V_{REF}} \cdot \frac{\partial V_{REF}}{\partial T} \tag{23.3}$$

and if we assume $VDD >> V_{REF}$, then

$$TCV_{REF} = \frac{1}{V_{REF}}\left[ V_{THN} \cdot TCV_{THN} - \frac{1}{2}\sqrt{\frac{2L_1}{W_1} \cdot \frac{VDD}{R \cdot KP(T)}} \cdot \left[\frac{1}{R}\frac{\partial R}{\partial T} - \frac{1.5}{T}\right]\right] \tag{23.4}$$

**Example 23.1**

Estimate the temperature performance of the resistor-MOSFET voltage references seen in Fig. 23.3. Assume that the temperature coefficient of the resistor is 2,000 *ppm/C*, the long-channel process is used where $KP_n$ = 120 μA/V$^2$, and the nominal *VDD* is 5 V. Use simulations to verify the answers. Also show how the reference voltages change with *VDD*.


**Figure 23.3** Resistor-MOSFET references used in Ex. 23.1

For the reference made using the 1MEG resistor, Fig. 23.3a, the current that flows in the circuit is

$$I = \frac{VDD - V_{REF}}{10^6} = \frac{KP_n}{2} \cdot \frac{W}{L}(V_{REF} - V_{THN})^2$$

which can be solved to determine $I$ is around 4 μA and

$$V_{REF} = V_{GS} \approx 900\ mV$$

From Sec. 9.1.3 the rate the threshold voltage changes with temperature is

$$\frac{\partial V_{THN}}{\partial T} \approx -1\ mV/C^{\circ} \approx \frac{\partial V_{REF}}{\partial T}$$

The temperature coefficient of the reference voltage is

$$TCV_{REF} = \frac{1}{V_{REF}}\frac{\partial V_{REF}}{\partial T} = \frac{-0.001}{0.9} = -1,111\ ppm/C^{\circ} \tag{23.5}$$

and thus

$$V_{REF}(T) = V_{REF} \cdot (1 + TCV_{REF}(T - T_0)) = 0.9 \cdot (1 - 0.00111(T - 25))) \tag{23.6}$$

where we assume that the threshold voltage was measured at 25 °C. The simulation results are seen in Fig. 23.4. Note that at higher temperatures the threshold voltage decreases and thus so does $V_{REF}$. Further note that a change in temperature of 25 °C corresponds to a change in the reference voltage of 31.25 mV (= 25 · 0.00125).

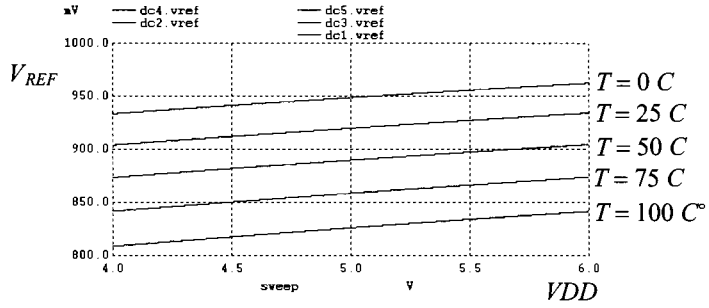



**Figure 23.4** How the reference voltage changes with VDD and temperature for the reference in Fig. 23.3a.

To estimate the temperature behavior of the circuit in Fig. 23.3b, we must first determine the value of $V_{REF}$. Using Eq. (23.2), we can write

$$V_{REF} = V_{THN} + \sqrt{\frac{2(VDD - V_{REF})}{R \cdot \beta_1}} = 0.8 + \sqrt{\frac{2(5 - V_{REF})}{10k \cdot \frac{10}{2} \cdot 120\mu A/V^2}}$$

After a few iterations, we can determine $V_{REF} \approx 1.85\ V$. The temperature coefficient is calculated using Eq. (23.4)

$$TCV_{REF} = \frac{1}{1.85} \cdot \left[ -1\ mV/C^\circ - \frac{1}{2}\sqrt{\frac{2 \cdot 2}{10} \cdot \frac{5}{10k \cdot 120\ \mu A/V^2}} \cdot \left[ 0.002 - \frac{1.5}{300} \right] \right]$$

which evaluates to $TCV_{REF} = 500\ ppm/C$. The simulation results are seen in Fig. 23.5. Note how, when comparing Figs. 23.4 and 23.5, one reference circuit performs well with regard to temperature (23.3b), while the other reference circuit (23.3a) performs well with regard to *VDD* variations. ■

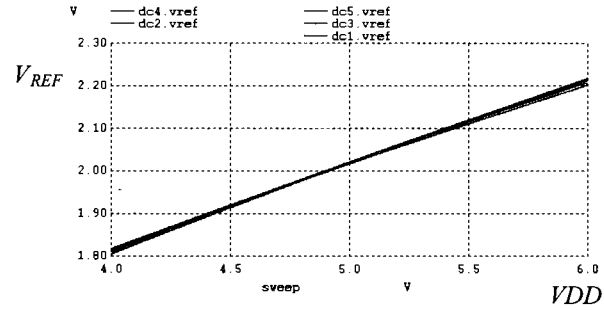



**Figure 23.5** How the reference voltage changes with VDD and temperature for the reference in Fig. 23.3b.

A modification to the basic resistor-MOSFET divider is shown in Fig. 23.6. The reference voltage in this circuit is given by

$$V_{REF} = V_{GS}\left(\frac{R_1}{R_2} + 1\right) \tag{23.7}$$

noting the ratio of the resistors (and so their temperature behavior or sheet resistance shift with process variations) doesn't affect the reference voltage. When $V_{GS}$ is designed to be approximately $V_{THN}$, the resulting reference circuit is said to be a threshold-voltage multiplier reference circuit.

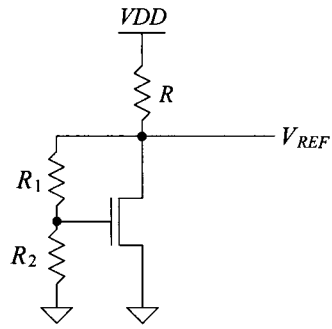



**Figure 23.6** Modification of the resistor-MOSFET voltage divider.

### 23.1.2 The MOSFET-Only Voltage Divider

The MOSFET-only voltage divider shown in Fig. 23.2 generates a reference voltage that is equal to the voltage on the gates of the MOSFETs with respect to ground. Since $I_{D1} = I_{D2}$, we can write

$$\frac{\beta_1}{2}(V_{REF} - V_{THN})^2 = \frac{\beta_2}{2}(VDD - V_{REF} - V_{THP})^2 \tag{23.8}$$

or the reference voltage is given by

$$V_{REF} = \frac{VDD - V_{THP} + \sqrt{\frac{\beta_1}{\beta_2}} \cdot V_{THN}}{\sqrt{\frac{\beta_1}{\beta_2}} + 1} \tag{23.9}$$

or knowing the desired reference voltage and the power supply voltage

$$\frac{\beta_1}{\beta_2} = \left[\frac{VDD - V_{REF} - V_{THP}}{V_{REF} - V_{THN}}\right]^2 \tag{23.10}$$

The temperature dependence of the MOSFET-only voltage divider, assuming the temperature dependence of the ratio of the transconductance parameters, $\frac{\beta_1}{\beta_2}$, is negligible, is given by

$$TCV_{REF} = \frac{1}{V_{REF}} \cdot \frac{\partial V_{REF}}{\partial T} = \frac{1}{V_{REF}} \cdot \frac{1}{\sqrt{\frac{\beta_1}{\beta_2}} + 1} \cdot \left[\frac{\partial(-V_{THP})}{\partial T} + \sqrt{\frac{\beta_1}{\beta_2}} \frac{\partial V_{THN}}{\partial T}\right] \tag{23.11}$$

From Ch. 9, we know for the long-channel devices

$$\frac{\partial V_{THN}}{\partial T} = -1\ mV/C^{\circ} \tag{23.12}$$

and

$$-\frac{\partial V_{THP}}{\partial T} = 1.4\ mV/C^{\circ} \tag{23.13}$$

To achieve $TCV_{REF} = 0$, requires

$$-\frac{\partial V_{THP}}{\partial T} = -\sqrt{\frac{\beta_1}{\beta_2}} \cdot \frac{\partial V_{THN}}{\partial T} \Rightarrow 1.4\ mV/C^{\circ} = \sqrt{\frac{\beta_1}{\beta_2}} \cdot 1\ mV/C^{\circ} \tag{23.14}$$

or

$$\sqrt{\frac{\beta_1}{\beta_2}} = 1.4 \tag{23.15}$$

Zero temperature coefficient, to a first order, can be met by satisfying this equation. However, this ratio is most often set by the desired $V_{REF}$.

### 23.1.3 Self-Biased Voltage References

We've already presented a voltage reference back in Ch. 20 using the beta-multiplier reference (BMR) (see Figs. 20.15, 20.19, and 20.22). Consider the BMR seen in Fig. 23.7. The added amplifier forces the drain/gates of M1 and M2 to the same potential. Because the gates and sources of M3/M4 are at the same potential, the same current is forced through each side of the reference. *This is an important common theme for all of the self-biased references discussed in this chapter.* We'll discuss this in greater detail in a moment. Before moving on to this topic, let's discuss why we connect the inverting and noninverting inputs to the added amplifier in the way seen in Fig. 23.7. (Why is M2 connected to the + amplifier input instead of the – input?) For the amplifier to be stable, we want the amount of signal fed back and subtracted from the input to be larger than the

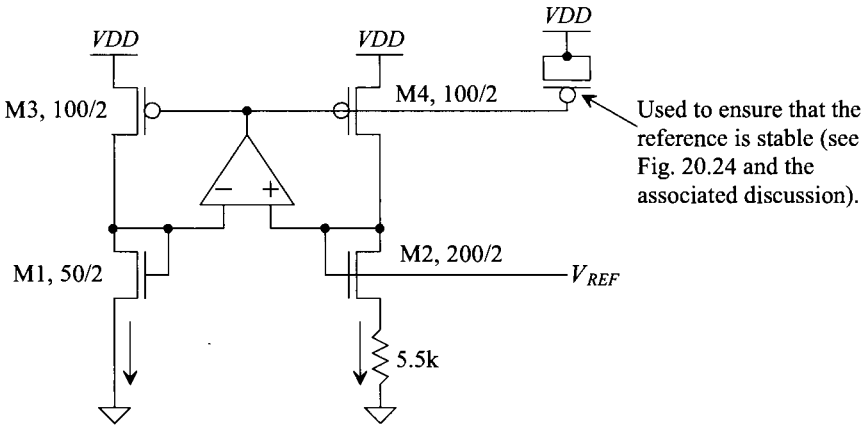



**Figure 23.7** BMR from Figs. 20.19 and 20.22.

amount of signal fed back and added to the input. Because M3 and M4 are *inverting* common-source amplifiers, we want the signal fed back to the + input of the amplifier to be larger than the signal fed back to the – input of the amplifier. Since the (AC) currents flowing in M3 and M4 are equal and the small-signal resistance of M2 + $R$ is larger than the small-signal resistance of M1, we connect M2 to the + amplifier input.

*Forcing the Same Current through Each Side of the Reference*

The simplest method to force the same current through each side of a reference is to use a simple current mirror, Fig. 23.8a. As we saw in Fig. 20.15, the low-output resistance found in short-channel devices makes the resulting reference very sensitive to changes in *VDD*. By cascoding the current mirror, Fig. 23.8b, the currents can be made more equal and the sensitivity to *VDD* can be reduced. The problem with using a cascode current mirror is that the minimum allowable *VDD* increases. Consider the following.


**Figure 23.8** Using a current mirror to force the same current through each side of a reference.

**Example 23.2**

Resimulate the BMR in Fig. 20.18 using a cascode current mirror for the PMOS devices as seen in Fig. 23.9.

Using the cascode current mirror, we expect the currents through each branch of the reference to be very nearly equal. As seen in the simulation results in Fig. 23.10, the currents *are* equal. However, they are not constant and independent of changes in *VDD*. Similarly, if we were to use $V_{biasn}$ as a reference voltage (see Sec. 20.1.5), then $V_{biasn}$ would show a large sensitivity to changes in *VDD*. The problem with cascoding only the PMOS devices is that while the currents through each branch are equal (but not constant), the variation with *VDD* is still present. The voltages at the drains of M1 and M2 change with *VDD*. To reduce this voltage variation, we might consider cascoding the NMOS devices as well (see Fig. 23.11). The PMOS devices are still used to force the same current through each side of the reference, while now the NMOS cascode stack is used to keep the voltages across M1 and M2 constant with changes in *VDD*. As the simulation results, Fig. 23.12, show, the currents do stabilize but at a voltage 20% higher than *VDD*. Clearly, cascoding devices won't be useful in a short-channel CMOS process (and so *we'll stick with using the added amplifier to both set the currents*

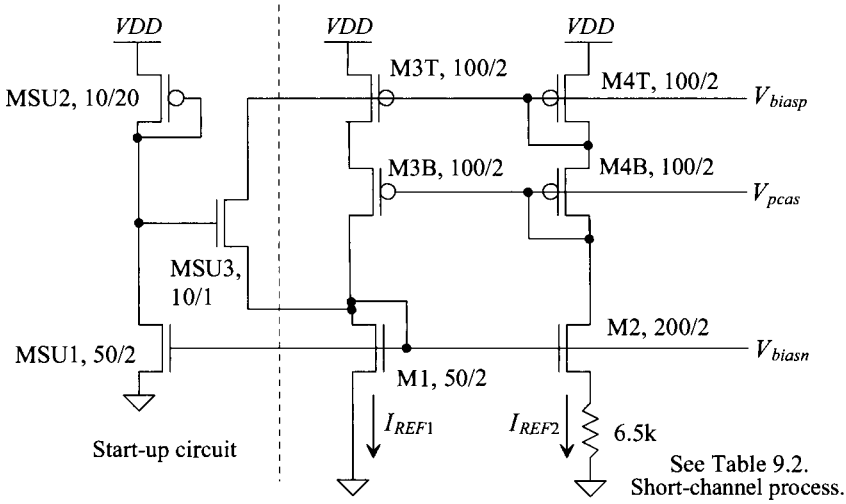



**Figure 23.9** Cascoding the PMOS devices in the BMR circuit.

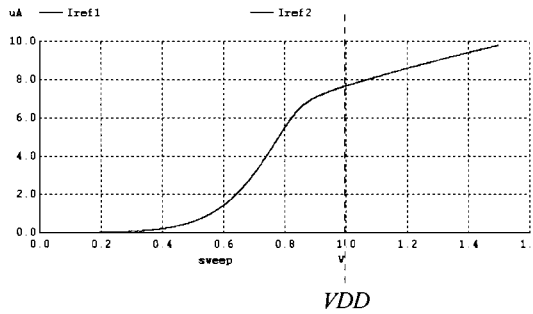



**Figure 23.10** Simulating the behavior of the currents in the BMR of Fig. 23.9.

*and hold the voltage across M1 and M2 constant in the remainder of the* ***short-channel CMOS*** *designs presented in this chapter*). Note that cascoding devices can be useful when designing in long-channel CMOS processes. In these processes, the threshold voltage is a smaller percentage of the power supply voltage. For example, in our short-channel process, Table 9.2, this percentage is 28%. In the long-channel process, Table 9.1, it is 16%. Also note that using NMOS cascodes alone won't make the reference more tolerant to changes in *VDD*. The NMOS cascodes will keep the voltages across M1 and M2 constant (but not equal). Since the currents through each branch aren't equal (because the PMOS devices aren't cascoded), we still get significant sensitivity to *VDD*.

Finally, we need to, again (see Fig. 20.15 and the associated discussion), mention the importance of the start-up circuit. The start-up circuit is often overlooked and is often a cause of problems in practical designs. We include a start-up circuit in every self-biased reference to avoid the situation where zero

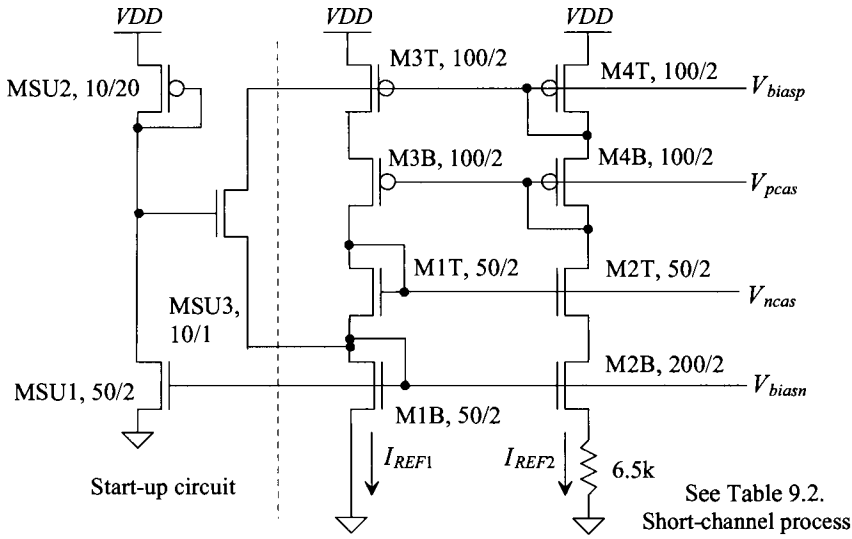



**Figure 23.11** Cascoding both NMOS and PMOS devices in the BMR circuit.

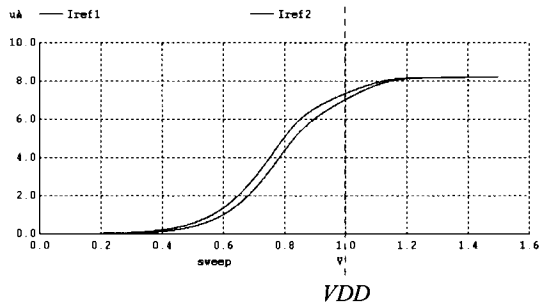



**Figure 23.12** Simulating the behavior of the currents in the BMR of Fig. 23.11.

current flows in the reference. It's important to ensure that the start-up circuit doesn't affect normal operation or draw too much current from *VDD*. For the start-up circuit seen in Figs. 23.9 and 23.11, we use the $V_{biasn}$ to set the current drawn by the bias circuit. In normal operation, MSU3 should be off (it should have a negative $V_{GS}$). ■

**Example 23.3**

Using the topology seen in Fig. 20.22, design a voltage reference with, ideally, zero temperature coefficient. Simulate the design to determine the reference's sensitivity to changes in temperature and *VDD*. Comment on the repeatability of the $V_{REF}$ (with process variations from one process run to the next) and methods (and concerns) with trimming $V_{REF}$. Assume $TCR = 0.002$ (2,000 ppm/C).

We begin by writing the long-channel equation, Eq. (20.40), for the resistance needed for zero temperature coefficient (ZTC)

$$R = \frac{2}{\frac{\partial V_{THN}}{\partial T} \cdot KP_n \cdot \frac{W}{L}} \left(1 - \frac{1}{\sqrt{K}}\right) \cdot \left(\frac{1}{R}\frac{\partial R}{\partial T} + \frac{1}{KP_n} \cdot \frac{\partial KP_n}{\partial T}\right) \quad (23.16)$$

While this equation won't directly apply for the design in a short-channel process, we can use it, with simulations, to help point us to the factors that influence the temperature behavior of the reference. Substituting in the appropriate numbers with $K = 4$, we get

$$R = \frac{1}{(-0.0006) \cdot KP_n \cdot \frac{W}{L}} \cdot \left((0.002) - \frac{1.5}{300}\right) \quad (23.17)$$

or

$$R = \frac{5}{KP_n \cdot \frac{W}{L}} \quad (23.18)$$

To move the reference towards a ZTC, let's set the resistor to nominally 5.5k (the same value we used before, see Fig. 20.22 and the associated discussion) and adjust the widths and lengths of the NMOS devices until the simulations show good temperature behavior (keeping in mind that we must keep the W/L of M2 $K$ times the W/L of M1). The resulting circuit is seen in Fig. 23.13. Simulation results are seen in Fig. 23.14. (Note that the currents and gate-source voltages have nothing to do with the values listed in Table 9.2.) The reference voltage is nominally 500 mV (= *VDD*/2). The reference, according to simulations, moves 40 mV over a 100 °C temperature change (–400 μV/C or a TC of –800 ppm/C, not that great when compared to the references described later). Further, the reference is fairly insensitive to variations in *VDD* once *VDD* gets above 600 mV.

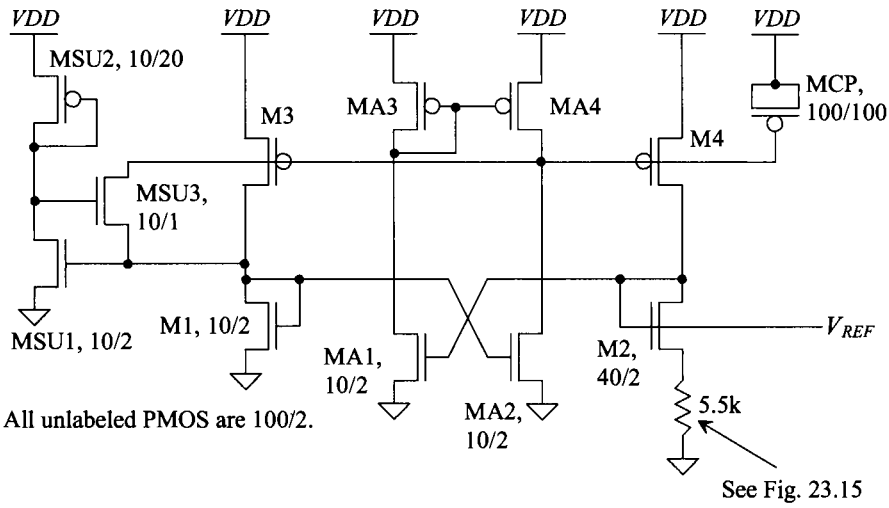



**Figure 23.13** Voltage reference using the beta-multiplier.

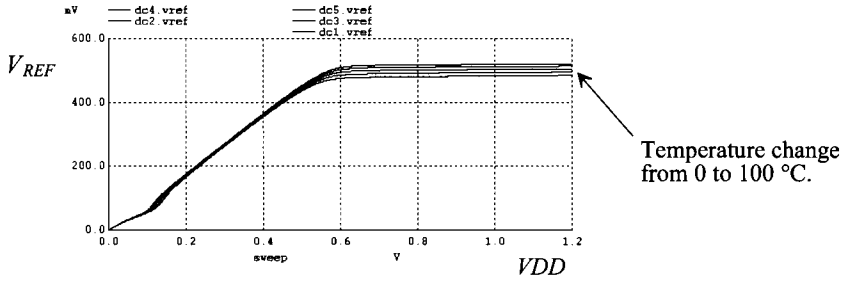



**Figure 23.14** Simulating the operation of the reference in Fig. 23.13.

A couple of practical notes are needed at this point. While we've used simulations to zero in on a design with decent temperature behavior and a reference voltage at *VDD*/2, actually fabricating this reference would result in a $V_{REF}$ different from the one seen in Fig. 23.14 (in most fabrication runs). The MOSFET characteristics and the sheet resistance vary with each process run.

To adjust the reference voltage to *VDD*/2, the resistor must be trimmed using fuses, Fig. 23.15. It can be shown that the temperature behavior doesn't vary significantly with small changes in $V_{REF}$ when trimming. As seen in Eq. (20.38), lowering the resistor value causes $V_{REF}$ to increase, while increasing the resistor value causes $V_{REF}$ to decrease. The fuses in Fig. 23.15 short across the resistor until they are blown. To trim the resistor, we start blowing the resistors (electrically or with a laser). With each blown fuse we add (nominally) 200 Ω in series with the nominally 4k resistor. If the processes' sheet resistance increases by 20% (so that the resistors are now 4.8k and 240 Ω), then we only need to blow three fuses (neglecting the change in the MOSFET characteristics) to trim the resistor to 5.5k. If the sheet resistance decreases by 20%, then the resistors are 3.2k and 160 Ω. Fifteen fuses would need to be blown to trim the resistor to 5.5k.

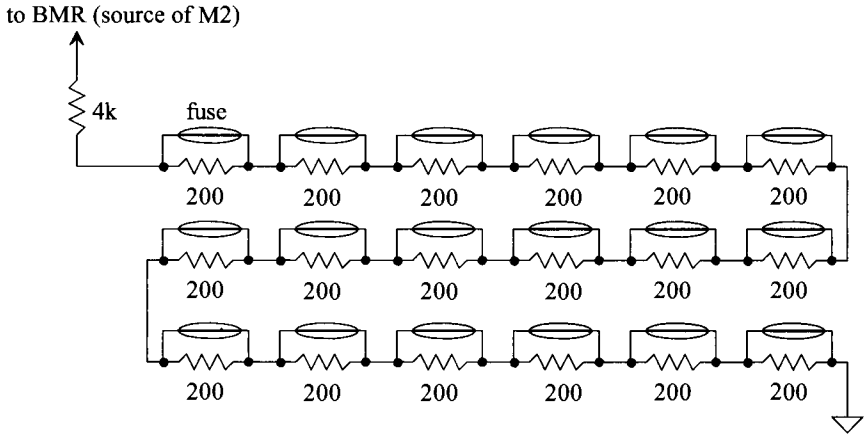
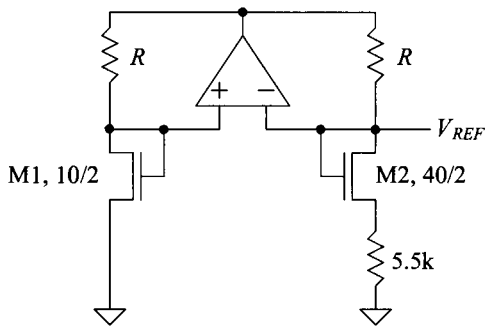



**Figure 23.15** Trimming a resistor with fuses.

Finally, it's important to remember that stability is of great importance when using feedback. As discussed in Sec. 20.1.4, the feedback loop is made stable by adding a capacitance on the output of the added amplifier. The bigger this capacitance, the more stable the reference. We stabilize the reference in Fig. 23.13 with the addition of MCP. ■

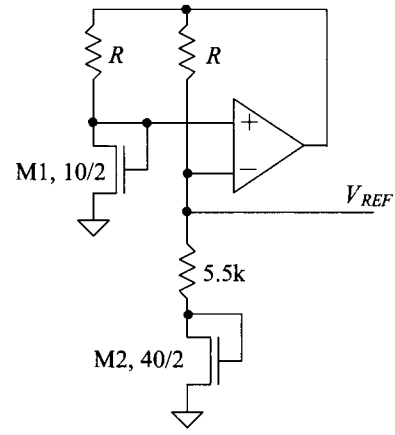
*An Alternate Topology*

Instead of using PMOS devices in the top of each branch of the reference, we might try holding the voltage across resistors constant to force the current through each branch of the reference to be the same. Figure 23.16 shows the idea drawn two different ways. In (a) the amplifier tries to hold both of its inputs at the same potential. This causes the voltage across each $R$ to be the same and thus each branch of the reference has the same current. Note now we've tied M2 and the resistor (a resistance larger than M1 alone) to the – amplifier input. This is because the inverting PMOS common-source amplifiers (M3 and M4) are no longer in the feedback signal path; we need to ensure that the largest signal is fed back to the inverting amplifier terminal. Note also, in (b), that the series order of the resistor and MOSFET is not important. In fact, having both sources connected to ground eliminates the body-effect mismatch and may result in better temperature performance. We won't use these topologies in any of the MOSFET-resistor topologies in this chapter because the amplifier has to drive a resistive load (which, as we saw in Chs. 22 and 23, kills the amplifier's gain). A two-stage op-amp, discussed in the next chapter, can be used. However, then we have to be concerned with compensating the op-amp. Finally, note that a start-up circuit is still needed with these topologies. The start-up circuit would leak current into the node connected to the + amplifier input to start the reference circuit up (and then shut off after the reference turns on). Connecting the start-up circuit to the – amplifier input would move the amplifier output in the wrong direction and the reference would never start up (noting in Figs. 23.7 and 23.13 that we do connect the start-up circuit to the – input because M3 and M4 are inverting amplifiers).




(a) Holding the voltage across resistors to force the same current through each branch of the reference.

Note start-up circuit not shown (see text).




(b) Redrawing (a) and switching the places of the resistor and M2.

**Figure 23.16** Other references useful in MOSFET-resistor circuits.

## 23.2 Parasitic Diode-Based References

By using a junction diode, the variability encountered in the references of the last section that used a MOSFET's threshold voltage can be reduced. One practical implementation of a parasitic diode available in CMOS is seen in Fig. 23.17. A diode is formed between the p+ implant and the n-well. However, in a practical circuit the parasitic vertical PNP bipolar device formed by the p+, n-well, and p-substrate causes current to be injected into the substrate. Good guard rings are used to surround the p+ in both the n-well and the p-substrate to collect this current. This ensures that the injected carriers are collected and not causing substrate current to flow in other portions of the chip. Because the substrate is connected to ground, the diode's cathode (K) must be tied to ground. We might try to use an n+ implant directly in the substrate for diode formation. However, assuming the substrate (which forms the anode of the resulting diode) is grounded, we would have to apply a negative voltage to the n+ (K) to forward-bias the diode. One other practical parasitic diode available in CMOS is made using the lateral PNP device seen in Fig. 23.18. In this device, the p+ forms the emitter/collector of the resulting device (the n-well is the base). However, the vertical PNP (and the resulting substrate current) is still present. A significant portion of the lateral PNP's emitter current will flow into the substrate. In the following example, we'll assume vertical PNP (diodes) are used.

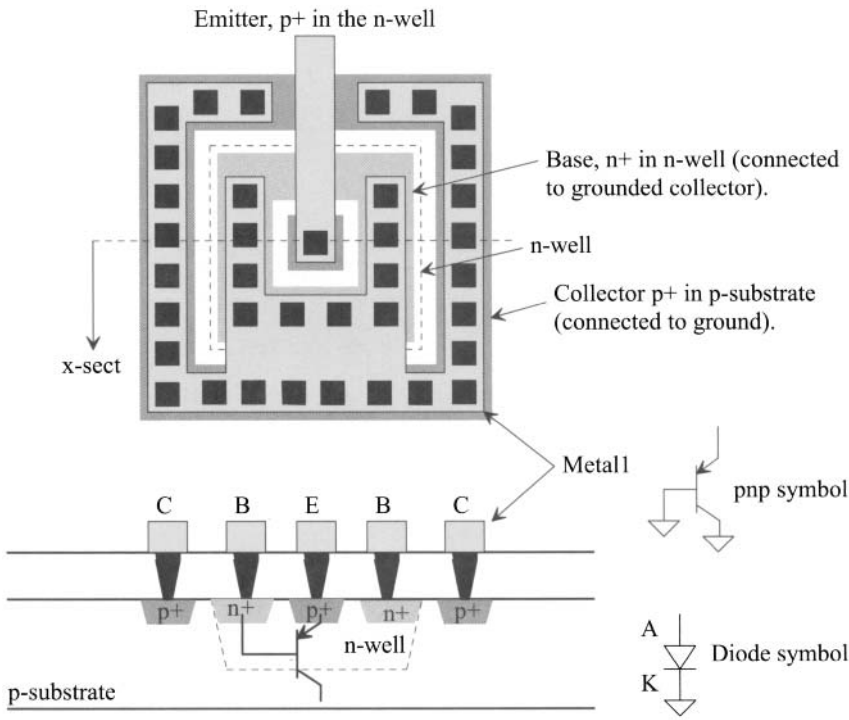



**Figure 23.17** A vertical parasitic pnp bipolar junction transistor used as a diode.

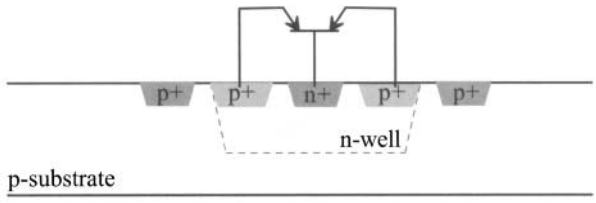



**Figure 23.18** A lateral parasitic bipolar junction transistor.

*Diode Behavior*

It's important to realize that the parasitic diode's behavior must be thoroughly characterized in a particular CMOS process to determine its voltage-current (and temperature) characteristics. For the sake of illustrating design procedures, considerations, and examples in this chapter, we can develop a general diode model. The current through a forward-biased diode is given by

$$I_D = I_S \cdot e^{V_D/n \cdot V_T} \tag{23.19}$$

where $V_D$ is the voltage across the diode, $n$ is the emission coefficient (used to shape the diode's current-voltage curve to fit experimental data), $V_T$ is the thermal voltage ($kT/q$ or 26 mV at room temperature), and $I_S$ is the diode's scale current. Here, we'll use a value of $10^{-18}$ A for the scale current and an $n$ of 1. The SPICE statement corresponding to the schematic seen in Fig. 23.19 is

```
D1    1    0    PNPDIODE
D2    2    0    PNPDIODE    4
```

where the 4 indicates 4 diodes are connected in parallel. We may use, in schematics drawn in later in the chapter, the term $K$ to indicate $K$ diodes are connected in parallel. The model statement for the diode, using the parameters seen above, is

```
.MODEL      PNPDIODE    D      is=1e-18      n=1
```

Figure 23.20 shows how the voltage across the diode changes if the current through the diode is held constant and the temperature is changed. Using our model ($n$ =1 and $I_S$ =

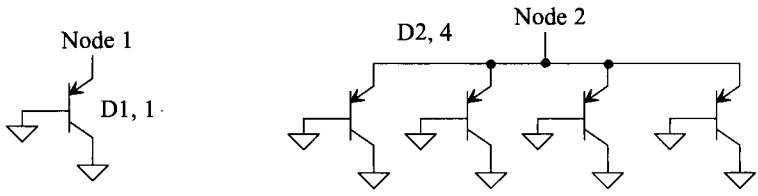



**Figure 23.19** A schematic of diodes.

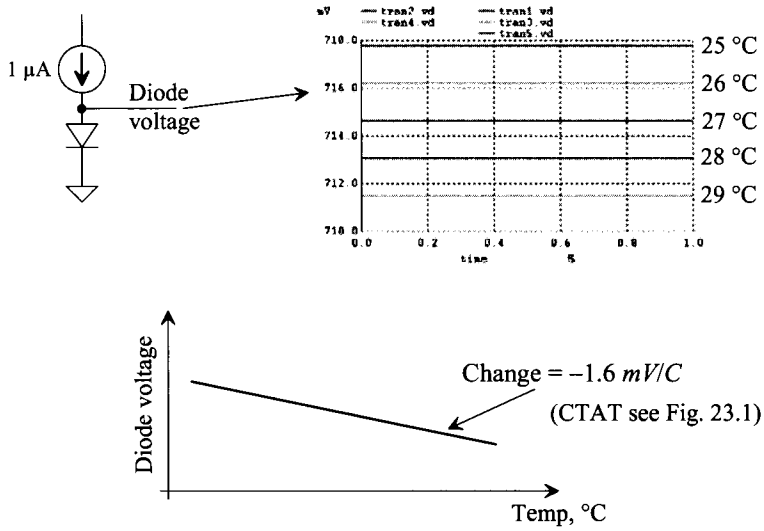



**Figure 23.20** Change in diode voltage with temperature.

$10^{-18}$), we can estimate the change in the diode's voltage with temperature, from the simulation data, as

$$\frac{dV_D}{dT} = -1.6\ mV/C \tag{23.20}$$

noting that this number is very dependent on the DC current through the diode. (Also note this voltage change is complementary to absolute temperature, CTAT.) Increasing the bias current in Fig. 23.20 to 10 μA, causes the diode's voltage drop to increase (of course) and its voltage change with temperature to become −1.4 *mV/C*.

*The Bandgap Energy of Silicon*

The silicon bandgap energy as a function of temperature is given by

$$E_g(T) = 1.16 - (702 \times 10^{-6}) \cdot \frac{T^2}{T + 1108}\ (\text{eV}) \tag{23.21}$$

At room temperature, the bandgap of silicon is approximately 1.1 eV (where 1 electron-volt, eV, is $1.6 \times 10^{-19}$ J). Looking at Eq. (23.21), notice that the bandgap energy decreases with increasing temperature. If we put a constant current through a diode and increase the temperature, the barrier height between the n and p sides of the diode decreases and thus so does the diode's voltage drop (and that is why the diode's voltage change with temperature in Fig. 23.20 is negative).

In the next two sections we'll talk about *BandGap References* (BGR). BGR's combine the CTAT behavior of the bandgap of silicon (the diode's forward voltage drop) with the PTAT behavior of the thermal voltage (the thermal voltage, $kT/q$ , increases with increasing temperature see Fig. 23.1) to form a voltage reference (a BGR) that doesn't vary (much) with temperature.

*Lower Voltage Reference Design*

While, at the time of this writing, power supply voltages are well above the forward turn-on voltage of the pn junction diode (parasitic PNP device), it is clear that the near future will bring *VDD* voltages below 0.7 V. To implement a reference in these lower supply voltage processes, consider the Schottky diode layout of Fig. 23.21. In this layout, we connect the metal (the anode) directly to the n-well (that is, without the p+) to form the Schottky diode. To connect the metal directly to the substrate, we need an opening in the oxide. To form this opening, we use the "active" layer without the select layer (without the implant). It's important that no select layer surrounds this Schottky contact.

The turn-on voltage of a Schottky contact is considerably lower than a standard pn junction. In Fig. 23.21 we draw the turn on voltage as 300 mV. In real silicon this voltage will depend highly on the doping of the n-well (which, as we saw in Ch. 6, scales up as process dimensions shrink). The design discussions and procedures developed in the next two sections can be applied to Schottky diode-based references. Again, though, thorough characterization of the parasitic diode is required prior to designing the reference. One concern, among others, is the repeatability of the diode's current-voltage characteristics from one process run to the next. We don't discuss Schottky diode-based references any further in this chapter, but, rather, leave it to the refereed literature.

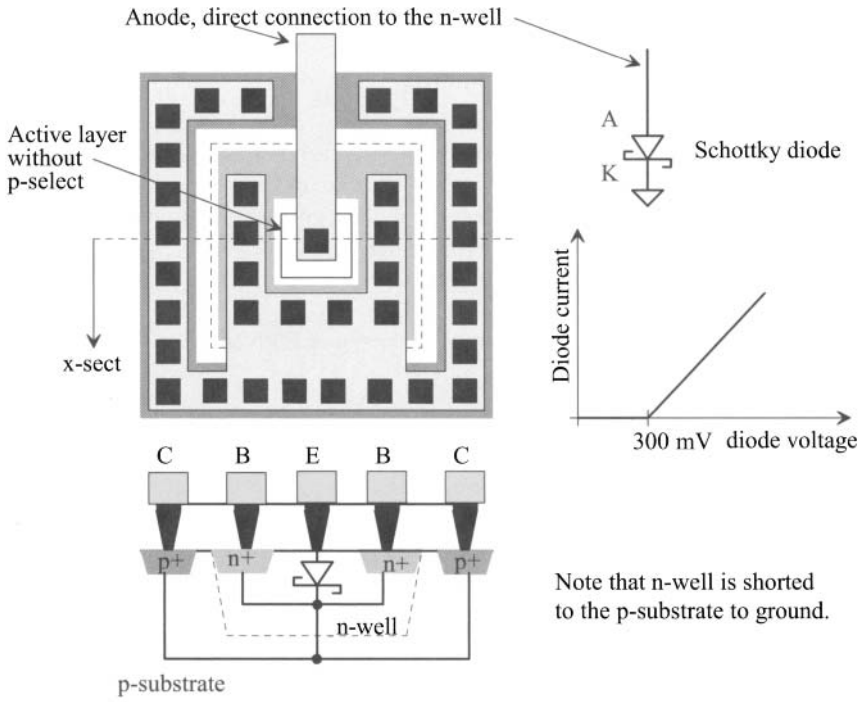



**Figure 23.21** Connecting metal directly to n-well to make a Schottky diode.

### 23.2.1 Long-Channel BGR Design

In this section we present some long-channel designs for bandgap references (BGR) using the cascode structure seen in Fig. 23.11. We will not show the (**required**) start-up circuit in the following schematics.

*Diode-Referenced Self-Biasing (CTAT)*

A diode-referenced, self-biasing circuit is seen in Fig. 23.22. The cascode structures force the same current through each branch of the reference. The voltage across the resistor now equals the forward voltage drop of the diode. The current in the circuit (the current flowing in each branch of the reference) is then

$$I_{REF} = \frac{V_D}{R} = I_S e^{V_D/nV_T} \tag{23.22}$$

Solving for a resistor to set the reference current level gives

$$R = \frac{nV_T}{I} \ln \frac{I}{I_S} \tag{23.23}$$

To determine the reference current's variation with temperature, we can write

$$\frac{\partial I_{REF}}{\partial T} = \frac{\partial}{\partial T}\left(\frac{V_D}{R}\right) = \frac{1}{R} \cdot \overbrace{\frac{\partial V_D}{\partial T}}^{\text{change in } V_D \text{ with } T} - \overbrace{\frac{V_D}{R^2}\frac{\partial R}{\partial T}}^{\text{TC of the resistor}} \tag{23.24}$$

Remembering that the overall current change with temperature is written as

$$I_{REF}(T) = I_{REF}(T_0) \cdot (1 + TCI_{REF}(T - T_0)) \tag{23.25}$$

Start-up circuit not shown.
NMOS are 10/2.
PMOS are 30/2.
Scale factor is 1 micron.

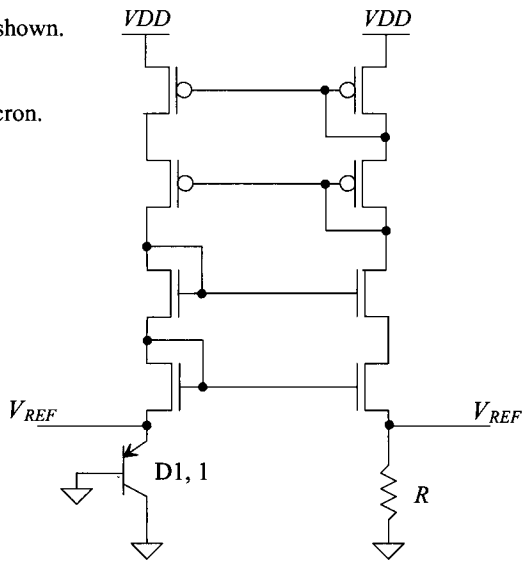



**Figure 23.22** Diode-referenced, self-biasing circuit.

where

$$TCI_{REF} = \frac{1}{I_{REF}} \cdot \frac{\partial I_{REF}}{\partial T} \tag{23.26}$$

we can, with the help of Eq. (23.24), write

$$\frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial T} = \frac{1}{V_D} \frac{\partial V_D}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \tag{23.27}$$

The behavior of the diode-referenced, self-biased circuit shows a large negative coefficient. If the TC of the resistor is 0.002 and the change in the diode voltage with $T$ (Eq. (23.20)) is –0.0016 (or if the diode voltage, $V_D$, is nominally 0.7, the first term in Eq. (23.27) is –0.0023), then the overall TC of the current is, roughly, –0.004 or –4,000 ppm/C. If we were to use the voltage across the diode (or resistor) as a voltage reference, the fact that the current through the diode is decreasing with increasing temperature (causing the diode's voltage to drop) and the bandgap of silicon is decreasing with increasing temperature, causes $V_D$ to drop (relatively quickly) with increasing temperature (CTAT). Consider the following example.

**Example 23.4**

Simulate the operation of the reference in Fig. 23.22 where the voltage across the diode is used as a reference voltage. Use a nominal reference current of 1 μA.

Using Eq. (23.23), we can set $R$ to 700k. The simulation results are seen in Fig. 23.23. The reference voltage change is essentially set by the decrease in the diode voltage with increasing temperature, that is, –1.6 mV/C. At the risk of stating the obvious, this isn't a very good voltage reference. ■

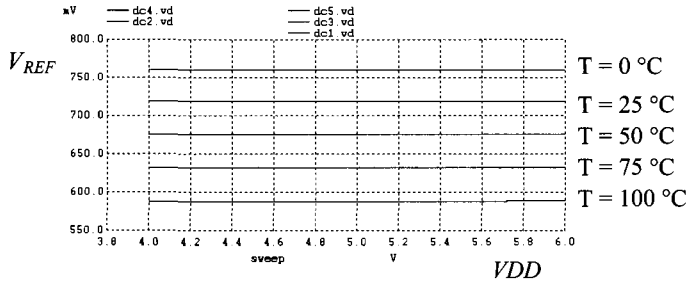



**Figure 23.23** Temperature behavior of the diode-referenced circuit of Fig. 23.22. See Ex. 23.4.

*Thermal Voltage-Referenced Self-Biasing (PTAT)*

A thermal voltage, $V_T$, referenced, self-biasing circuit is seen in Fig. 23.24. In this configuration the voltage across D1 must equal the voltage across D2 and the resistor

$$V_{D1} = V_{D2} + I_{D2}R \tag{23.28}$$

Notice that D2 must be larger than D1 if the current flowing in the reference is to be nonzero. The larger D2 will drop a smaller voltage than D1 for the same current through each branch. As indicated in Eq. (23.28), the difference in the diode voltages is dropped

Start-up circuit not shown.
NMOS are 10/2.
PMOS are 30/2.
Scale factor is 1 micron.

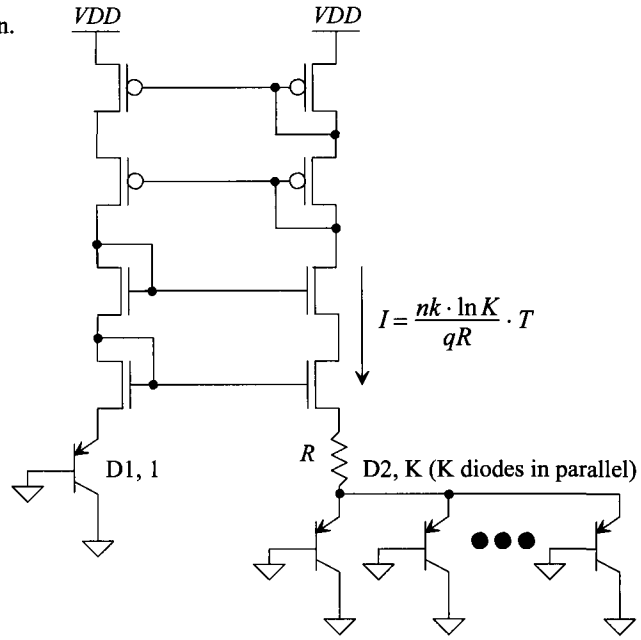



**Figure 23.24** Thermal voltage-referenced, self-biasing circuit.

across $R$. Alternatively, we could size the diodes the same and increase the current flowing in the left branch of the reference by making the MOSFETs $K$ times wider. The current in the left branch would be $K$ times more than the current in the right branch of the reference.

We know

$$I_{D1} = I_S e^{V_{D1}/nV_T} \rightarrow V_{D1} = nV_T \cdot \ln \frac{I_{D1}}{I_S} \tag{23.29}$$

and

$$I_{D2} = K \cdot I_S e^{V_{D2}/nV_T} \rightarrow V_{D2} = nV_T \cdot \ln \frac{I_{D2}}{K \cdot I_S} \tag{23.30}$$

Knowing, because of the cascode structures, $I_{D1} = I_{D2} = I$, we can write

$$R = \frac{nV_T \cdot \ln K}{I} \text{ or } I = \frac{nk \cdot \ln K}{qR} \cdot T \tag{23.31}$$

Notice that the current is proportional to absolute temperature (PTAT). To get a voltage reference that is also PTAT, consider the reference seen in Fig. 23.25. Here the reference voltage is given by

$$V_{REF} = I \cdot L \cdot R = \frac{nk \cdot L \cdot \ln K}{q} \cdot T \tag{23.32}$$

Notice how the temperature behavior of the resistor falls out of the equation.

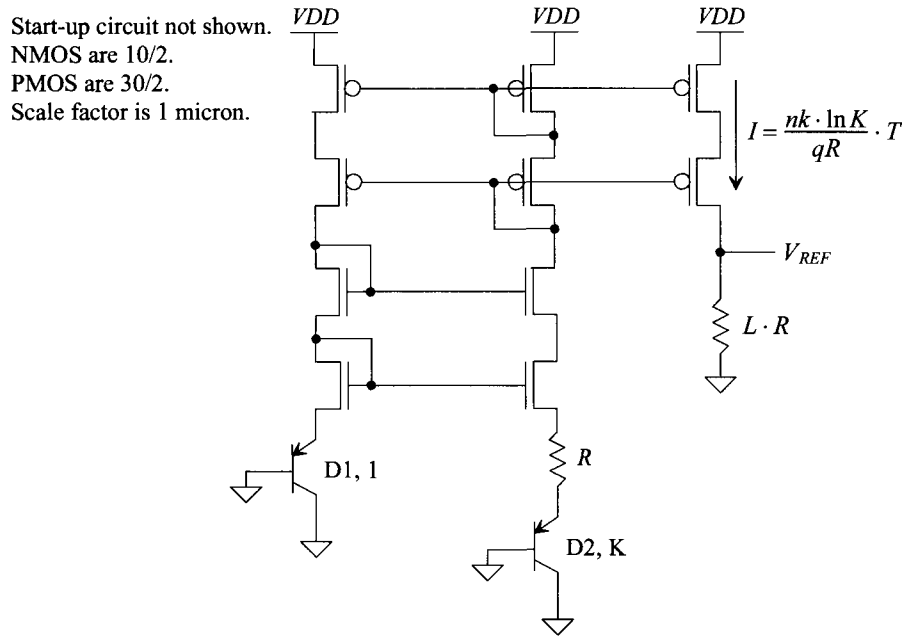



**Figure 23.25** PTAT voltage reference based on the thermal voltage-referenced, self-biased circuit.

**Example 23.5**

Design a nominally 2.500 V voltage reference (at room temperature of 27 °C or 300 °K) PTAT voltage reference. Use the topology seen in Fig. 23.25 with a bias current of 1 μA. Simulate the operation of the design.

Let's set $K$ (the number of diodes connected in parallel) to 8. We do this since it is easy to remember ln 8 = 2. Solving for $R$ using Eq. (23.31) gives

$$R = \frac{1 \cdot 0.026 \cdot 2}{10^{-6}} = 52k$$

The voltage drop across the resistor is $1\ \mu A \cdot 52k = 52\ mV$. Using Eq. (23.32), we can solve for $L$ as 48 (so $L \cdot R = 2.5\ M\Omega$). The simulation results are seen in Fig. 23.26. At room temperature, the reference voltage is roughly 2.5 V. Note how, as temperature increases, the reference voltage (PTAT) increases. Using Eq. (23.32), we can estimate the reference voltage's change with temperature as

$$\frac{\partial V_{REF}}{\partial T} = \frac{nk \cdot L \cdot \ln K}{q} \tag{23.33}$$

Using the numbers from this example with $k = 1.38 \times 10^{-23} J/K$ and $q = 1.6 \times 10^{-19} C$ gives

$$\frac{\partial V_{REF}}{\partial T} = \frac{1 \cdot 1.38 \cdot 10^{-23} \cdot 48 \cdot 2}{1.6 \times 10^{-19}} = 8.26\ mV/C$$

For every 25 °C increase in temperature, we expect $V_{REF}$ to go up by 206 mV. ■

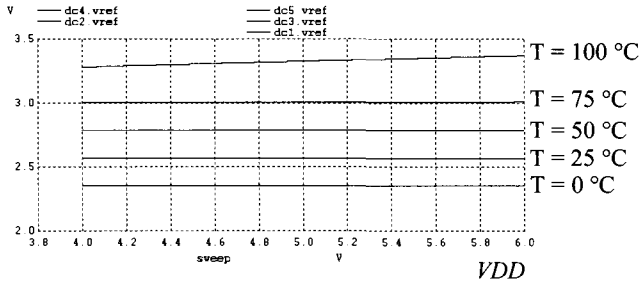



**Figure 23.26** A PTAT voltage reference. See Ex. 23.5.

*Bandgap Reference Design*

The bandgap reference (BGR) is formed using CTAT and PTAT references. When designed properly, the TC of the BGR can be very small. Figure 23.27 shows a schematic of a BGR. The PTAT current generated from the circuit in Fig. 23.24 is driven into a resistive load (to give a PTAT voltage drop, see Eq. (23.32)) and a diode (to give a CTAT voltage drop, see Eq. (23.20)). The reference voltage is then the sum of the PTAT and CTAT voltage drops or

$$V_{REF} = V_{D3} + I \cdot L \cdot R = V_{D3} + L \cdot n \cdot \ln K \cdot V_T \qquad (23.34)$$

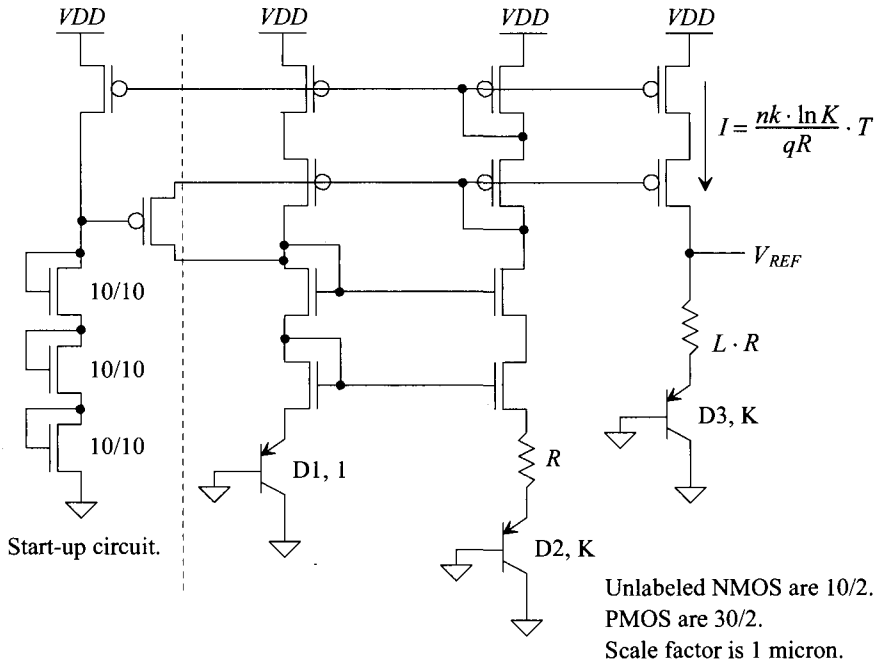



**Figure 23.27** A bandgap reference circuit.

The change in the reference voltage with temperature is

$$\frac{\partial V_{REF}}{\partial T} = \overbrace{\frac{\partial V_{D3}}{\partial T}}^{-1.6\,mV/C} + L \cdot n \cdot \ln K \cdot \overbrace{\frac{\partial V_T}{\partial T}}^{0.085\,mV/C} \tag{23.35}$$

where the change in the thermal voltage with temperature was taken from Eq. (9.44). To determine the value of $L$ that causes the change in $V_{REF}$ with temperature to go to zero, we set Eq. (23.35) to zero and solve

$$L = \frac{1.6}{n \cdot \ln K \cdot 0.085} \tag{23.36}$$

If $K = 8$ and $n = 1$, then $L = 9.41$. Using Eq. (23.34) with these values, gives a $V_{REF}$ of 1.2V. Figure 23.28 shows the simulation results using these values and the schematic seen in Fig. 23.27. The start-up circuit causes the reference to turn on at a *VDD* of approximately 3V. The change in the reference voltage with temperature is roughly 1.5 mV per 75 °C or 20 μV/C. The TC of the reference, Eq. (23.3), is then 16.7 ppm/C. At higher temperatures the variation in $V_{REF}$ (with *VDD*) is slightly poorer likely due to not keeping the currents in each branch equal. Note that if a precise voltage is needed, trimming the $L \cdot R$ resistor (see Fig. 23.15 and the associated discussion) is required.

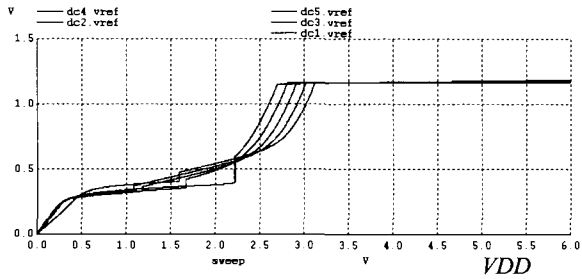
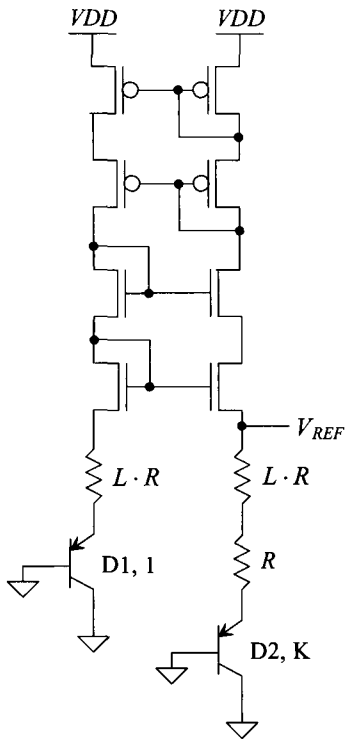



**Figure 23.28** Simulating the BGR in Fig. 23.27 from 0 to 100 C.

*Alternative BGR Topologies*

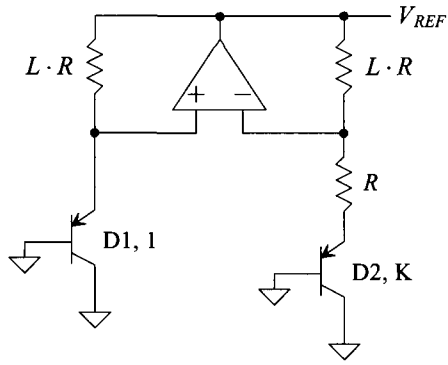
We might wonder if there is a way to simplify the BGR of Fig. 23.27 to reduce power and layout area. Figure 23.29a shows one possibility. In this circuit we've combined the three branches in Fig. 23.27 into two branches. The same voltage, as in Fig. 23.25, is dropped across the single resistor $R$. The $L \cdot R$ resistors are a common element to both branches. The current is still PTAT, while the reference voltage at the top of the $L \cdot R$ resistor is still a bandgap voltage. The drawback of this topology is the fact that the minimum value of *VDD* for proper reference operation increases.

Figure 23.29b shows a topology based on the configuration, using resistors, seen in Fig. 23.16. As with all of the topologies in this chapter (again), the point of the added amplifier is to force the same current through each side of the reference. The benefit of this topology over the topology in (a) is that *VDD* can move lower before it affects $V_{REF}$. The drawback of this topology is that the amplifier must be capable of driving a resistive load (which we'll see in the next chapter requires two gain stages for the amplifier's overall gain to be reasonably high). In (c) PMOS devices are added to isolate the

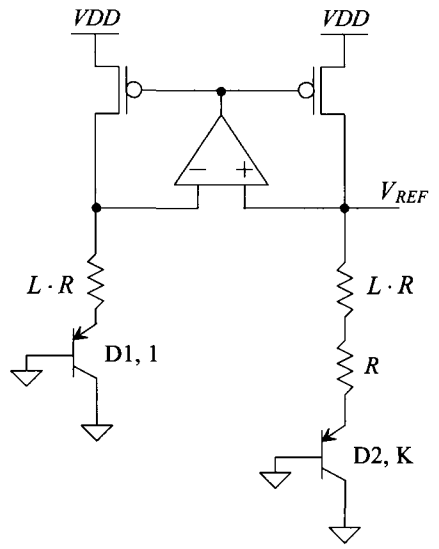



(a) Alternative BGR using cascodes.

Note: start-up circuits (required) not shown.




(b) Using an amplifier to force the same current through each branch of the reference, see Fig. 23.16.




(c) Using PMOS devices to isolate the amplifier from the resistive loading.

**Figure 23.29** Alternative BGR topologies.

amplifier's output from the resistors. This makes using a diff-amp for the added amplifier possible. The currents are equal in (c) because the source-gate voltages of the PMOS devices are equal. Note how the branch containing D2 is a higher resistance (than the branch containing D1) and so it (the D2 branch) is always connected to an inverting point in the feedback loop. As seen in (c) the addition of the PMOS devices (which are inverting) means that we need to switch the inverting and noninverting amplifier inputs from (b). Finally, note that a start-up circuit is required for all three of these references.

### 23.2.2 Short-Channel BGR Design

The bandgap reference voltage of 1.2 V developed in the last section is greater than *VDD* (= 1 V) in our short-channel process. To develop a BGR for short-channel processes, consider the schematic seen in Fig. 23.30. The diodes D1 and D2 together with the resistor, *R*, form a PTAT current generator, as seen in Fig. 23.24. To provide a CTAT current to sum with the PTAT current, consider the addition of the $L \cdot R$ resistors, as seen in the schematic. As temperature increases, the diode voltage decreases, causing the current through the $L \cdot R$ resistors to decrease (CTAT). We know that the current due to the PTAT portion of the circuit, see Eq. (23.31), is

$$I_{PTAT} = \frac{nV_T \cdot \ln K}{R} \tag{23.37}$$

The current through the added resistors (the CTAT portion of the circuit) is

$$I_{CTAT} = \frac{V_{D1}}{L \cdot R} \tag{23.38}$$

The total current is driven through the $N \cdot R$ to generate the reference voltage

$$V_{REF} = nV_T \cdot N \cdot \ln K + \frac{N}{L} \cdot V_{D1} \tag{23.39}$$

The temperature behavior of the BGR is

$$\frac{\partial V_{REF}}{\partial T} = n \cdot N \cdot \ln K \cdot \overbrace{\frac{\partial V_T}{\partial T}}^{0.085\ mV/C} + \frac{N}{L} \cdot \overbrace{\frac{\partial V_{D1}}{\partial T}}^{-1.6\ mV/C} \tag{23.40}$$

For zero TC, we get an *L* of

$$L = \frac{1.6}{n \cdot \ln K \cdot 0.085} \tag{23.41}$$

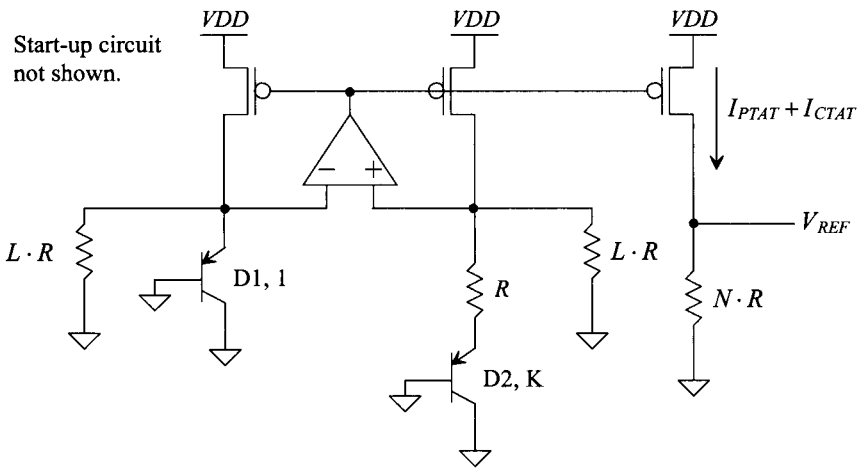
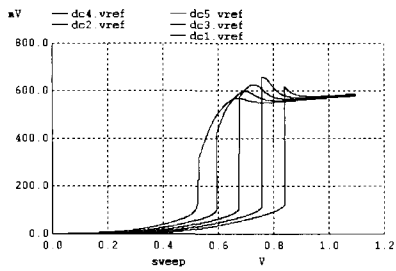



**Figure 23.30** Lower voltage BGR.

Using a $K$ of 8 results in, again, an $L$ of 9.41. To get a particular reference voltage, we use Eq. (23.39) to determine $N$. For example, if we want a reference voltage of 500 mV (half of $VDD$), we get an $N$ of (using a $K$ of 8)

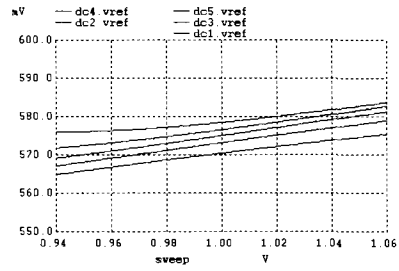
$$N = \frac{V_{REF}}{nV_T \cdot \ln K + \frac{V_{D1}}{L}} = \frac{0.5}{0.052 + \frac{0.7}{9.41}} = 3.91 \qquad (23.42)$$

Figure 23.31 shows some simulation results using these numbers (the schematic of the full design is seen in Fig. 23.32). In (a) the reference turns on at a $VDD$ of approximately 900 mV. The temperature behavior of the reference is seen in (b). Notice that the reference voltage is higher than what we designed for. In all practical situations, the $N \cdot R$ resistor (the 205k resistor in Fig. 23.32) would need trimming (see Fig. 23.15) to set the reference voltage to a precise value.




*VDD*

(a) The BGR turns on at 900 mV.




*VDD*

(b) Close-up temperature behavior.

**Figure 23.31** Simulating the behavior of the reference in Fig. 23.30.

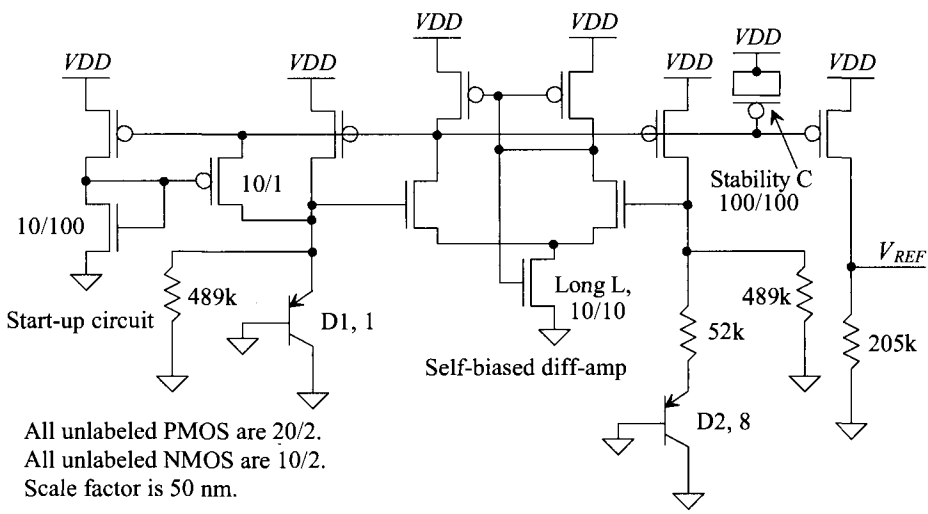



**Figure 23.32** Lower voltage BGR used to generate the simulation data seen in Fig. 23.31.

*The Added Amplifier*

In Fig. 23.32 we used a self-biased amplifier (see Fig. 18.17) to hold the voltage across D1 to the same value as the voltage across the 52k resistor and D2. This amplifier is critical for good BGR performance. For example, notice how the reference voltage in Fig. 23.31b varies with changes in *VDD*. By using a higher-gain amplifier, we can reduce this variation. While we'll discuss op-amp design in detail in the next chapter, one concern is the added amplifier's input common-mode voltage. Because the forward voltage drop of the diodes is approximately 0.7 V (a significant percentage of *VDD*), the performance (gain) of the amplifier may drop if any of the MOSFETs in the diff-amp triode or shut off. To lower the input common-mode voltage, consider the topology of Fig. 23.33. Here we set

$$R_1 + R_2 = L \cdot R \tag{23.43}$$

The amplifier sets the voltages across each $R_2$ to the same value and so the current flowing in $R_1$ and $R_2$ is the same as in Fig. 23.30, provided Eq. (23.43) is satisfied. The big benefit of using the topology is that the DC input common-mode voltage of the added amplifier can be reduced.

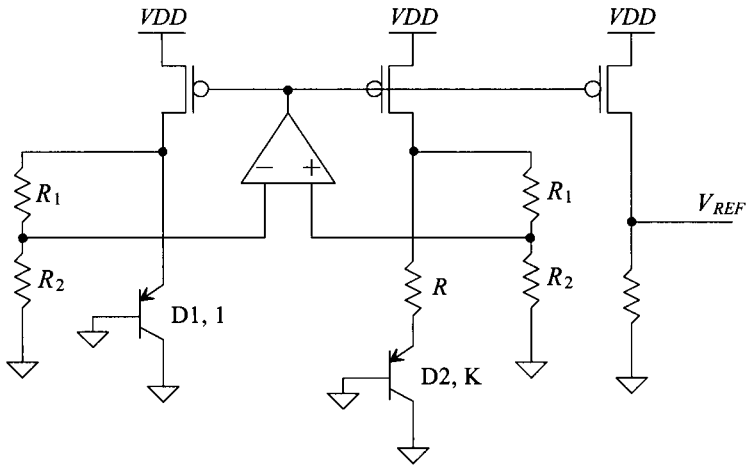



**Figure 23.33** Lowering the input common-mode range of the added amplifier.

*Lower Voltage Operation*

Fundamentally, the limitation on how low *VDD* can be in the BGR reference of Fig. 23.30 (or 23.33) is the forward voltage drop of the diodes. As the dimensions of CMOS technology continue to scale downwards, so does *VDD*. While the MOSFET-resistor references, such as the beta-multiplier reference (BMR), discussed in the first section of this chapter may provide a solution to many reference circuit needs at lower *VDD*s, it is unlikely that they will replace the BGR in all applications. Even though both the BMR and BGR require trimming to set $V_{REF}$, the temperature performance of the BGR is, in general, better than that of the BMR. What may happen is that the pn junction used in the BGR is replaced by a junction with a lower built-in potential (and thus lower forward turn-on voltage) like the Schottky diode (see Fig. 23.21).

## ADDITIONAL READING

[1] K. N. Leung and P. K. T. Mok, "A Sub-1-V 15-ppm/C CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Device," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 4, April 2002, pp. 526–530. Develops the scheme seen in Fig. 23.33 for lowering the input common-mode range of the added amplifier.

[2] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, May 1999, pp. 670–674. Presents the design of the lower voltage BGR seen in Fig. 23.30.

[3] G. Tzanateas, C. A. T. Salama, and Y. P. Tsividis, "A CMOS Bandgap Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. SC-13, no. 3, June 1979, pp. 655–657. Good paper discussing BGR reference design.

[4] E. Vittoz and J. Fellrath, "CMOS Analog Integrated Circuits Based on Weak Inversion Operation," *IEEE Journal of Solid-State Circuits*, vol. SC-12, no. 3, June 1977, pp. 224–231. Covers the BMR design operating in the weak inversion region.

[5] K. E. Kuijk, "A Precision Reference Voltage Source," *IEEE Journal of Solid-State Circuits*, vol. SC-8, no. 3, June 1973, pp. 222–226. Development of the BGR seen in Fig. 23.29b.

## PROBLEMS

**23.1** Using the MOSFET-only reference seen in Fig. 23.2, design a nominally 500 mV reference in the short-channel CMOS process. Using simulations, characterize the sensitivity of the reference voltage to changes in *VDD* and temperature.

**23.2** Use the long-channel CMOS process and the topology seen in Fig. 23.6 to design a voltage reference of $3V_{THN}$. Simulate your design and show the *VDD* sensitivity and temperature behavior of the reference. Do TCs of $R_1$ and $R_2$ affect the performance of the reference? Why or why not?

**23.3** Suppose it was desired, in Fig. 23.7 (see also Fig. 20.22), to make M1 and M2 the same size. However, to increase the gate source voltage of M1, relative to M2, the width of M3 is increased by *K*. How do the equations governing the operation of the BMR change? How does the current flowing in the BMR change?

**23.4** Verify that if the PMOS devices in Fig. 23.11 are not cascoded (that is, they have only NMOS cascodes), the currents in each branch will not be equal and there will be significant sensitivity to *VDD* (a sensitivity similar to what is seen in Fig. 23.10).

**23.5** In a CMOS process, several of the layers including poly, n+, p+, and n-well can be used for resistor formation. Each of these layers has a different temperature coefficient (TC). For the BMR that generated Fig. 23.14, use simulations to determine the optimum resistor TC.

**23.6** Derive the equations that govern the operation of the reference in Fig. 23.16b.

**23.7** Show why n+ directly in the p-substrate cannot be used as a diode in a CMOS process.

**23.8** Generate a diode model that produces a forward voltage drop of 700 mV when driven with 1 μA and has a change with temperature, $dV_D/dT$, near room temperature, of −2 mV/C. Use simulations to verify your model meets the requirements.

**23.9** Generate a SPICE model for the Schottky diode seen in Fig. 23.21. Assume that the series resistance of the diode is 1 kΩ.

**23.10** Estimate, using hand calculations, the minimum allowable *VDD* for the reference of Ex. 23.4. What are the PMOS and NMOS gate-source and drain-source voltages when the reference current is 1 μA? Note that the parameters in Table 9.1 have nothing to do with the operating conditions in this question. Verify your answers using SPICE.

**23.11** Show that $K$ forward-biased diodes in parallel behave like a single diode with a scale current of $K \cdot I_S$, as assumed in Eq. (23.30).

**23.12** Suggest a reference design that would output a voltage of $n \cdot V_T$.

**23.13** Determine whether the performance of the BGR of Fig. 23.32 can be enhanced by using the topology of Fig. 23.33. Use simulations to verify your answer.