Chapter

25

Dynamic Analog Circuits

In Chapter 14 we discussed dynamic logic gates. Dynamic logic is useful for reducing power dissipation and the number of MOSFETs used to perform a given circuit operation (layout area). Dynamic analog circuits exploit the fact that information can be stored on a capacitor or gate capacitance of a MOSFET for a period of time. In this chapter, we discuss analog circuits such as sample and holds, current mirrors, amplifiers, and filters using dynamic techniques.

25.1 The MOSFET Switch

A fundamental component of any dynamic circuit (analog or digital) is the switch (Fig. 25.1). An important attribute of the switch, in CMOS, is that under DC conditions the gate of the MOSFET does not draw a current. Therefore, neglecting capacitances from the gate to the drain/source, we find that the gate control signal does not interfere with information being passed through the switch. Figure 25.2 shows the small-signal resistance of the switches of Fig. 25.1 plotted against input voltage. The benefits of using the CMOS transmission gate are seen from this figure, namely, lower overall resistance. Another benefit of using the CMOS TG is that it can pass a logic high or a logic low without a threshold voltage drop. The largest voltage that an NMOS switch can pass is $VDD - V_{THN}$, while the lowest voltage a PMOS switch can pass is V_{THP}.

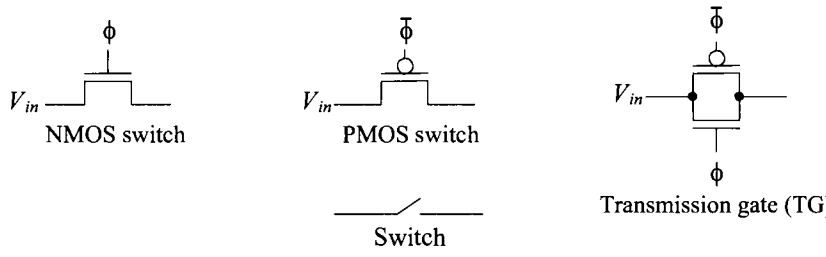

Figure 25.1 MOSFETs used as switches.

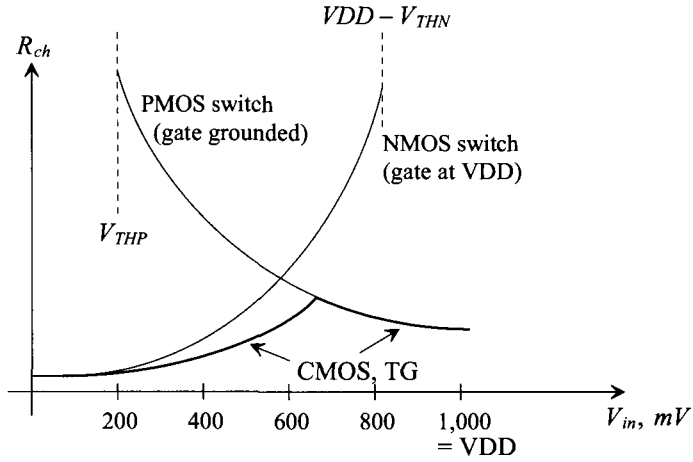

Figure 25.2 Small-signal on-resistance of MOSFET switches.

While MOS switches may offer substantial benefits, they are not without some detraction. Two nonideal effects typically associated with these switches may ultimately limit the use of MOS switches in some applications (particularly sampled-data circuits such as data converters). These two effects are known as *charge injection* and *clock feedthrough.*

Charge Injection

Charge injection can be understood with the help of Fig. 25.3. When the MOSFET switch is on and V_{DS} is small, the charge under the gate oxide resulting from the inverted channel is (from Ch. 6) Q'_{ch}. When the MOSFET turns off, this charge is injected onto the capacitor and into V_{in}. Because V_{in} is assumed to be a low-impedance, source-driven node, the injected charge has no effect on this node. However, the charge injected onto C_{load} results in a change in voltage across it. Note that we also have charge injection (in the opposite direction) when we turn the switch on. However, the fact that the input voltage is connected to C_{load} through the channel resistance makes this error unimportant (the voltage across C_{load} charges to V_{in} through the MOSFET's channel resistance).

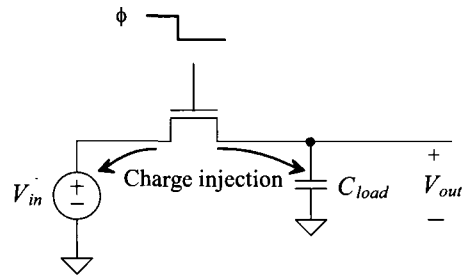

Figure 25.3 Simple configuration using an NMOS switch to show charge injection.

Although the charge injection mechanism is itself a complex one, many studies have sought to characterize and minimize its effects. It has been shown that if the clock signal turns off fast, the channel charge distributes fairly equally between the adjacent nodes. Thus, half of the channel charge is distributed onto C_{load}. From Ch. 6, the charge/unit area of an inverted channel can be approximated as

$$Q_I'(y) = C_{ox}' \cdot (V_{GS} - V_{THN}) \tag{25.1}$$

The total charge in the channel must then be multiplied by the area of the channel resulting in

$$Q_I(y) = C_{ox}' \cdot W \cdot L \cdot (V_{GS} - V_{THN}) \tag{25.2}$$

Therefore, the change in voltage across C_{load} (if an NMOS switch is used) is

$$\Delta V_{load} = -\frac{C_{ox}' \cdot W \cdot L \cdot (V_{GS} - V_{THN})}{2C_{load}} \tag{25.3}$$

which can be written as

$$\Delta V_{load} = -\frac{C_{ox}' \cdot W \cdot L \cdot (VDD - V_{in} - V_{THN})}{2C_{load}} \tag{25.4}$$

if it is assumed that the clock swings between *VDD* and ground. The threshold voltage, Eq. (6.19), can also be substituted into Eq. (25.4) to form

$$\Delta V_{load} = -\frac{C_{ox}' \cdot W \cdot L \cdot (VDD - V_{in} - [V_{THN0} + \gamma(\sqrt{|2V_{fp}| + V_{in}} - \sqrt{|2V_{fp}|})])}{2C_{load}} \tag{25.5}$$

Note that Eq. (25.5) illustrates the problem associated with charge injection. The change in voltage across C_{load} is nonlinear with respect to V_{in} due to the threshold voltage. Thus, it can be said that if the charge injection is signal-dependent, harmonic distortion results. In sampled-data systems, charge injection results in nonlinearity errors. In the case where the charge injection is signal-independent, a simple offset occurs, which is much easier to manage than harmonic distortion. These will be discussed in more detail in Chs. 28 and 29, but it should be obvious here that charge injection effects should be minimized as much as possible.

Capacitive Feedthrough

Consider the schematic of the NMOS switch shown in Fig. 25.4. Here the capacitances between the gate/drain and gate/source of the MOSFET are modeled with the assumption that the MOSFET is operating in the triode region. When the gate clock signal, ϕ, goes high, the clock signal feeds through the gate/drain and gate/source capacitances. However, as the switch turns on, the input signal, V_{in}, is connected to the load capacitor through the NMOS switch. The result is that C_{load} is charged to V_{in} and the capacitive feedthrough has no effect on the final value of V_{out}. However, now consider what happens when the clock signal makes the transition low, that is, the n-channel MOSFET turns off. A capacitive voltage divider exists between the gate-drain (source) capacitance and the load capacitance. As a result, a portion of the clock signal, ϕ, appears across C_{load} as

$$\Delta V_{load} = \frac{C_{overlap} \cdot VDD}{C_{overlap} + C_{load}} \tag{25.6}$$

where $C_{overlap}$ is the overlap capacitance value,

$$C_{overlap} = C'_{ox} \cdot W \cdot LD \tag{25.7}$$

and LD is the length of the gate that overlaps the drain/source.

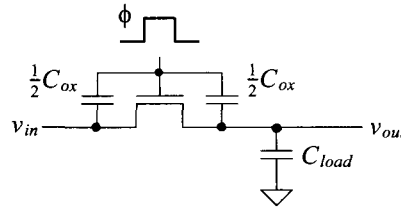

Figure 25.4 Illustration of capacitive feedthrough.

Reduction of Charge Injection and Clock Feedthrough

Many methods have been reported that reduce the effects of charge injection and capacitive feedthrough. One of the most widely used is the dummy switch, as seen in Fig. 25.5. Here, a switch, M2, with its drain and source shorted is placed in series with the desired switch M1. Notice that the clock signal controlling the dummy switch is the complement of the signal controlling M1, and in addition, should also be slightly delayed.

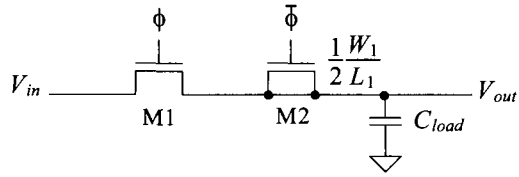

Figure 25.5 Dummy switch circuit used to minimize charge injection.

When M1 turns off, half of the channel charge is injected toward the dummy switch, thus explaining why the size of M2 is one-half that of M1. Although M2 is effectively shorted, a channel can still be induced by applying a voltage on the gate. Therefore, the charge injected by M1 is essentially matched by the charge induced by M2, and the overall charge injection is canceled. Note what happens when M2 turns off. It will inject half of its charge in both directions. However, because the drain and source are shorted and M1 is on, all of the charge from M2 will be injected into the low-impedance, voltage-driven source, which is also charging C_{load}. Therefore, M2's charge injection will not affect the value of voltage on C_{load}.

Another method for counteracting charge injection and clock feedthrough is to replace the switch with a CMOS transmission gate (TG). This results in lower changes in V_{out} because the complementary signals that are used will act to cancel each other.

However, this approach requires precise control on the complementary clocks (the clocks must be switched at exactly the same time) and assumes that the input signal, V_{in}, is small, since the symmetry of the turn-on and turn-off waveforms depend on the input signal.

Fully-differential circuit topologies are used to cancel these effects to a first order, as seen in Fig. 25.6. Since the nonideal charge injection and clock feedthrough effects appear as a common-mode signal to the amplifier, they will be reduced by the CMRR of the amplifier. However, the second-order effects resulting from the input signal amplitude dependence will ultimately limit the dynamic range of operation, neglecting coupled and inherent noise in the dynamic circuits. This subject will be discussed in more detail in the following sections and in the next chapter.

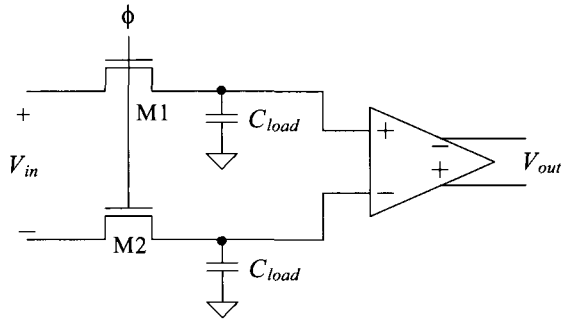

Figure 25.6 Using a fully-differential circuit to minimize charge injection and clock feedthrough.

kT/C Noise

In Ch. 8 we saw that the maximum RMS output noise generated from a simple *RC* circuit was $\sqrt{kT/C}$ (see Table 8.1). If we think of the MOSFET in Fig. 25.7 as a resistor (when the MOSFET is on), then we can add this RMS noise source in series with the output of the capacitor. The noise can be regarded as a sampled (random) voltage onto the capacitor each time the switch is turned on. The RMS noise generated, at room temperature, when using a 1 pF capacitor is 64 μV, while a 100 fF capacitor results in a noise voltage of 200 μV. In other words, the larger the capacitor, the smaller the noise voltage sampled on to the storage capacitor. For high-speed systems, it is desirable to use small capacitors since they take less time to charge. When designing a high-speed and low-noise circuit, trade-offs must be made when selecting the capacitor size.

Note, as mentioned above, the MOSFET is thought of as a resistor (and so *kT/C* noise in the circuit in Fig. 25.7 is from MOSFET thermal noise). If we review the noise mechanisms found in a MOSFET in Ch. 9, we also see that Flicker noise may be present. However, for a MOSFET's drain current to contain Flicker noise, the MOSFET must be conducting a DC current. Because the MOSFET in Fig. 25.7 doesn't conduct any DC current after C_H is charged, Flicker noise doesn't affect the sampled voltage.

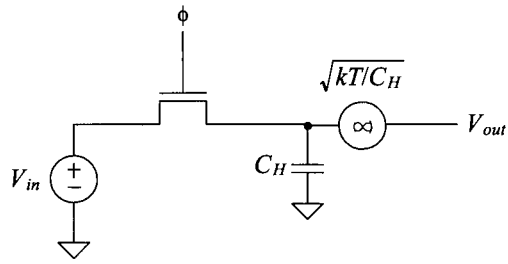

Figure 25.7 How kT/C noise adds to a sampled signal.

25.1.1 Sample-and-Hold Circuits

An important application of the switch is in the sample-and-hold circuit. The sample-and-hold circuit finds extensive use in data converter applications as a sampling gate. A variety of topologies exist, each with their own benefits. The simplest is shown in Fig. 25.8. A narrow pulse is applied to the gate of the MOSFET, enabling v_{in} to charge the hold capacitor, C_H. The width of the strobing gate pulse should allow the capacitor to fully charge before being removed. The op-amp simply acts as a unity gain buffer, isolating the hold capacitor from any external load. This circuit suffers from the clock feedthrough and charge injection problems mentioned in the previous discussion.

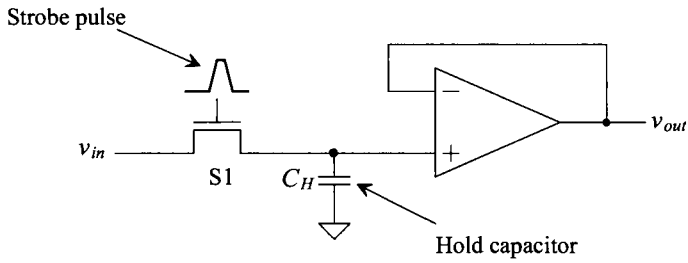

Figure 25.8 A basic sample-and-hold circuit (more correctly called a track-and-hold, see Fig. 28.5b).

A possible improvement in the basic S/H circuit is seen in Fig. 25.9. Here, two amplifiers buffer the input and the output. Notice that switch S_2 ensures that amplifier A1 is stable while in hold mode. If the switch were not present, A1 would be open loop during hold mode and would swing to one of the rails. During the next sample mode, it would then be slew-limited while going from the supply to the value of v_{in}. However, with the addition of S_2, the output of A1 tracks v_{in} even while in hold mode. The switch S_3 also disconnects A1 from the output during hold mode. This S/H has its disadvantages, however. The capacitor is still subjected to charge injection and clock-feedthrough problems. In addition, during sample mode, the circuit may become unstable since there are now two amplifiers in the single-loop feedback structure. Although compensation

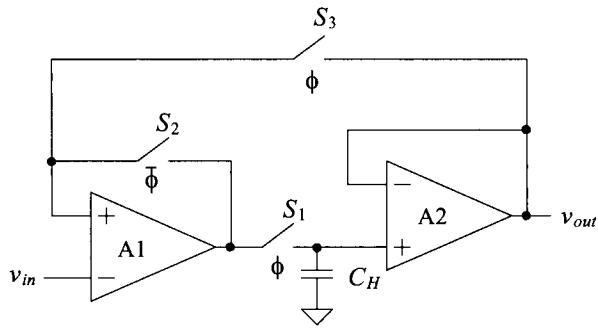

Figure 25.9 A closed-loop S/H circuit.

capacitors can be added to stabilize its performance, the size and placement of the capacitors depend solely on the type and characteristics of the op-amps.

Another S/H circuit is seen in Fig. 25.10. Here, a transconductance amplifier is used to charge the hold capacitor. A control signal turns the amplifier, A1, on or off digitally, thus eliminating the need for the switches S_2 and S_3 (from Fig. 25.9). Since CMOS op-amps are well suited for high-output impedance applications, this configuration would seem to be a popular one. However, the speed of this topology is dictated by the maximum current output of the transconductance amplifier and the size of the hold capacitor.

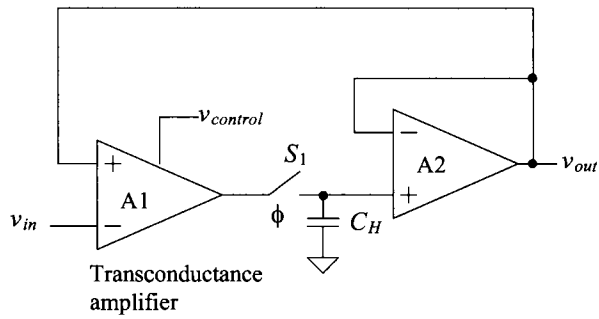

Figure 25.10 A closed-loop S/H circuit using a transconductance amplifier.

A third S/H circuit can be seen in Fig. 25.11. The advantage of this circuit may not be completely obvious and warrants further explanation. First, notice that the hold capacitor is actually in the feedback path of the amplifier, A2, with one side connected to the output of the amplifier and the other connected to a virtual ground. When switch S_1 turns off, any charge injected onto the hold capacitor results in a slight change in the output voltage. However, now that one side of the switch is at virtual ground, the change in voltage is no longer dependent on the threshold voltage of the switch itself. Therefore,

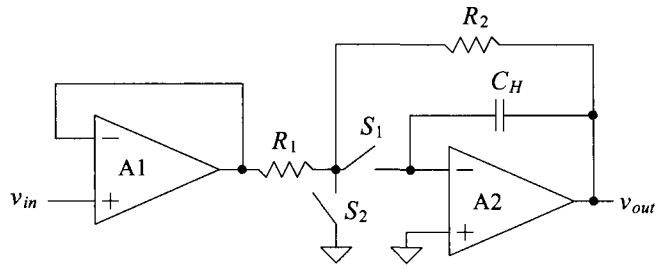

Figure 25.11 A closed-loop S/H circuit using a transconductance amplifier.

the charge injection will be independent of the input signal and will result as a simple offset at the output. An offset error is much easier to tolerate than a nonlinearity error, as will be seen in Chs. 28 and 29.

When sampling, S_1 is closed and S_2 is open, and the equivalent circuit is simply a low-pass filter with a buffered input. The overall transfer function becomes

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1} \cdot \frac{1}{(sR_2C_H + 1)} \tag{25.8}$$

Therefore, this circuit performs a low-pass filter function while sampling. The buffer A1 can be eliminated when we desire a low-input impedance. Once hold mode commences, the output will stay constant at a value equal to v_{in}, while the switch S_2 isolates the input from the hold capacitor. One important issue to note here is that A2 will need to be a buffered CMOS amplifier because of the resistive load attached at v_{out} during hold mode. Notice also that during both sample mode and hold mode, there is only one op-amp in each feedback loop, so this S/H topology is much more stable than the closed-loop structure introduced in Fig. 25.10.

25.2 Fully-Differential Circuits

As we saw in Fig. 25.6 and the associated discussion, using a fully-differential topology (an op-amp with both differential inputs and outputs) can reduce the effects from imperfect switches. However, using a fully-differential topology requires the use of a *common-mode-feedback* (CMFB) circuit. In the following we present an overview of fully-differential op-amps and their application in a sample-and-hold circuit.

Gain

The differential output op-amp symbol is shown in Fig. 25.12. The open-loop gain of the op-amp is related to its inputs and outputs by

$$v_{out} = v_{op} - v_{om} = A_{OL} \cdot (v_p - v_m) \tag{25.9}$$

This should be compared to the single-ended output op-amp (the op-amp we have been discussing up to this point), which has a gain given by

$$v_{out} = v_{op} = A_{OL} \cdot (v_p - v_m) \tag{25.10}$$

If we ignore v_{om}, then the differential output op-amp behaves just like a single-ended op-amp. For linear applications, the op-amp is used with a feedback network, the inputs are related (assuming the open-loop gain, A_{OL} is large) by

$$v_p \approx v_m \tag{25.11}$$

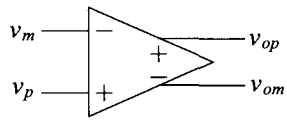

Figure 25.12 Differential output op-amp.

Common-Mode Feedback (CMFB)

Normally, the average of the op-amp outputs is called the common-mode output voltage. The two op-amp outputs swing around the common-mode voltage. If the largest op-amp output voltage is *VDD* and the minimum output voltage is ground, then the common-mode voltage is

$$V_{CM} = \frac{VDD}{2} \tag{25.12}$$

Figure 25.13a shows a simple differential output op-amp gain configuration (inverting or noninverting, depending on which output is used as the positive output). Because the input voltages to the circuit are equal, the output voltages of the op-amp should remain at V_{CM}. Due to the op-amp's high gain and the negative feedback, we always have $v_p \approx v_m$ (Eq. [25.11]). However, if $v_{op} = v_{om} = VDD$ or $v_{op} = v_{om}$ = ground or $v_{op} = v_{om}$ = anything, then $v_p = v_m$ and Eq. (25.11) is satisfied. *This is a problem* and the reason why we need a CMFB circuit. In Fig. 25.13b, we add a CMFB circuit to monitor the outputs of the op-amp and make adjustments in the op-amp (how these adjustments are made is discussed in the next chapter) to keep the two outputs balanced around V_{CM} ($VDD/2$).

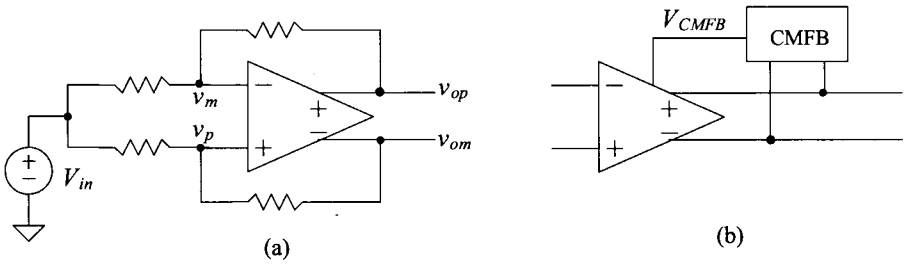

Figure 25.13 (a) Simple gain configuration using differential output op-amp and (b) the use of a common-mode feedback circuit to adjust the common-mode output voltage.

Coupled Noise Rejection

Differential topologies are required to minimize the effects of charge injection and capacitive feedthrough from switches. They also are used to help reduce the effects of coupled noise. Consider the cascade of differential output op-amps, with no feedback network shown, seen in Fig. 25.14. The stray capacitance between the interconnecting metal lines (the metal lines that carry the signals between op-amps) and the substrate or any other noise source are shown. If the metal lines are run close to one another, then the noise voltage will couple even amounts (ideally) of noise into each signal wire. Since the diff-amp, on the input of the op-amp, rejects common signals (signals that are present on both inputs), the coupled noise is not passed to the next op-amp in the string. Variations on the power supply rails are rejected as well. If the differential op-amp is symmetric, then changes on the power supply couple evenly into both outputs, having little effect on the difference, or desired signal, coming out of the op-amp. For these reasons, that is, good coupled noise rejection and PSRR, the differential op-amp is a necessity in any dynamic analog integrated circuit.

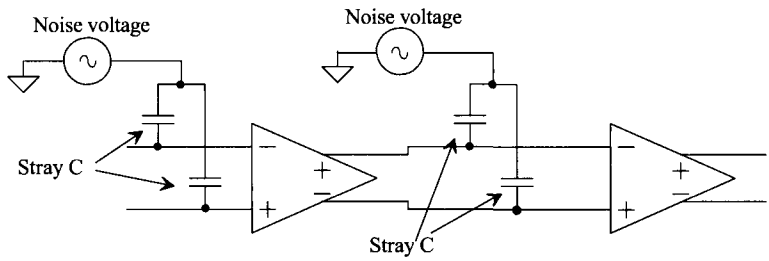

Figure 25.14 Differential output op-amps showing parasitic capacitance and noise.

Other Benefits of Fully-Differential Op-Amps

Another benefit of fully-differential circuits is a doubling in output voltage swing. For example, if *VDD* is 1 V, then the output of a single-ended op-amp can swing from 1 V to ground. In a fully-differential topology, both v_{op} and v_{om} can swing from 0 to 1. Using Eq. (25.9), we can write

$$v_{out,\max} = v_{op} - v_{om} = 1 - 0 = 1\ V \text{ and } v_{out,\min} = v_{op} - v_{om} = 0 - 1 = -1\ V \quad (25.13)$$

The output swing is $2VDD$ when using fully-differential topologies.

A further benefit of fully-differential topologies is the fact that the input common-mode voltage of the op-amp remains at V_{CM} (and so the op-amp's first stage diff-amp's common-mode voltage range requirements are easy to meet).

25.2.1 A Fully-Differential Sample-and-Hold

Figure 25.15 shows a fully-differential sample-and-hold circuit and the associated clock waveforms that eliminate clock feedthrough and charge injection to a first order. The switches in this figure are closed when their controlling clock signals are high. The basic operation can be understood by considering the state of the circuit at t_0. At this time, the

input signals charge the sampling capacitors. The bottom plates of the capacitors (poly1) are tied directly to the input signals, for reasons that will be explained below. The op-amp is operating in a unity-follower configuration in which both inputs of the op-amp are held at V_{CM}. At this particular instance in time, prior to t_1, the amplifier is said to be operating in the sample mode of operation.

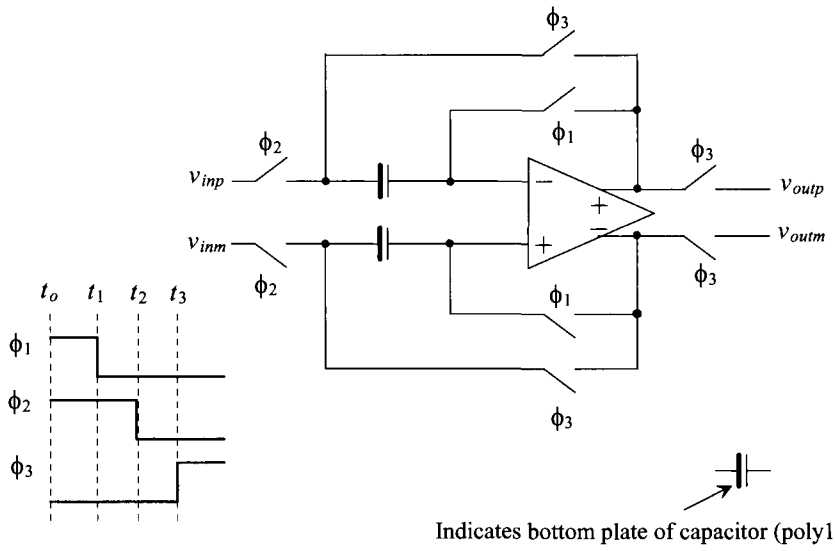

Figure 25.15 Sample-and-hold using differential topology.

At t_1, the ϕ_1 switches turn off. The resulting charge injection and clock feedthrough appear as a common-mode signal on the inputs of the op-amp and are ideally rejected. Since the top plates of the hold capacitors (the inputs to the op-amp) are always at V_{CM}, at this point in time the charge injection and clock feedthrough are independent of the input signals. This produces an increase in the dynamic range of the sample-and-hold (the minimum measurable input signal decreases). The voltage on the inputs of the op-amp (the top plate of the capacitor) between t_1 and t_2 is $V_{OFF1} + V_{CM}$, a constant voltage. Note that the op-amp is operating open loop at this time so the time between t_1 and t_3 should be short.

At t_2 the ϕ_2 switches turn off. At this point in time, the voltages on the bottom plates of the sampling (or hold) capacitors (poly1) are v_{inp} and v_{inm}. The voltages on the top plates of the capacitors (connected to the op-amp) are $V_{OFF1} + V_{OFF2} + V_{CM}$ (assuming that the storage capacitors are much larger than the input capacitance of the op-amp). The term V_{OFF2} is ideally a constant that results from the charge injection and capacitive feedthrough from the ϕ_2 switches turning off. The time between t_1 and t_2 should be short compared to variations in the input signals.

At time t_3 the ϕ_3 switches turn on and the op-amp behaves like a voltage follower; the circuit is said to be in the hold mode of operation. The charge injection and clock feedthrough resulting from the ϕ_3 switches turning on causes the top plate of the capacitor to become $V_{OFF1} + V_{OFF2} + V_{OFF3} + V_{CM}$, again assuming that the storage capacitors are much larger than the input capacitance of the op-amp. The outputs of the sample-and-hold are v_{inp} and v_{inm}, assuming infinite op-amp gain since these offsets appear as a common-mode voltage on the input of the op-amp. Note that the terms V_{OFF2} and V_{OFF3} are dependent on the input signals.

Connecting the Inputs to the Bottom (Poly1) Plate

The reason for connecting the input signals to the bottom plate of the capacitor can be explained with the help of Fig. 25.16. This figure is a simplified, single-ended version of Fig. 25.15 where the capacitance, C_p, is the parasitic capacitance from the bottom plate to the substrate. With regard to Fig. 25.16a, coupled noise from the substrate sees either the input voltage from the op-amp driving the sample-and-hold (in the sample mode) or the output voltage of the op-amp used in the sample-and-hold itself (in the hold mode). Since the op-amps in either mode directly set this voltage, the substrate noise has, ideally, little effect on the circuit's operation.

In Fig. 25.16b, coupled substrate noise feeds directly into the input of the op-amp and can thus drastically affect the output of the sample-and-hold. Another more subtle problem occurs in the circuit of Fig. 25.16b. When the circuit makes the transition to the hold mode at t_3, the output of the op-amp should quickly change to the voltage sampled on the input capacitors. The time it takes the output of the op-amp to change and settle to this final voltage is called the *settling time*. The parasitic capacitance on the input of the op-amp in (b) reduces the feedback factor from unity to $C_H/(C_p + C_H)$. This slows the settling time and causes a gain error in the circuit's transfer function. For these reasons, the parasitic capacitance on the top plate of the capacitor should be small. Nothing should be laid out over or in near proximity of poly2.

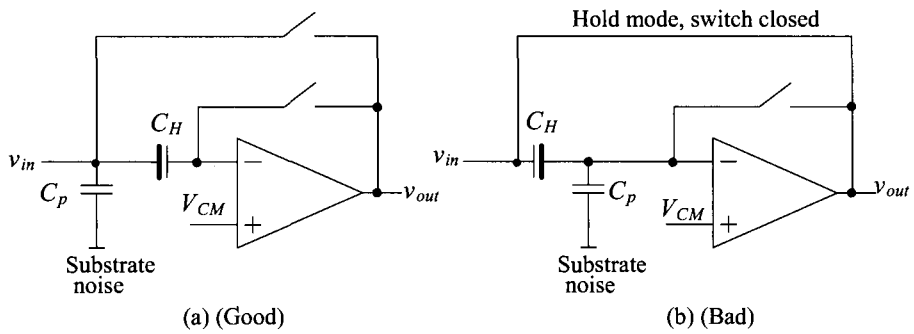

Figure 25.16 Explanation for connecting the bottom plate of the capacitor to the input.

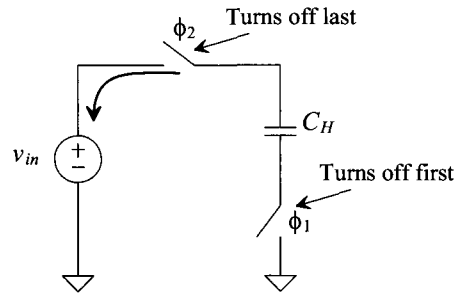

Figure 25.17 Bottom plate sampling.

Bottom Plate Sampling

Turning the ϕ_1 controlled switches off in Fig. 25.15 slightly before the ϕ_2 controlled switches is sometimes called *bottom plate sampling*. Figure 25.17 illustrates why. When the ϕ_1 switches turn off, the charge injected into C_H is a constant independent of the input signal amplitude. The resulting offset voltage across C_H is then constant. When the ϕ_2 switches turn off, the resulting charge injection then takes the path of least resistance, that is, into the input source v_{in}. The voltage across C_H is then, ideally, independent of the input signal voltage.

SPICE Simulation

Let's simulate the operation of the sample-and-hold in Fig. 25.15. To begin, let's use voltage-controlled voltage sources and a DC voltage to model the op-amp (again, we'll discuss differential output op-amps in the next chapter). The ideal fully-differential output op-amp SPICE model is seen in Fig. 25.18. The SPICE netlist statements used to model this circuit (we'll assume an open-loop gain of 10^6 and *VDD* of 1 *V*) are

```
E1    vop   vcm   vp    vm    1e6
E2    vcm   vom   vp    vm    1e6
Vcm   vcm   0     DC    500m
```

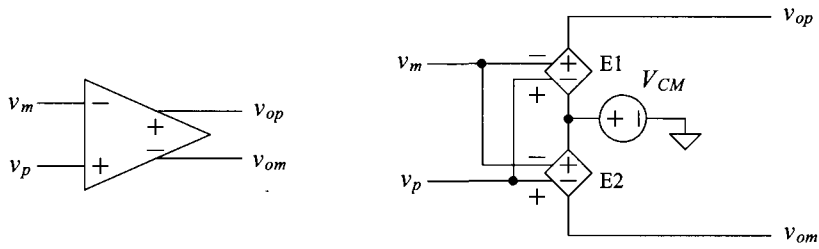

Figure 25.18 SPICE modeling a differential input/output op-amp with common-mode voltage.

For the switches we'll use NMOS devices as seen in the simulation schematic of Fig. 25.19. For the input signals, we've used a 5 MHz sinewave signal with a peak amplitude of 200 mV. Note that each of the inputs is referenced to the common-mode voltage, V_{CM} (which is 500 mV here).

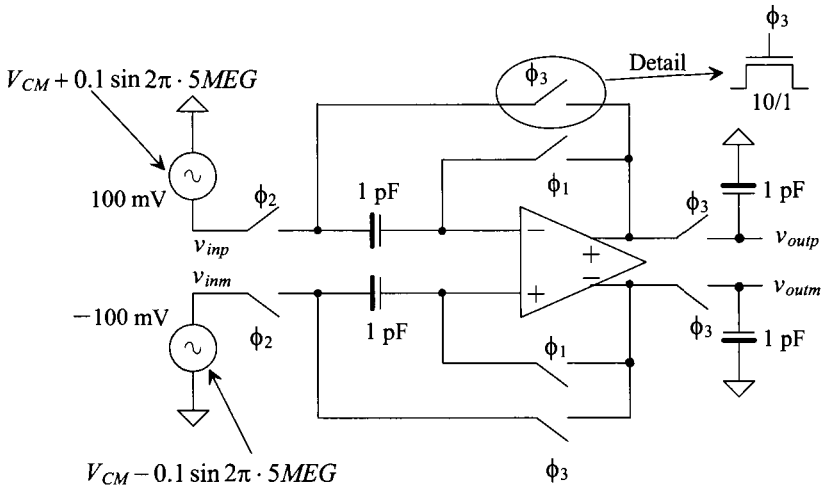

Figure 25.19 Simulating the operation of the fully differential sample-and-hold.

The simulation results are seen in Fig. 25.20. Let's first focus on the clock signals. Notice how ϕ_3 isn't high at the same time as ϕ_1 or ϕ_2. If all switches were "on" at the same time, the charge stored (or held) on the 1 pF capacitors at the output of the circuit would change (remember when the ϕ_1 switches close the op-amp is in the follower configuration with the inputs and outputs pulled to V_{CM}). We make sure to disconnect these output capacitors before putting the circuit into the sample mode. The output of the sample-and-hold seen in Fig. 25.20 doesn't exactly match the input signal. There is a one-clock cycle delay and we can see the effects of the finite clock frequency (finite sample points). Note, these topics are discussed in detail in the book entitled *CMOS Mixed-Signal Circuit Design*.

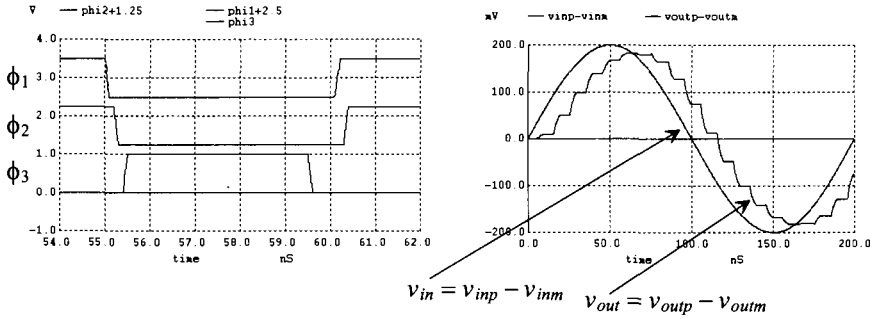

Figure 25.20 Simulating the operation of the sample-and-hold in Fig. 25.19.

25.3 Switched-Capacitor Circuits

Consider the circuit shown in Fig. 25.21a. This dynamic circuit, named a *switched-capacitor resistor*, is useful in simulating a large value resistor, generally >1 MΩ. The clock signals ϕ_1 and ϕ_2 form two phases of a nonoverlapping clock signal with frequency f_{clk} and period T as seen in the figure. Let's begin by considering the case when S1 is closed. When ϕ_1 is high, the capacitor C is charged to v_1. The charge, q_1, stored on the capacitor during this interval, Fig. 25.21c, is

$$q_1 = Cv_1 \tag{25.14}$$

while if S2 is closed, the charge stored on the capacitor is

$$q_2 = Cv_2 \tag{25.15}$$

If v_1 and v_2 are not equal, keeping in mind that S1 and S2 cannot be closed at the same time due to the nonoverlapping clock signals, then a charge equal to the difference between q_1 and q_2 is transferred between v_1 and v_2 during each interval T. The difference in the charge is given by

$$q_1 - q_2 = C(v_1 - v_2) \tag{25.16}$$

If v_1 and v_2 vary slowly compared to f_{clk}, then the average current transferred in an interval T is given by

$$I_{avg} = \frac{C(v_1 - v_2)}{T} = \frac{v_1 - v_2}{R_{sc}} \tag{25.17}$$

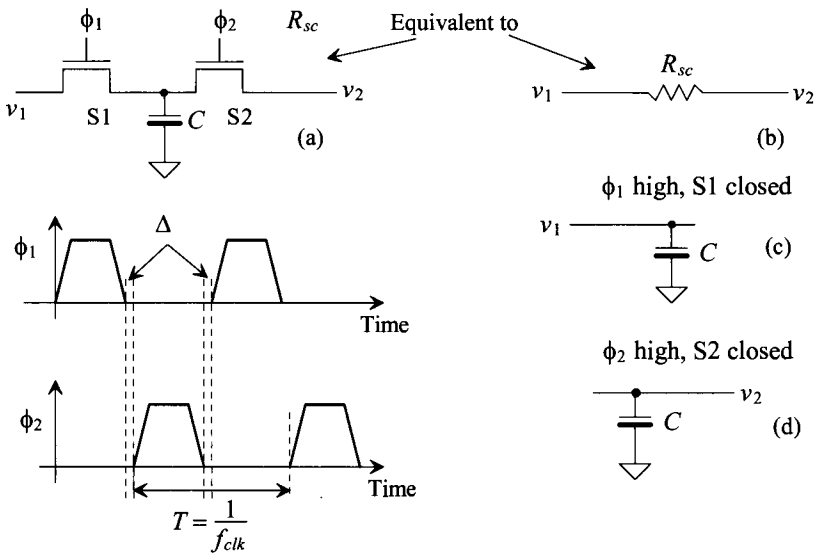

Figure 25.21 Switched-capacitor resistor (a) and associated waveforms and (b, c, d) the equivalent circuits.

The resistance of the switched-capacitor circuit is given by

$$R_{sc} = \frac{T}{C} = \frac{1}{C \cdot f_{clk}} \tag{25.18}$$

In general, the signals v_1 and v_2 should be bandlimited to a frequency at least ten times less than f_{clk} (more on this later). Note that we derived a similar result back in Ch. 17, see Eq. (17.29).

Example 25.1

Using switched-capacitor techniques, implement the circuit shown in Fig. 25.22a so that the product of RC is 1 ms, that is, the 3-dB frequency of $|v_{out}/v_{in}|$ is 159 Hz.

The switched-capacitor implementation of this circuit is shown in Fig. 25.22b. The product of RC may now be written in terms of Eq. (25.18) as

$$RC_2 = \frac{C_2}{C_1} \cdot \frac{1}{f_{clk}} \tag{25.19}$$

This result is important! The product RC_2 is determined by f_{clk}, which may be an accurate frequency derived from a crystal oscillator and the ratio of C_2 to C_1, which will be within 1% on a chip. This means that even if the values of the capacitors change by 20% from wafer to wafer, the ratio of the capacitors relative to one another, on the same wafer, will remain constant within 1%.

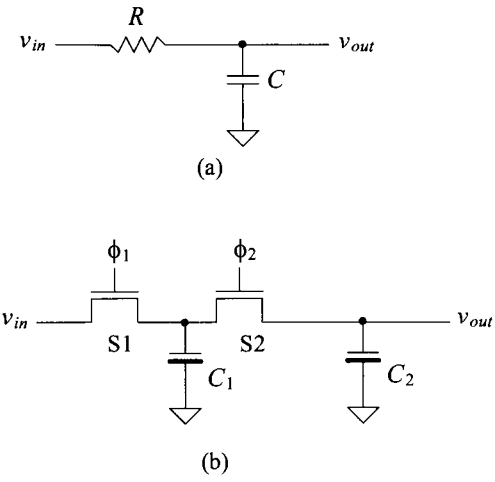

Figure 25.22 (a) Circuit used in Ex. 27.1 and (b) its implementation using a SC resistor.

It is also desirable to keep C_1 larger than the associated parasitics present in the circuit (e.g., depletion capacitances of the source/drain implants and the stray capacitances to substrate). For the present example, we will set C_1 to 1 pF. The selection of f_{clk} is usually determined by what is available. For the present design, a value of 100 kHz will be used. This selection assumes that the energy present in v_{in} at frequencies above 10 kHz is negligible. The value of C_2 is determined solving Eq. (25.19) and is 100 pF. Note that the value of the switched-capacitor

resistor is 10 MΩ. Implementing this resistor in a CMOS process using n-well with a sheet resistance of 1,000 ohms/square would require 10,000 squares! The resulting delay through the n-well resistor, because of the capacitance to substrate, may cause a significant phase error in the transfer function. ■

25.3.1 Switched-Capacitor Integrator

Because the switched-capacitor resistor of Fig. 25.21a is sensitive to parasitic capacitances, it finds little use, by itself, in analog switched-capacitor circuits. Consider the circuit of Fig. 25.23a. This circuit, a switched-capacitor integrator, is the heart of the circuits we will be discussing in the remainder of the section. The portion of the circuit consisting of switches S1 through S4 and C_I forms a switched-capacitor resistor with a value given by

$$R_{sc} = \frac{1}{C_I f_{clk}} \tag{25.20}$$

The equivalent continuous time circuit for the switched-capacitor integrator is shown in Fig. 25.23b. Notice that v_{in} is now negative. It may be helpful in the following discussion to remember that the combination of switches and C_I of the switched-capacitor integrator can be thought of as a simple resistor. The transfer function of the switched-capacitor integrator is given by

$$\frac{v_{out}}{v_{in}} = \frac{1/j\omega C_F}{R_{sc}} = \frac{1}{j\omega\left(\frac{C_F}{C_I} \cdot \frac{1}{f_{clk}}\right)} \tag{25.21}$$

Again, the ratio of capacitors is present, allowing the designer to precisely set the gain of the amplifier and the integration time constant.

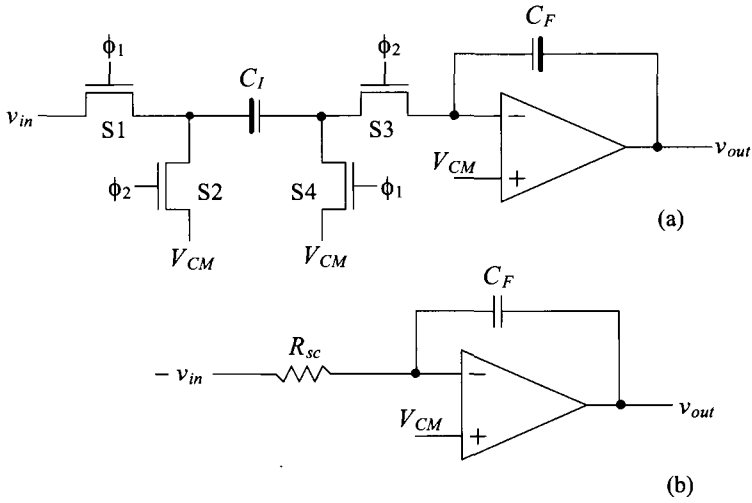

Figure 25.23 (a) A stray insensitive switched-capacitor integrator (noninverting) and (b) the equivalent continuous time circuit.

Parasitic Insensitive

The switched-capacitor integrator in Fig. 25.23 is not sensitive to parasitic or stray capacitances. This can be understood with the use of Fig. 25.24. To begin, if we realize that C_{p2} (the parasitic capacitance on the right side of C_I) is always connected to V_{CM} either through S4 or through the connection to the inverting input of the op-amp, then C_{p2} doesn't see a change in the charge stored on it. Next, the capacitance C_{p1} is charged to v_{in} when S1 is closed and then charged to V_{CM} when S2 closes. Since none of the charge stored on C_{p1} when S1 is closed is transferred to C_I, it does not affect the integrating function. A practical minimum for C_I is 100 fF set by kT/C noise (see Table 8.1).

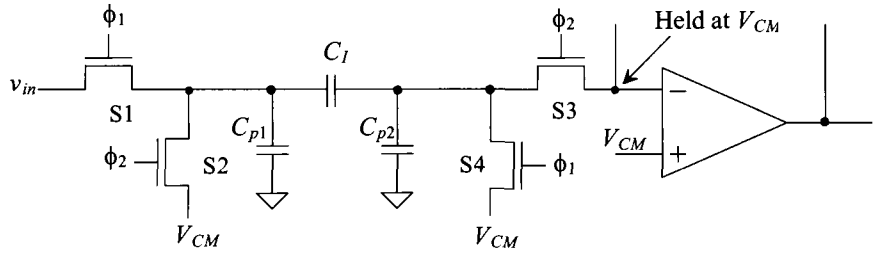

Figure 25.24 Parasitic capacitances associated with a switched-capacitor resistor.

Other Integrator Configurations

An inverting integrator configuration can be formed by simply swapping the clock signals used with S1 and S2 in Fig. 25.23 (the noninverting configuration). The gate of S1 is connected, for the inverting configuration, to ϕ_2 while the gate of S2 is connected to ϕ_1. The gain of this configuration is given by

$$\frac{v_{out}}{v_{in}} = -\frac{1}{j\omega\left(\frac{C_F}{C_I}\cdot\frac{1}{f_{clk}}\right)} \tag{25.22}$$

An example of a switched-capacitor integrator circuit that combines input signals is shown in Fig. 25.25a. Remembering that each switched-capacitor section can be thought of as a resistor, we note that the relationship between the inputs and output is

$$v_{out} = \frac{v_1}{j\omega\left(\frac{C_F}{C_1}\frac{1}{f_{clk}}\right)} + \frac{v_2}{j\omega\left(\frac{C_F}{C_2}\frac{1}{f_{clk}}\right)} - \frac{v_3}{j\omega\left(\frac{C_F}{C_3}\frac{1}{f_{clk}}\right)} \tag{25.23}$$

Figure 25.25b shows how redundant switches can be combined to reduce the number of devices used. Used alone, the basic integrator has the practical problem of integrating not only the input signal but also the offset voltage of the op-amp. In many applications, a reset switch or resistor is placed across the feedback capacitor (Fig. 25.25b). An example of a lossy integrator circuit useful in first-order filter design is shown in Fig. 25.26. The transfer function of this circuit is given by

$$\frac{v_{out}}{v_{in}} = \frac{R_4}{R_3}\left(\frac{1+j\omega R_3 C_1}{1+j\omega R_4 C_2}\right) = \frac{C_3}{C_4}\left(\frac{1+j\omega\left(\frac{C_1}{C_3}\cdot\frac{1}{f_{clk}}\right)}{1+j\omega\left(\frac{C_2}{C_4}\cdot\frac{1}{f_{clk}}\right)}\right) \tag{25.24}$$

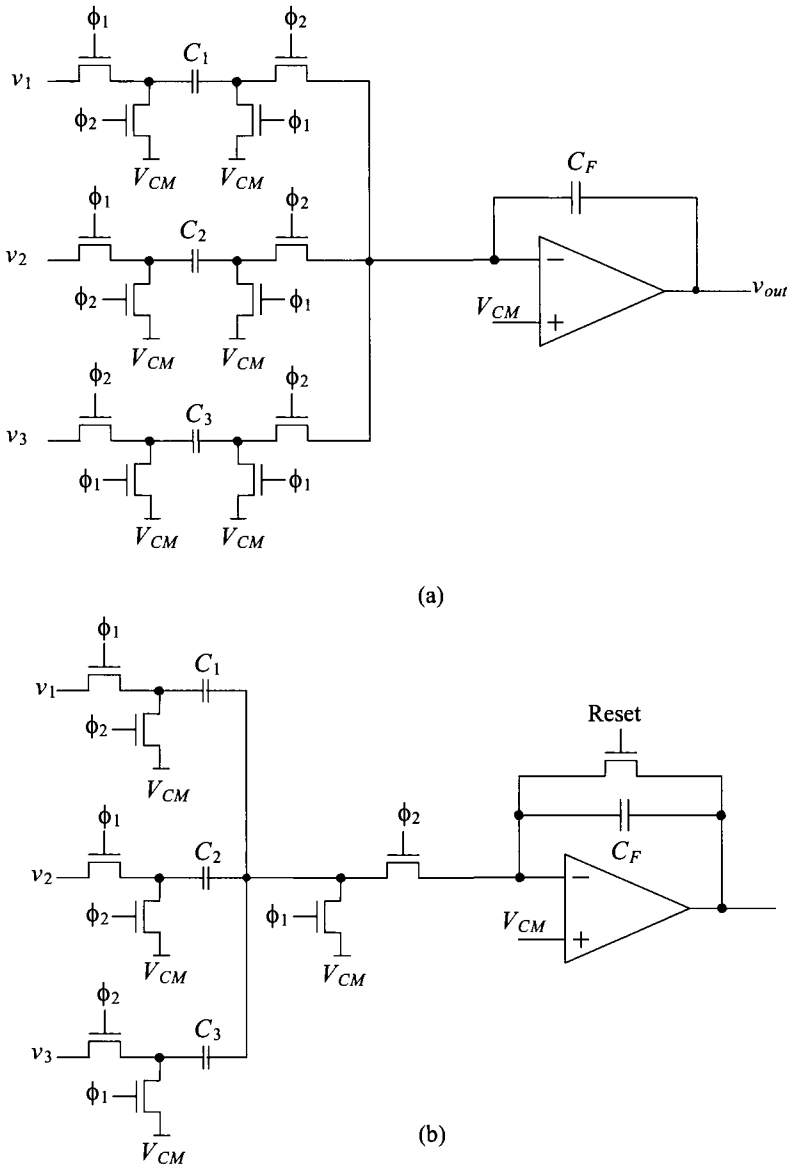

Figure 25.25 (a) Switched-capacitor implementation of a summing integrator and (b) practical implementation of the circuit combining switches and adding reset.

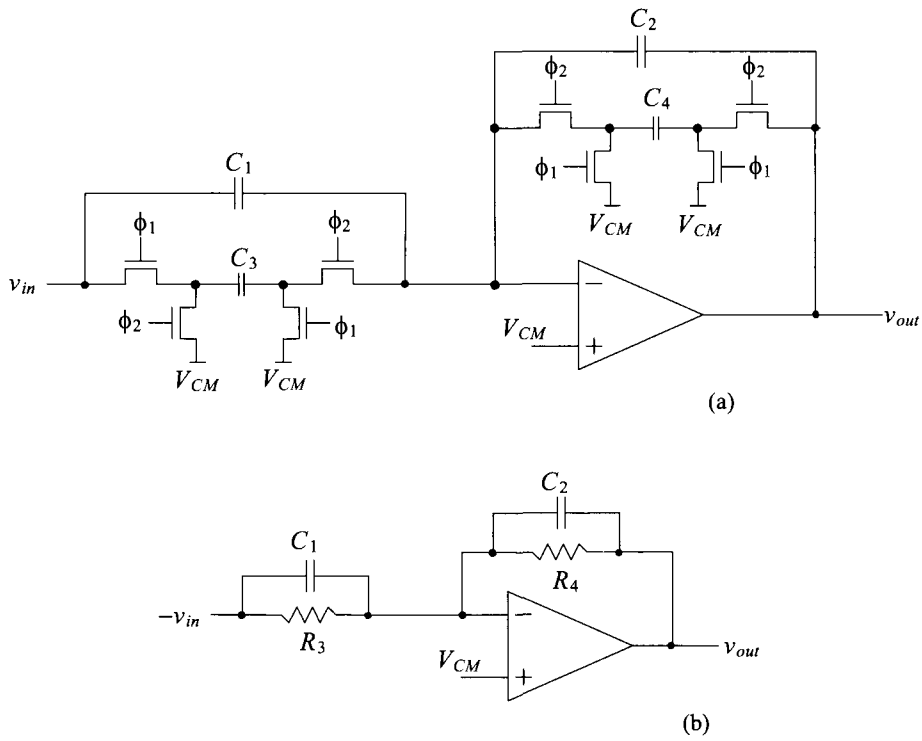

Figure 25.26 Lossy integrator (a) switched-capacitor implementation and (b) continuous time circuit.

For low-frequency input signals (low frequencies compared to the pole and zero given in Eq. (25.24), the gain of the lossy integrator is simply

$$\frac{v_{out}}{v_{in}} = \frac{C_3}{C_4} \tag{25.25}$$

which is again a precise number due to the ratio of the capacitors. Also note that the switched-capacitor resistor in the feedback loop is stray insensitive. The left side of C_4 is always connected to V_{CM}, while the right side is either connected to V_{CM} or to the output of the op-amp.

Note that we cannot eliminate the capacitor across the switched-capacitor resistor in the feedback path. If we were to do so, then the op-amp would be operating open-loop when ϕ_2 goes low. The outputs of the op-amp would then rail up at *VDD* or down at ground.

Example 25.2

Design a switched-capacitor filter with the transfer characteristics shown in Fig. 25.27.

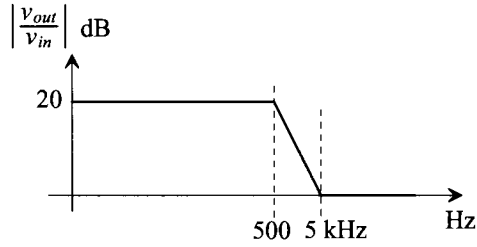

Figure 25.27 Filter characteristics for Ex. 25.2.

We can see that this transfer function has a pole at 500 Hz and a zero at 5 kHz. The lossy integrator of Fig. 25.26 will be used to realize this filter. The low-frequency gain of this circuit is 10 (20 dB). Using Eq. (25.25), we have

$$\frac{C_3}{C_4} = 10$$

while the pole and zero locations are given by

$$f_p = \frac{1}{2\pi\left(\frac{C_2}{C_4} \cdot \frac{1}{f_{clk}}\right)} = 500 \text{ and } f_z = \frac{1}{2\pi\left(\frac{C_1}{C_3} \cdot \frac{1}{f_{clk}}\right)} = 5 \text{ kHz}$$

If we set f_{clk} to 100 kHz and C_4 to 100 fF, then C_3 = 1.0 pF, C_2 = 3.2 pF, and C_1 = 3.2 pF. ■

Exact Frequency Response of a Switched-Capacitor Integrator

We will now develop an exact relationship between the switching frequency, f_{clk}, and the signal frequency ω. Referring to Fig. 25.28, we can write the output of the integrator as the sum of the previous output voltage, $v_{out(n)}$, at a time nT and the contribution from the current sample as

$$v_{out(n+1)} = v_{out(n)} + \frac{C_I}{C_F} \cdot v_{in(n)} \tag{25.26}$$

Since a delay in the time domain of T corresponds to a phase shift of ωT in the frequency domain, we can take the Fourier transform of this equation and get

$$e^{j\omega T} v_{out}(j\omega) = v_{out}(j\omega) + \frac{C_I}{C_F} \cdot v_{in}(j\omega) \tag{25.27}$$

Solving this equation for v_{out}/v_{in} gives

$$\frac{v_{out}}{v_{in}}(j\omega) = \frac{C_I}{C_F}\left(\frac{1}{e^{j\omega T} - 1}\right) = \frac{C_I}{C_F}\left(\frac{e^{-j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}\right) = \frac{C_I}{C_F}\left[\frac{1}{z-1}\right] \tag{25.28}$$

where $z = e^{j\omega T}$. Remembering $f_{clk} = 1/T$ and $\omega = 2\pi f$, we get

$$\frac{v_{out}}{v_{in}}(j\omega) = \frac{1}{j\omega\left(\frac{C_F}{C_I} \cdot \frac{1}{f_{clk}}\right)}\left(\frac{\frac{\pi \cdot f}{f_{clk}}}{\sin\frac{\pi \cdot f}{f_{clk}}} \cdot e^{-j\pi \cdot f/f_{clk}}\right) \tag{25.29}$$

Ideally, the term on the right in parentheses is unity. This occurs when f is much less than f_{clk}. This equation describes how the magnitude and phase of the integrator are affected by finite f_{clk}.

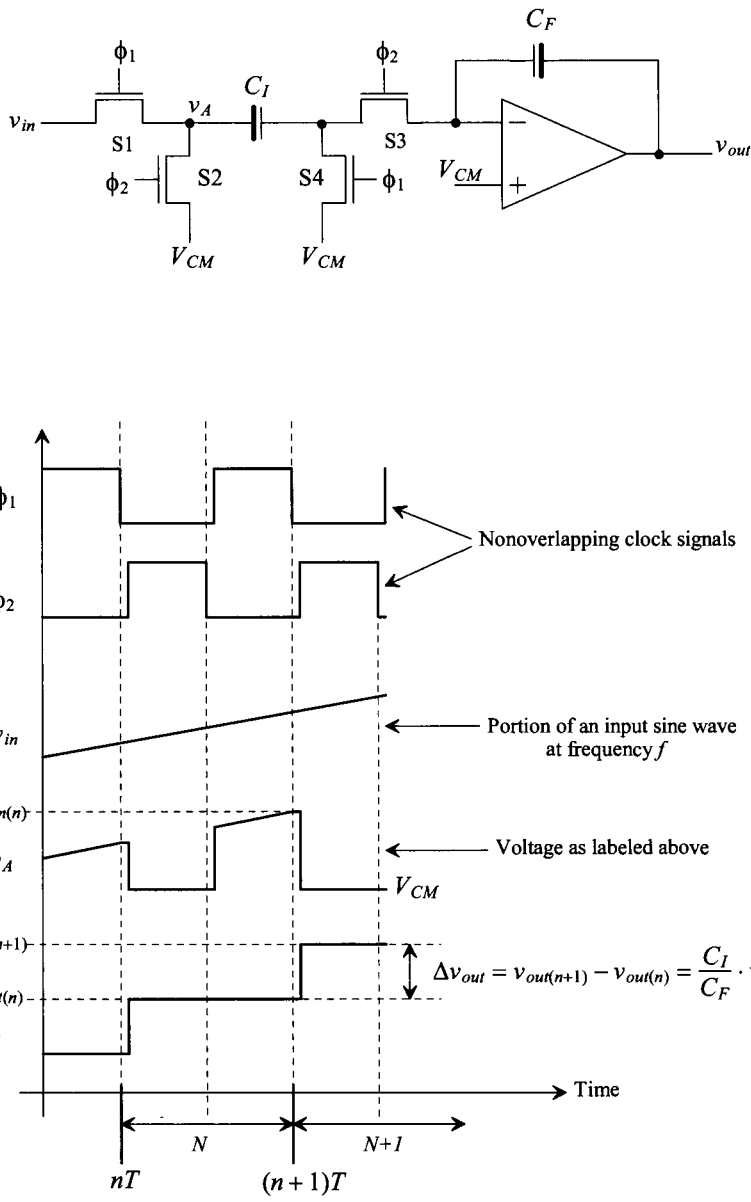

Figure 25.28 Switched-capacitor integrator used to determine the relationship between input frequency and switch clock frequency.

Capacitor Layout

An important step in the implementation of any switched-capacitor design is the layout of the capacitors. Normally, a unit-size capacitor is laid out and then replicated to the desired capacitance (as discussed in Ch. 6). For Ex. 25.2, the unit size capacitance would nominally be 100-fF (using the 1 μm process) or 10 *fF* (in the 50 nm process), as in Fig. 25.29. Note that here, in Fig. 25.29a, we are assuming that a circle can be accurately reproduced on the reticle and patterned on the wafer. In practice, effects such as the finite e-beam size (and the granularity of the grid) used to make the reticle can make this assumption questionable. Figure 25.29b shows a layout where we've tried to minimize the number of 90° corners in an effort to avoid pattern errors when etching poly2.

Again, the absolute value of the capacitors isn't important; rather, the important value is the ratio. A total of 32 of these unit-size capacitors (using a unit-size cell of 100 *fF*) would be used to achieve the larger nominally 3.2 pF capacitors in Ex. 25.2 (see Fig. 25.30). This approach (using unit elements to make the large capacitors) eliminates errors due to uneven patterning of poly to a first order. A p+ guard ring can be placed around the capacitor to help reduce coupled substrate noise. Substrate noise can also be reduced by laying the capacitor out over an n-well that is tied to *VDD*. Injected minority carriers are collected either by the p+ or the n-well (or a combination of both). If matching of the capacitors is critical, schemes that use a common-centroid layout can be used. Also, as was discussed in Ch. 20, dummy poly strips or capacitors can be placed around the array of capacitors so that the edge differences from underetching poly are eliminated. In both cases, what we are doing is trying to ensure that all capacitors see the same adjacent structures.

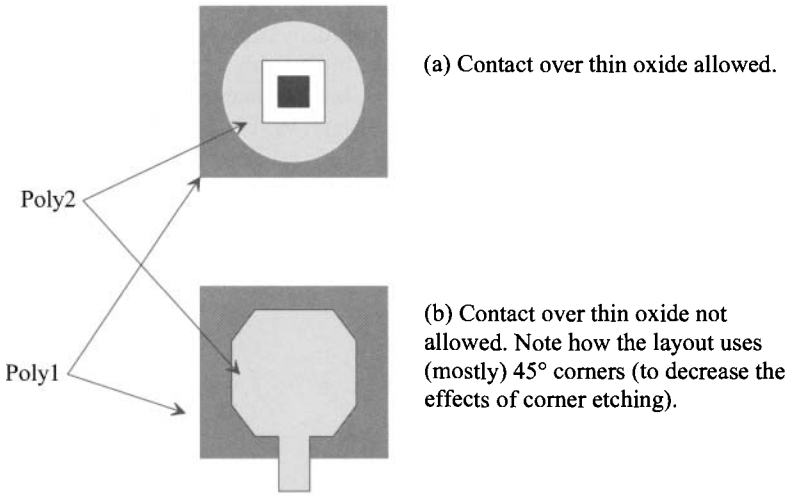

Figure 25.29 Layout of a unit cell capacitor.

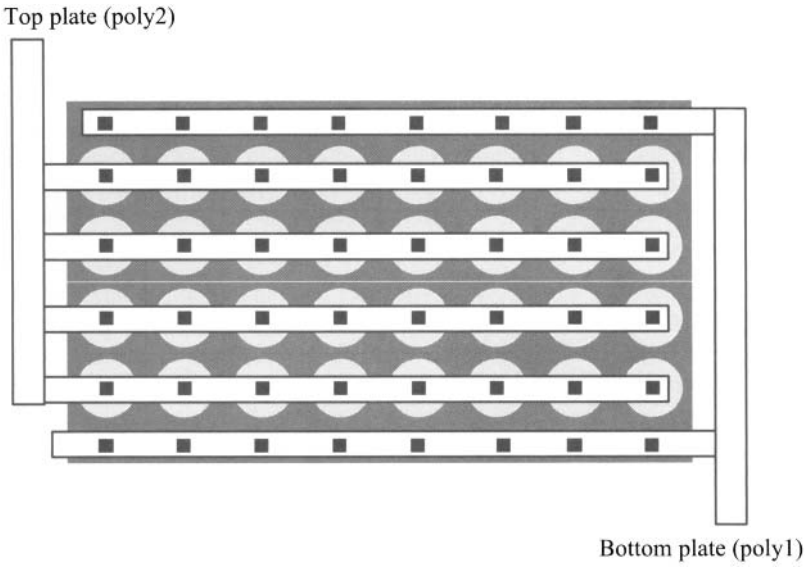

Figure 25.30 Layout of a 3.2 pF capacitor using a 100 fF unit cell.

Op-Amp Settling Time

Figure 25.31 shows an op-amp configuration in which the op-amp can source or sink current to a switched capacitor and a feedback capacitor. The time it takes to charge and discharge these capacitors is important because it directly affects the maximum switched capacitor clocking frequency, f_{clk}. The slew-rate limitations of the op-amp have been discussed in detail already. Let's now consider the limitations due to op-amp finite bandwidth. The closed-loop gain of the op-amp is given by (see Eq. [24.5])

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL} \cdot \beta} \tag{25.30}$$

while the open-loop gain of an op-amp is given, with units of A/A, V/V, V/A, or A/V, by

$$A_{OL} = \frac{A_{OL}(0)}{1 + j\frac{f}{f_{3dB}}} \tag{25.31}$$

Combining these equations and assuming $1 >> 1/[\beta \cdot A_{OL}(0)]$, we get

$$A_{CL} = \frac{\frac{1}{\beta}}{1 + j\frac{f}{f_{un} \cdot \beta}} \tag{25.32}$$

where $f_{3dB} \cdot A_{OL}(0) = f_{un}$, where f_{un} may have units of Hz, Hz/Ω, or Hz·Ω ($f_u\beta$ is in Hz). The closed-loop gain reduces to a simple single-pole transfer function (see Eqs. [24.30]–[24.34]). The low-frequency gain of the circuit is $1/\beta$, while the product of f_{un} and β gives the circuit time constant of

$$\tau = \frac{1}{2\pi f_{un} \cdot \beta} \tag{25.33}$$

keeping in mind the unity-gain frequency of the op-amp, f_{un}, is a strong function of the load capacitance. For a step-input to the op-amp, a common occurrence in switched-capacitor circuits (Fig. 25.28), the output voltage of the op-amp, again neglecting slew-rate limitations, is given by

$$v_{out} = V_{outfinal}(1 - e^{-t/\tau}) \tag{25.34}$$

For the output voltage of the op-amp to settle to less than 1% of its final value requires 5τ. A "rule-of-thumb" estimate for the settling time is simply $1/(f_u \cdot \beta)$.

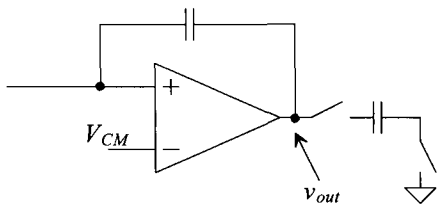

Figure 25.31 Charging and discharging a switched capacitor.

25.4 Circuits

This section presents several examples of dynamic analog circuits.

Reducing Offset Voltage of an Op-Amp

As seen in Fig. 24.4, the op-amp's offset voltage can be modeled by adding a DC voltage in series with the noninverting input of the op-amp, Fig. 25.32a. The basic idea behind eliminating the offset voltage is shown in Fig. 25.32b. A capacitor is charged to a voltage equal and opposite to the comparator offset voltage. The voltage across the capacitor is then added in series with the noninverting op-amp input to subtract away the op-amp's offset.

The dynamic analog circuit shown in Fig. 25.33 is used to implement this subtraction. For this method to be effective, *the op-amp must be stable* in the unity gain configuration. The clock signals ϕ_1 and ϕ_2 are the nonoverlapping clock signals discussed earlier (see Fig. 25.28). The nonoverlapping clocks keep switches S1, S2, and S3 from being on at the same time as switches S4 and S5. Let's consider the case shown in Fig. 25.33b where ϕ_1 is high and ϕ_2 is low. The op-amp, via the negative feedback, tries to force its inverting input to V_{CM}. However, because of the offset, the inverting input is actually charged to $V_{OS} + V_{CM}$. Note that under these conditions the op-amp is removed from the inputs. The voltage across the capacitor is then V_{OS}. When ϕ_2 is high and ϕ_1 is low, Fig. 25.33c, the op-amp functions normally, assuming the storage capacitance C is much larger than the input capacitance of the op-amp.

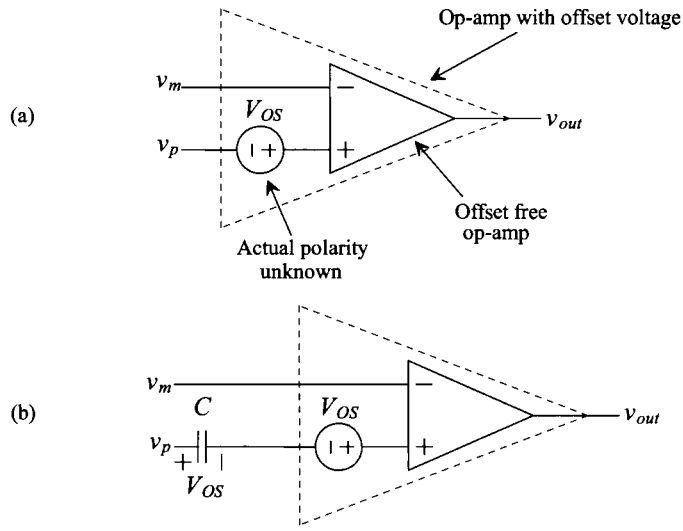

Figure 25.32 (a) Offset voltage of an op-amp modeled by a DC voltage source in series with the noninverting input of the op-amp and (b) using a capacitor to cancel the offset voltage.

Dynamic Comparator

Before we present a dynamic comparator, let's consider the *RC* switch circuit of Fig. 25.34a. When node A is connected to +1 V, node B is connected to ground. Consider what happens when the switches change positions, that is, when node A is connected to ground and the switch at node B is connected to an open. At the moment just after switching takes place, the potential at node B becomes –1 V. In other words, the voltage across the capacitor does not change instantaneously. If node A is connected back to +1 V and node B is connected back to ground a short time compared to the product of R and C, then the voltage across the capacitor remains +1 V.

A more useful circuit for CMOS is shown in Fig. 25.34b. If the switch across C_B is connected to ground when node A is connected to $V1$, then V_B, when the switches change positions, is given by

$$V_B = (V2 - V1) \cdot \frac{C_A}{C_A + C_B} \tag{25.35}$$

Figure 25.35 shows a dynamic comparator based on the inverter. When ϕ_1 is high, the voltage on the v_m input is connected to node A, while the voltage on node B is set via S3 so that the input and output voltages of the inverter are equal. (The inverter is operating as a linear amplifier where both M1 and M2 are in the saturation regions.) When ϕ_2 goes high (ϕ_1 is low since the clocks are nonoverlapping), the v_p input is connected to node A. If C_A is much larger than the input capacitance of the inverter (C_B), then the voltage change on the input of the inverter (V_B) is

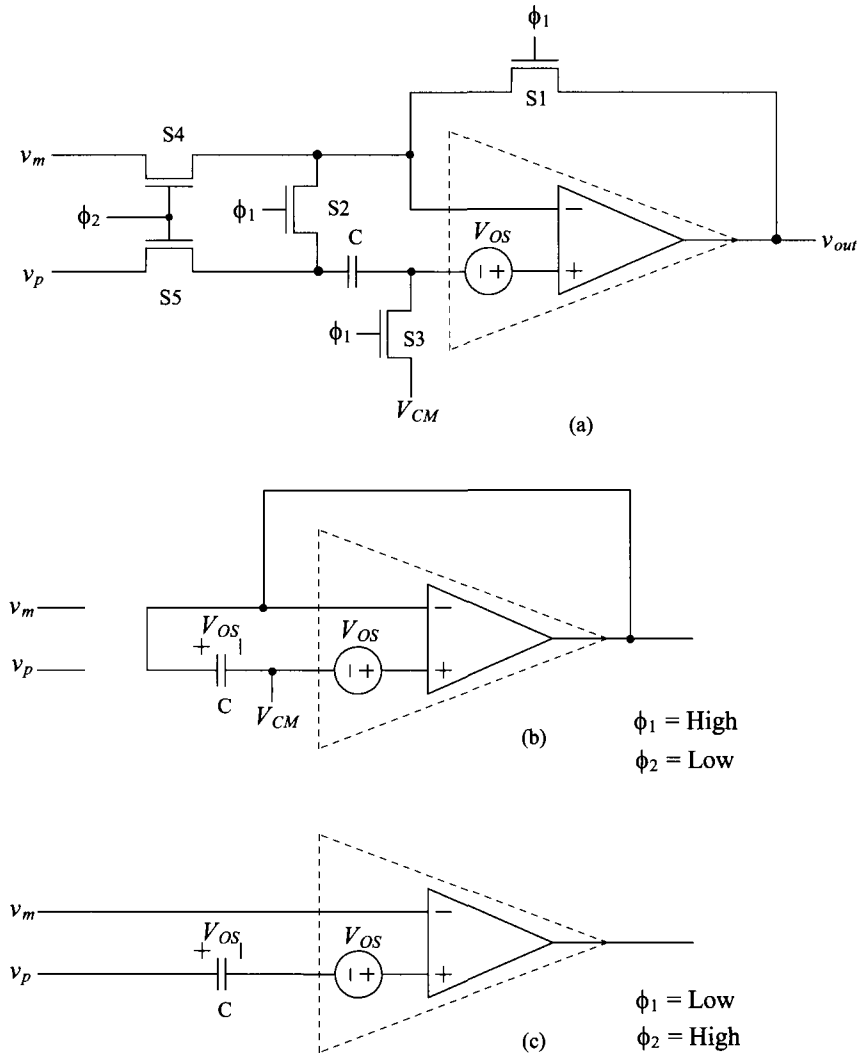

Figure 25.33 Dynamic reduction of the offset voltage.

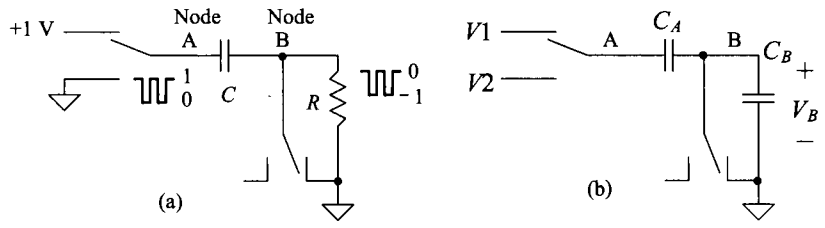

Figure 25.34 Circuits used to illustrate switching in dynamic circuits.

$$v_{in} = v_p - v_m \tag{25.36}$$

Provided the gain of the inverter is large, this change causes the inverter output to rail, that is, go to either *VDD* or ground. The output is then latched and available during ϕ_1. The gain of the comparator can be increased by using additional inverter stages.

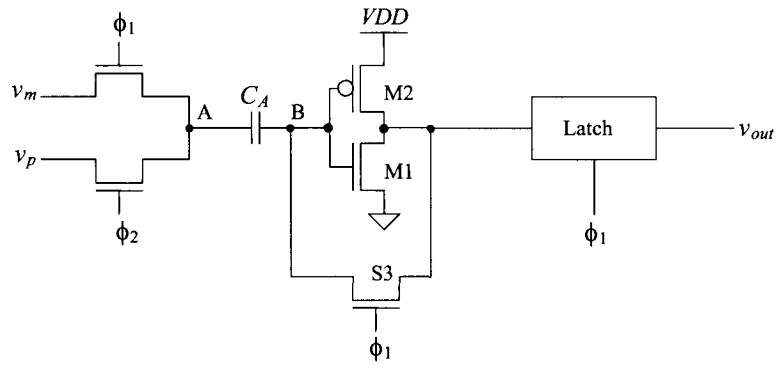

Figure 25.35 A dynamic comparator.

Another high-performance dynamic comparator configuration is based on the sense amplifier in Figs. 16.26 or 16.32 (or Fig. 16.35 so the final outputs only change on the clock's rising edge) that use positive feedback. The offset voltage of the overall comparator is reduced, using either input offset storage (IOS) or output offset storage (OOS) around the comparator preamp. Figure 25.36 shows the two types of offset cancellation techniques. In the IOS configuration in (a), the preamp must be stable in the unity feedback configuration. In the OOS configuration in (b) the MOSFETs in the preamp must remain in saturation when the offset voltage is stored on the capacitors. If a differential amplifier is used as the preamp, this condition is usually easily met.

The size of the storage capacitors is based on three important considerations: (1) preamp or latch input capacitance, (2) charge injection, and (3) kT/C noise. For the IOS scheme, the input storage capacitance must be much larger than the input capacitance of the preamp, so that the storage capacitors don't attenuate the input signals. For example, if the storage capacitors have the same capacitance value as the input capacitance of the preamp, then one-half of the input signals reaches the preamp. For the OOS scheme, the storage capacitors should be much larger than the input capacitance of the dynamic latch.

Dynamic Current Mirrors

Using dynamic techniques can reduce the effects of threshold voltage mismatches in current mirrors. Consider the circuit of Fig. 25.37. When ϕ_1 is high and ϕ_2 is low (again, these clock signals are nonoverlapping), switches S1 and S3 are on, while switch S2 is off. A current I_{ref} flows through M1, setting its gate-source voltage. This information [the gate-source voltage (actually the charge) of M1] is stored on *C*. When S2 closes with S1 and S3 off, a current I_{out} equal to I_{ref}, neglecting channel length modulation, flows. This circuit behaves like a current source when ϕ_2 is high and as an open when ϕ_2 is low. The circuit shown in Fig. 25.38 shows a dynamic current mirror that operates continuously.

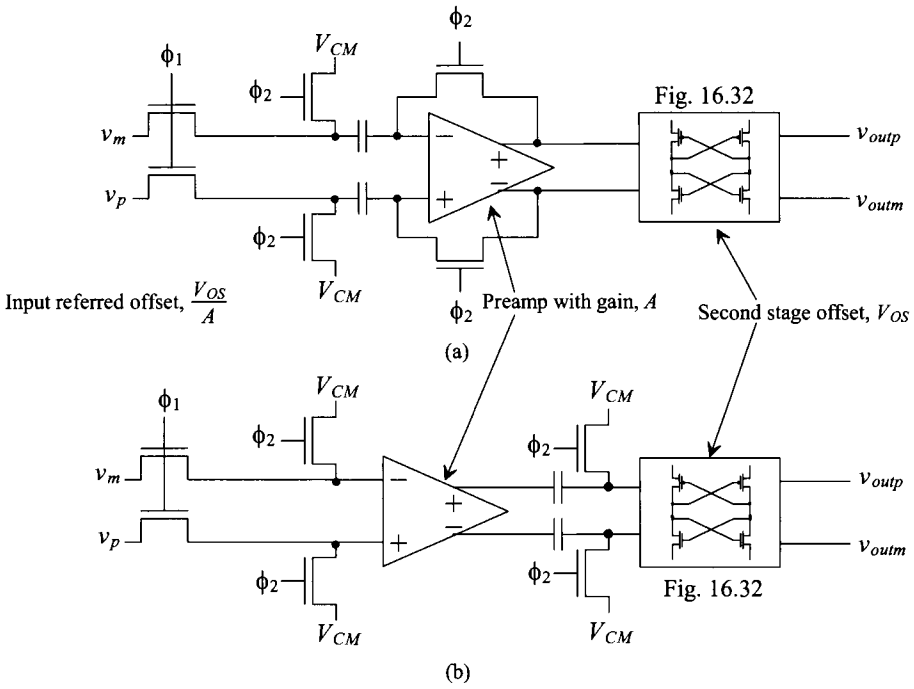

Figure 25.36 (a) Input offset storage (IOS) and (b) output offset storage (OOS).

When ϕ_1 is high, M2 sinks current, and when ϕ_2 is high, M1 sinks current. These circuits are useful in eliminating the mismatch effects and, thus, differences in the output currents, resulting from threshold voltage and transconductance parameter differences between devices. Since a single-reference current can be used to program the current in a string of current mirrors, only the finite output resistance of the mirrors causes current differences.

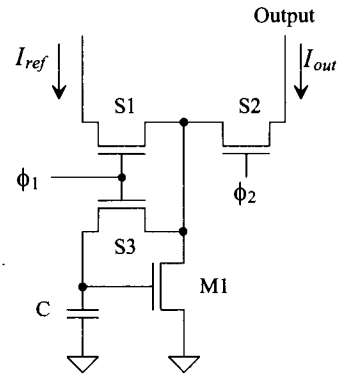

Figure 25.37 Dynamic biasing of a current mirror.

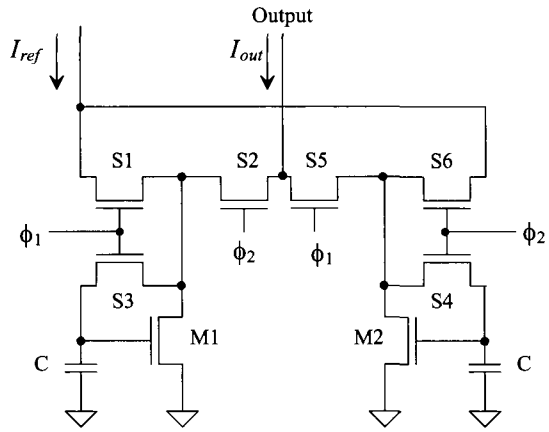

Figure 25.38 Dynamic current mirror that operates during both clock phases.

Dynamic Amplifiers

Figure 25.39 shows a dynamic amplifier. The circuit amplifies when ϕ is low and dynamically biases M1 and M2, and therefore does not amplify, when ϕ is high. If C1 and C2 are large compared to the input capacitance of M1 and M2, then the input AC signal, v_{in}, is applied to both gates. This biasing scheme makes the amplifier less sensitive to threshold and power supply variations. Other dynamic amplifier configurations exist, which have differential inputs and operate over both clock cycles.

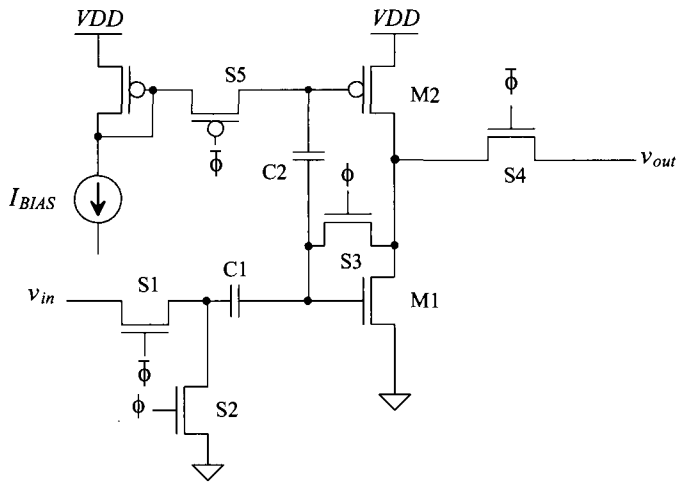

Figure 25.39 Dynamic amplifier used to reduce biasing sensitivity to power supply and threshold voltage.

ADDITIONAL READING

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PROBLEMS

In the following problems, where appropriate, use the short-channel CMOS process with a scale factor of 50 nm and a *VDD* of 1 V.

25.1 Using SPICE simulations, show the effects of clock feedthrough on the voltage across the load capacitor for the switch circuits shown in Fig. 25.40. How does this voltage change if the capacitor value is increased to 100fF?

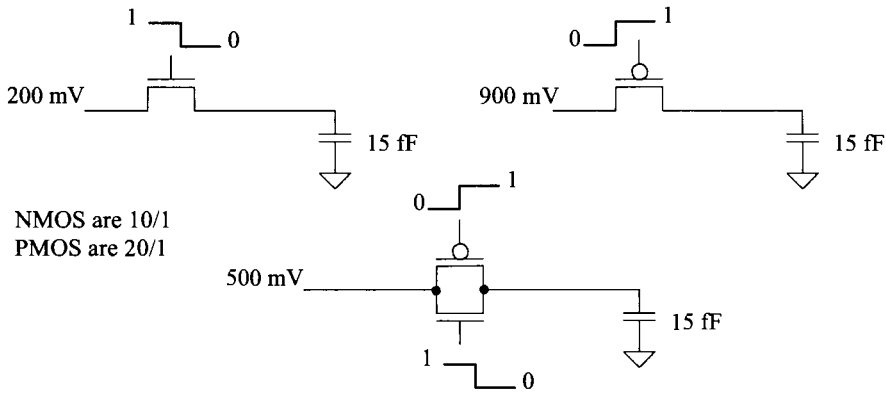

Figure 25.40 Circuits used in Problem 25.1 to show clock feedthrough.

25.2 Repeat problem 25.1 if dummy switches are used. Show schematics of how the dummy switches are added to the schematics.

25.3 Using a voltage-controlled voltage source for the op-amp (see Fig. 20.19 for example) with an open-loop gain of 10^6, use SPICE to show how the track-and-hold seen Fig. 25.8 operates with a sinewave input. What happens if the input sinewave's amplitude is above $VDD-V_{THN}$? Use a 100 MHz clock (strobe) pulse with a 50% duty cycle and an input sinewave frequency of 5 MHz. Note that the input sinewave should be centered around V_{CM} (= 500 mV).

25.4 Using the topology seen in Fig. 25.13a and the SPICE op-amp model in Fig. 25.18, show how both V_{in} and V_{CM} can be varied while the op-amp's inputs are equal, that is, $v_p \approx v_m$. Is the output common-mode voltage always at V_{CM} using the simple SPICE model for the fully-differential output op-amp in Fig. 25.18? Why or why not? Give an example supporting your answer.

25.5 Suppose, in Fig. 25.19, that instead of the two input sine waves being connected to ground they are tied (together) to a common mode signal (say a noise voltage). Show that a common mode signal (like a sine wave) won't change the circuits' output signals. The amplitude of the common-mode signal shouldn't be so large that the NMOS switches shut off.

25.6 Show that the switched-capacitor circuits shown in Fig. 25.41 behave like resistors, for $f << f_{clk}$, with the resistor values shown.

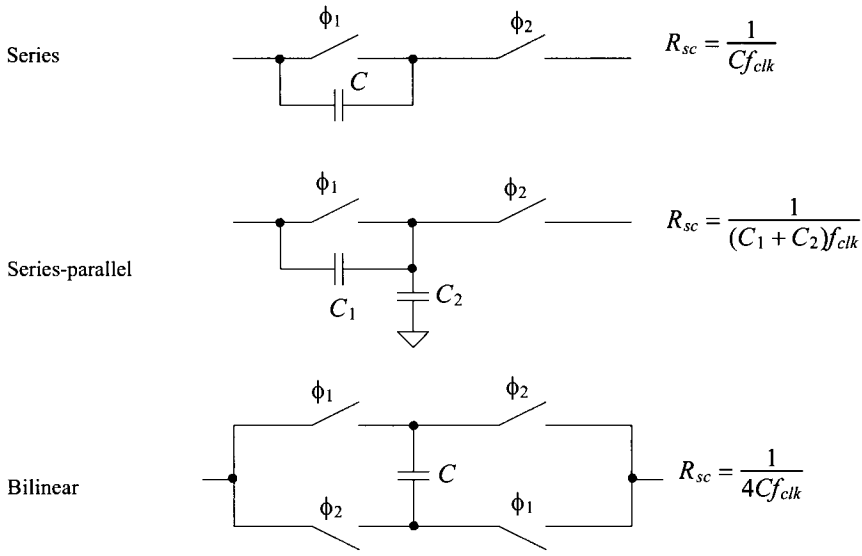

Figure 25.41 Alternative forms of switched-capacitor resistors.

25.7 Simulate the operation of the switched-capacitor resistor seen in Fig. 25.21. Plot the mean of the current flowing in the voltage sources v_1 or v_2 to show that the circuit actually behaves like a resistor. Comment on the selection of the bottom plate of the capacitor shown in Fig. 25.21a.

25.8 Comment on the selection of the bottom plate of C_F shown in Fig. 25.23.

25.9 Sketch the schematic, similar in form to Fig. 25.23, of the fully-differential switched-capacitor integrator made using a differential input/output op-amp. What is the transfer function of this topology?

25.10 Repeat Ex. 25.2 if the low-frequency gain is 40 dB and the zero is located at 50 kHz.

25.11 Using the results given in Eq. (25.29), plot the magnitude of v_{out}/v_{in} against f/f_{clk}. Comment on the resulting plot.

25.12 An important consideration in SC circuits is the slew-rate requirements of the op-amps used. In the derivation in Fig. 25.28, we assumed that a voltage source was connected to the input of the circuit. In reality, the input of the circuit is provided by an op-amp. When ϕ_1 goes high, in this figure, the capacitor C_I is charged to the input voltage v_{in} (= v_A). If C_I is 5 pF and f_{clk} is 100 kHz, estimate the minimum slew-rate requirements for the op-amp providing v_{in}.

25.13 Suppose that the op-amp in problem 25.12 is used with a feedback factor of 0.5. Estimate the minimum unity gain frequency, f_{un}, that the op-amp must possess.

25.14 Simulate the operation of the dynamic comparator shown in Fig. 25.35.