Chapter

26

Operational Amplifiers II

In the last chapter we saw that MOSFET switches cause charge injection and clock feedthrough in the circuits where they are used. To reduce the effects of these problems (and others), fully-differential op-amp topologies are used. As discussed in Sec. 25.2, the fully-differential output op-amp requires the design of a common-mode feedback (CMFB). The CMFB circuit keeps the op-amp's outputs balanced around a known voltage (generally the common-mode voltage of $V_{CM} = VDD/2$).

In this chapter we discuss the design of fully-differential output op-amps and CMFB circuits. Our discussion is centered around practical design where power, speed, offsets, and gain are (as usual) of importance. Throughout the chapter, the 50 nm process (with a *VDD* of 1 V) is used to illustrate the design techniques.

26.1 Biasing for Power and Speed

The biasing circuits we developed earlier were used for general analog design. In this chapter we want to design circuits that are used for very high speed with the least amount of power dissipation possible.

For high-speed design, we must use the minimum channel length ($L = 1$). However, using minimum channel lengths results in large mismatches between devices and low MOSFET output resistance (hence, why we used $L = 2$ for the designs presented earlier). The results are low gain and large input-referred offset voltages. Further, for low power design we want to use the lowest biasing currents possible. This (low biasing currents) is in direct conflict with high-speed design. As discussed in Ch. 9, the device speed figure-of-merit, FOM, was the transition frequency, f_T. Low biasing current is the same as low overdrive voltage. As seen in Eq. (9.55), using a low value of overdrive voltage results in slower circuits. Of course, if the overdrive voltage is too high, the MOSFET enters the triode region too soon. For general analog design, we set the overdrive voltage to 5% of *VDD*. For high-speed design, we might set the overdrive voltage to 10% of *VDD* or larger. *To minimize power and maximize speed, we will use minimum size devices.* For the NMOS, we'll use a 10/1. To match the drive, we'll use 20/1 for the PMOS devices. The question we need to answer having made these selections is: "Will these devices have the strength to drive a load capacitance quickly?"

26.1.1 Device Characteristics

Figure 26.1 shows the IV characteristics of our selected devices (an NMOS of 10/1 and a PMOS of 20/1). If we set the overdrive voltages to roughly 10% of *VDD* (here 100 mV), then knowing, from Table 9.2, the threshold voltages are 280 mV (typical), we can use gate-source voltages of, nominally, 400 mV with a corresponding drain current of 20 μA. If we want to increase the speed, then we must use a higher overdrive voltage (say bias the devices up at 50 μA).

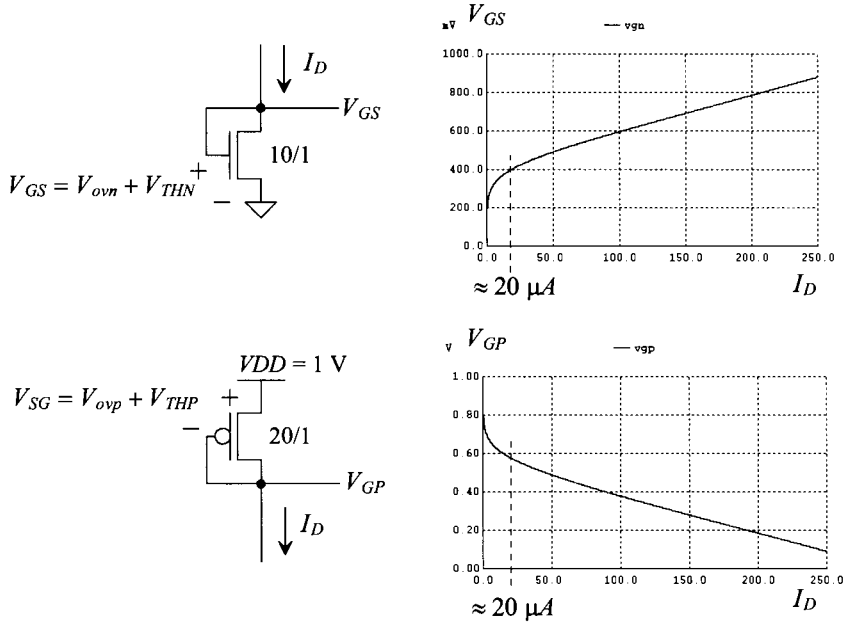


Figure 26.1 Gate-source voltages plotted against drain currents.

Next we need to determine if these devices will have the drive current needed to charge a specific size capacitor in the time required. Looking at Table 8.1 as a guide for selecting capacitor sizes, we see that using a 100 fF capacitor results in an RMS noise (because of the MOSFET switch thermal noise) of 200 μV. From Fig. 8.33 (the assumed PDF for thermal noise), the peak-to-peak value of this noise is (roughly) 1.2 mV. In this chapter *we'll use a load capacitance of 250 fF* for a peak-to-peak noise of 750 μV. Looking at the simulation results in Fig. 26.1, we see that a reasonable pulsed drain current estimate for the devices is 100 μA. The rate we can charge the load capacitor is then

$$\frac{dV_{out}}{dt} = \frac{I}{C_L} = \frac{100\ \mu A}{250\ fF} = 400\ mV/ns \tag{26.1}$$

If our clock frequency, f_{clk} , is 100 MHz, then half a clock cycle is 5 ns and the device sizes and bias conditions will likely be adequate (remembering that *VDD* is 1 V and V_{CM} is 500 mV). However, if our clock frequency approaches 1 GHz (or the load capacitance increases), then we must increase the widths of the devices (to get more drive) and the overdrive voltages (to get more speed).

26.1.2 Biasing Circuit

When designing the bias circuits earlier, Fig. 20.47 for example, our goals were to provide biasing for general analog design. Here, in this chapter, our goal is to design a bias circuit for our op-amp designs with minimum power dissipation. When designing biasing circuits fully-differential topologies have some advantages over the single output op-amps presented in Ch. 24. For example, our earlier bias circuit provided biasing, V_{pcas} and V_{ncas} , for the floating current sources used in the class AB output stages (see Fig. 24.29 for example). These bias voltages won't be needed here.

Towards understanding this last statement, consider the two-stage op-amp seen in Fig. 26.2. Consider what happens if the noninverting op-amp input, v_p , increases relative to the inverting input, v_m. The drain voltage of M1R drops while the drain voltage of M1L rises. The decrease in the gate voltage of M6R causes it to turn on and the output to go high. At the same time, the increase in the drain voltage of M1L causes M4R to shut off and thus so does M7R (giving class AB operation). In simple terms, we can yank the gates of M4 or M6 down independent of the diff-amp's tail current.

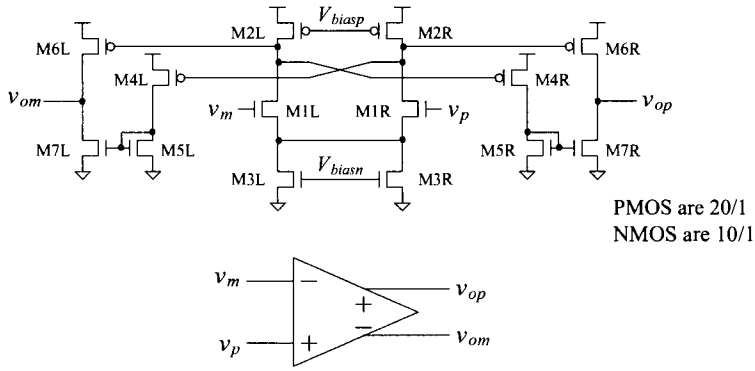


Figure 26.2 A two-stage fully-differential op-amp. Compensation and CMFB are not shown. Output stage operates class AB. See discussion in the next section concerning the output voltage of the diff-amp.

Layout of Differential Op-Amps

One of the common things we do in this chapter is draw schematics that are symmetrical. If we were to draw a line down the middle of the op-amp in Fig. 26.2, separating the left and right sides of the schematic, we could fold the left side of the schematic directly over onto the right side of the schematic and see a perfect match. For example, instead of drawing the diff-amp's tail current source (M3) as a single MOSFET with twice the width, we've drawn it as two MOSFETs in parallel, each having the same width. *Drawing schematics in this fashion is useful when doing layout.* We can fold the schematic in half and lay out like devices, e.g., M6L and M6R, directly next to each other. Further, then the outputs (and inputs) of the op-amp are laid out right next to each other.

Self-Biased Reference

Figure 26.3 shows the bias circuit we'll use in this chapter (see also Fig. 20.22 and the associated discussion). We used the length of 2 MOSFETs for the added amplifier to minimize power dissipation and boost the amplifier's gain. The current pulled from *VDD* is approximately 50 μA. Figure 26.4 shows the simulation results of how the current varies with changes in *VDD*. Notice how V_{biasn} is close to the 400 mV, and V_{biasp} is close to *VDD* – 400 mV (of course the absolute value of V_{biasp} varies with *VDD* but the ideal value of V_{SG} for the PMOS devices will be 400 mV). Note that, as discussed in Sec. 20.1.4, it is important to ensure that the reference is stable over all possible operating conditions and loads (connected to V_{biasn} and V_{biasp}). Notice that we aren't discussing how the reference currents vary with process shifts in the MOSFETs and the resistor. This is an important practical concern.

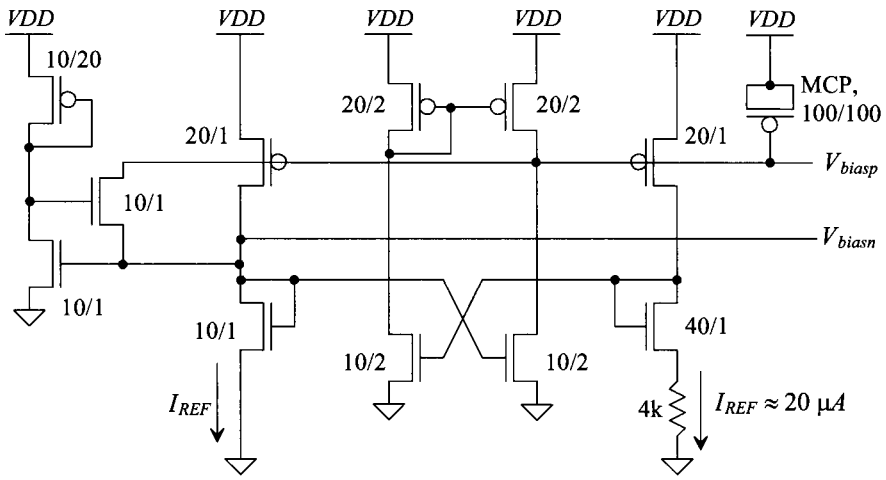


Figure 26.3 Biasing circuit used in this chapter. This bias circuit pulls approximately 50 microamps.

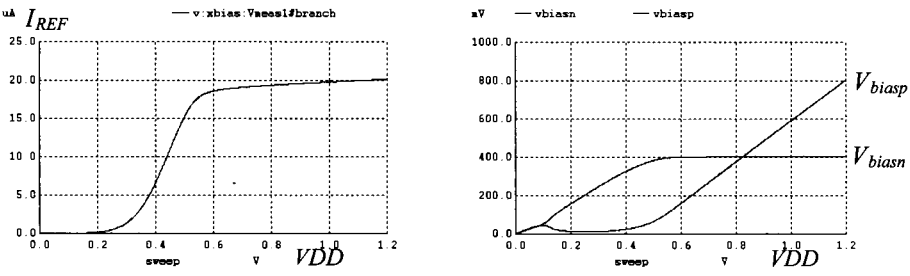


Figure 26.4 Simulating how the reference current changes with VDD.

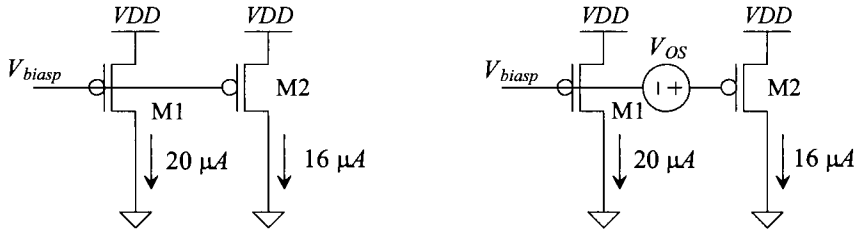
26.2 Basic Concepts

Before we discuss the design of op-amps, let's look at some basic concepts that will be useful when evaluating a specific op-amp topology.

Modeling Offset

In a real circuit, especially an analog circuit designed with minimum length devices, mismatches can be a significant factor in the selection of an op-amp topology. In a SPICE simulation, all of the MOSFETs are perfectly matched. We have to come up with a method, in SPICE, to determine an op-amp's sensitivity to offsets.

Consider the circuit in Fig. 26.5. In (a) the measured currents should be equal. Both MOSFETs V_{SG}s and V_{SD}s are equal (and they are the same size). However, for whatever reason (e.g., threshold voltage mismatch), there exists a mismatch between the two devices that causes a difference in their drain currents. We can model this mismatch in a SPICE simulation, as seen in (b), by adding a DC voltage source in series with the gate of M2. For a general design, we can insert these offset voltages at various points in the circuit and verify that the circuit still functions correctly. The next question that needs answering is: "What value of V_{OS} should be used?" While no absolute answer can be given here, **we'll use a V_{OS} of 50 mV** (5% of *VDD* or roughly 20% of the threshold voltage). The reader might feel that this value is way too high. However, if we can design circuits that function properly over the process, voltage, and temperature (PVT) variations with an offset this large, it is likely the op-amp will be difficult to "break."



(a) M1 and M2 are mismatched.

(b) M1 and M2 are perfectly matched (as in a SPICE simulation).

Figure 26.5 How we add an offset into the circuit to model mismatch.

A Diff-Amp

Figure 26.6a shows a basic diff-amp without an offset. This offset-free diff-amp has simulated output voltages of 700 mV. The diff-amp in (b) is simulated with an input-referred offset voltage of 50 mV. The polarity of the offset doesn't matter because it simply swaps the two output voltage values. In other words, we could have put the same polarity offset on the other input of the diff-amp and swapped the voltages on the output of the op-amp. We put the offset voltage on the op-amp's input because the input has the greatest effect on the diff-amp's output voltages. Note: we can think of the 50 mV as an input signal causing an output signal difference, from the ideal 700 mV, of 900 mV –550 mV or 350 mV (assuming linear operation). This indicates the gain of the diff-amp is only 7!

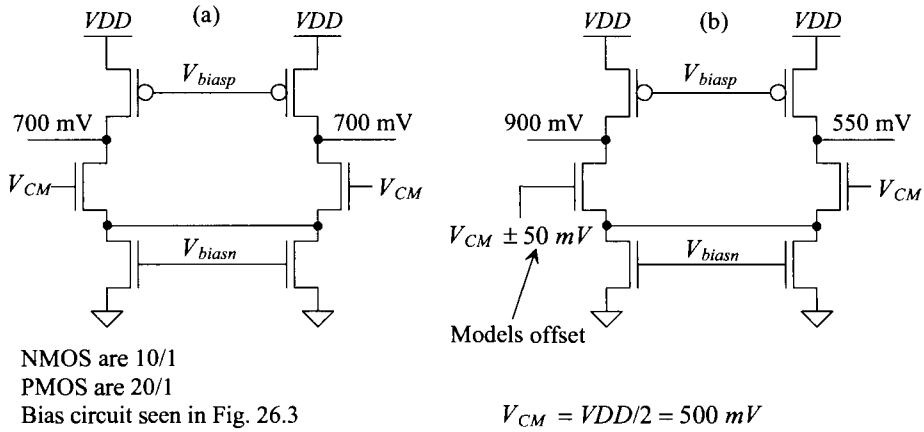


Figure 26.6 Comparing the diff-amp's output voltages with and without an offset.

The simulation results seen in Fig. 26.6 give some practical information that we need to consider. To begin, remember from Ch. 24 that we frequently use the diff-amp's output to bias the next stage (see Figs. 22.8 and 24.2). With a *VDD* of 1 V and a V_{SG} of nominally 400 mV, V_{biasp} is roughly 600 mV, as seen in Fig. 26.4. However, as seen in Fig. 26.6a, the diff-amp's output is 700 mV. The result, when the diff-amp is used with a second-stage and feedback, is an additional input-referred offset. It would be nice to know that the outputs of the diff-amp, in the ideal case, go to a known value (preferably a voltage that can be used to bias the next stage). The diff-amp in Fig. 26.6 is an example of two current sources, the PMOS biased with V_{biasp} and the NMOS biased with V_{biasn}, fighting each other for control of the output voltage. In general, we want to avoid this situation.

A Single Bias Input Diff-Amp

Figure 26.7 shows a diff-amp that generates its own bias reference for the PMOS devices. Notice that the two gate-drain-connected PMOS devices behave simply like a MOSFET with twice the width of the other two PMOS devices. Similarly, the four NMOS devices that are biased from V_{biasn} behave like a MOSFET with four times the width of the other NMOS devices. When the diff-amp's inputs are equal, the same current, *I*, flows in all of the MOSFETs. If the + diff-amp input is raised significantly above the – input, all of the bias tail current flows in the left two NMOS devices of the diff-amp (each will conduct 2*I*). The current flowing in the gate-drain-connected PMOS device, in either case, is the same, 2*I*, keeping the PMOS's gate voltage constant. The outputs of this diff-amp can be used to bias the next stage. Offsets, however, cause the diff-amp's outputs to vary from their ideal values. One drawback to using this diff-amp is that it dissipates twice the power of the diff-amp in Fig. 26.6. Another drawback is the larger input capacitance.

The Diff-Amp's Tail Current Source

Notice that we are not using a cascode tail current source to bias the diff-amps in this chapter, as we did in earlier chapters. We're avoiding the cascode structure because we'd need an additional bias voltage (resulting in more power dissipation). In a

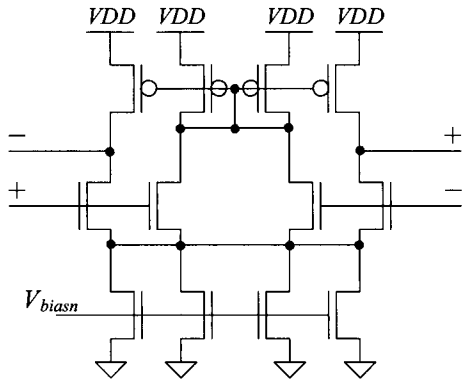


Figure 26.7 A fully-differential diff-amp that generates its own bias for the PMOS.

fully-differential op-amp topology (both the inputs and the outputs of the op-amp, with feedback, are double-ended signals swinging around V_{CM}), the input common-mode voltage of the op-amp is constant (= V_{CM}). The common-mode rejection ratio isn't as important when the input common-mode voltage of the op-amp doesn't vary.

Using a CMFB Amplifier

Another possible way to set the diff-amp's output voltages to a known value is seen in Fig. 26.8. An amplifier (called a common-mode feedback amplifier or CMFB amplifier) is used to amplify the difference between the average of the diff-amp's outputs and V_{biasp}. If the gain of the CMFB amplifier is large, then the average of the two outputs will be very close to V_{biasp}. Note that the CMFB amplifier's output signal, V_{CMFB} , is common, through M1L and M1R, to both outputs. Any variation in V_{CMFB} affects each output by the same amount. This is important because all we want the CMFB amplifier to do is make

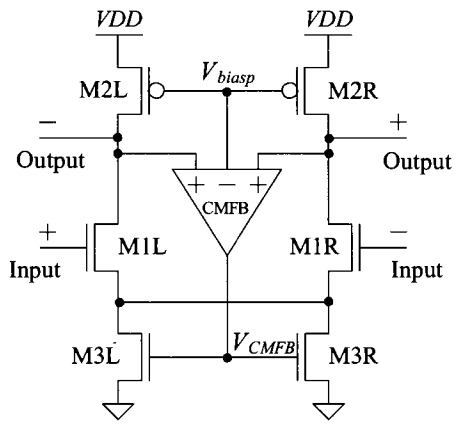


Figure 26.8 Using a common-mode feedback (CMFB) amplifier to set the output voltages.

sure that the diff-amp's outputs vary around V_{biasp}. The CMFB amplifier shouldn't affect the differential amplification in the diff-amp. When the diff-amp's outputs are equal (the inputs to the diff-amp are equal and neglecting offsets), they should be V_{biasp}.

Figure 26.9 shows one possible implementation of a CMFB amplifier. When the + inputs (noticing the PMOS connected to these inputs have half the width of the other PMOS) are equal to V_{biasp}, the currents that flow in M1 and M2 are 20 μA. This provides the proper mirroring action to the diff-amp (M3L, R) in Fig. 26.8. If the average of the + inputs moves above the – input, the current flowing in M2 decreases and the current in the 200/1 PMOS increases. This causes V_{CMFB} to increase. The result is that M3L and M3R turn on more and pull both of the outputs in Fig. 26.8 down (until their average is equal to V_{biasp}). Several concerns exist with this topology. To begin, whenever we employ feedback, we must be concerned with stability. To stabilize the CMFB loop, we can add capacitors to the outputs of the diff-amp (inputs to the CMFB amplifier). We may be able to stabilize the CMFB loop by adding capacitors to the CMFB amplifier's outputs. However, since we will need compensation capacitors for compensating the differential action of the op-amp, we might as well use these capacitors for both loops. The other concern with the CMFB amplifier in Fig. 26.9 is the input common-mode range. When the CMFB amplifier's + inputs move significantly away from the – input, we don't get the correct balancing. This keeps large signal swings on the diff-amp's outputs in Fig. 26.8 from being balanced around V_{biasp}.

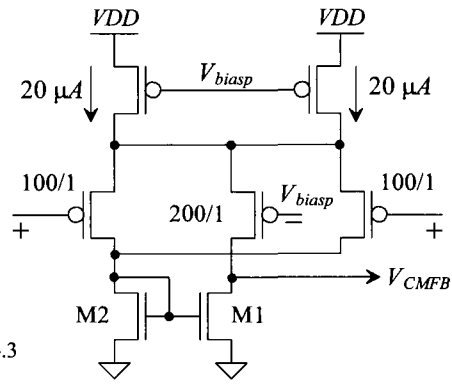
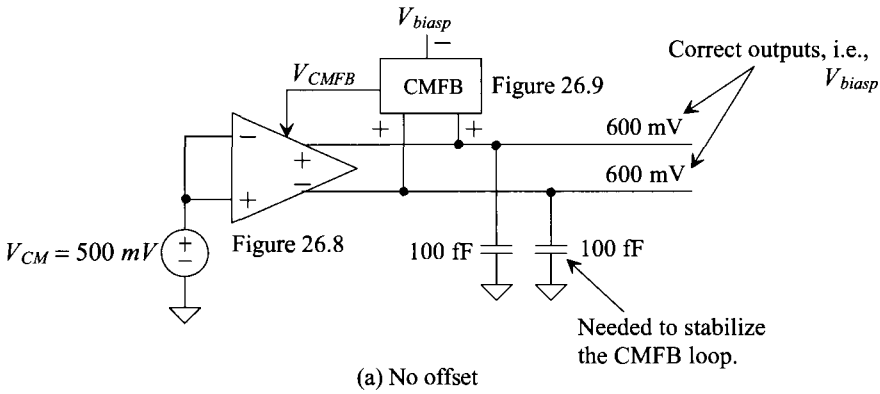
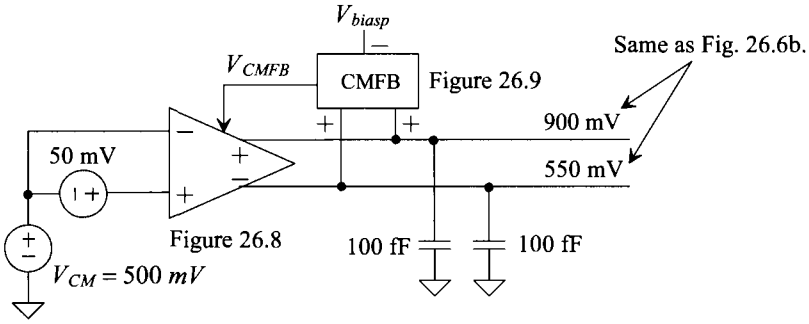


Figure 26.9 Implementation of the CMFB amplifier in Fig. 26.8.

Figure 26.10 shows simulation results using the CMFB amplifier in Fig. 26.9 with the amplifier in Fig. 26.8. The addition of the capacitors stabilizes the CMFB loop *(we need to discuss this further)*. In (a) we see the correct balancing. The CMFB loop adjusts the diff-amp's output voltages to V_{biasp}. In (b) we re-simulate with an offset and see that the CMFB circuit isn't balancing the outputs. If it were, we would see one output above V_{biasp} by some amount and the other output below V_{biasp} by the same amount. With these output voltages (the inputs to the CMFB amplifier), one of the PMOS devices on the input of the CMFB is off and we don't get proper amplifier action. *We must use a CMFB circuit that can balance the outputs over the entire range of diff-amp output voltages.*



(a) No offset



(b) With a 50 mV offset. Note how the CMFB isn't doing anything.

Figure 26.10 Simulating the operation of the CMFB circuit in Fig. 26.9.

Compensating the CMFB Loop

Consider the schematic seen in Fig. 26.11. The diff-amp behaves like an operational transconductance that can be compensated, as discussed in Sec. 24.3 (see Eq. [24.44]). The CMFB loop can be compensated in a similar fashion. The AC common-mode signal is represented in this schematic as v_c. If the gain of the CMFB amplifier is A_c, then following the procedure leading to Eq. (24.44), we can write the unity-gain frequency of the CMFB loop as

$$f_{un,cm} = \frac{A_{cm} \cdot g_{mn}}{2\pi C_L} \tag{26.2}$$

If we want to compensate the CMFB loop with the same load capacitance used to compensate the differential forward signal path, then we must ensure that the gain of the CMFB amplifier is less than or equal to unity,

$$A_{cm} \leq 1 \tag{26.3}$$

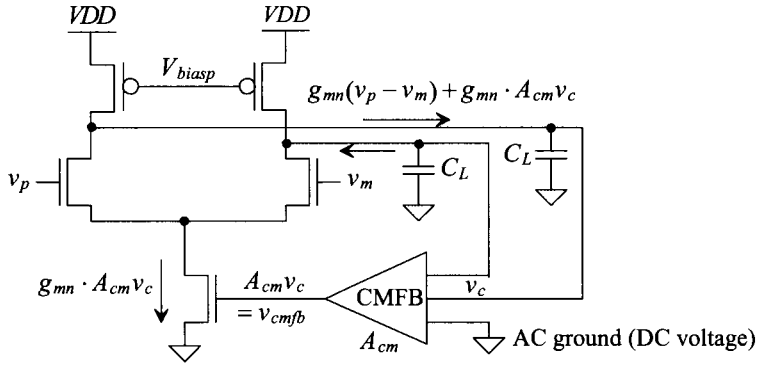


Figure 26.11 Schematic view of differential and CM feedback.

Reviewing the CMFB amplifier in Fig. 26.9 that has a current mirror active load, we see that A_{cm} is greater than 1. Removing the capacitors in Fig. 26.10 and resimulating will show that the CMFB loop is unstable. The added capacitors are relatively large and will overcompensate the differential signal path of the diff-amp. What we need to do is reduce the gain of the CMFB amplifier or reduce the CMFB loop's forward gain.

Towards reducing the gain, examine the CMFB amplifier seen in Fig. 26.12. This is the same amplifier topology seen in Fig. 26.9 except that here we've used a diode-connected load instead of a current mirror load (to reduce the gain). The schematic is drawn symmetrical around its center for ease of layout, as discussed earlier. Note that we used the common-mode voltage in this schematic, V_{CM}, as the voltage that the outputs of the amplifier will swing around (the more general case) rather than V_{biasp} as used in Fig. 26.10. Using this CMFB amplifier in the circuits of Fig. 26.10 (where the diff-amp of Fig. 26.8 has a low gain) won't precisely balance the outputs. The loop gain around the CMFB loop isn't large enough for proper operation. As we saw in Ch. 24, low first-stage gain can be remedied by using a telescopic input (cascode-load diff-amp) or a folded-cascode OTA. The other problem with this CMFB amplifier, again, is the limited allowable swing on the + inputs. As we've already seen, the input common-mode range limits the range of output voltages this CMFB can balance properly.

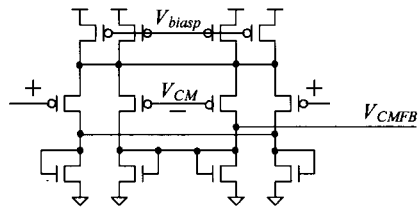


Figure 26.12 A CMFB amplifier with a gain of nominally unity.

Towards reducing the CMFB loop's forward gain, consider breaking the diff-amp's tail current up into parts, as seen in Fig. 26.13. The CMFB signal is applied to only one gate of the tail current. When compared to the topology in Fig. 26.8, the forward gain of the CMFB loop is halved. Further reduction can be implemented by adjusting the sizes of the transistors to further reduce the strength of the V_{CMFB} signal. *This is a common practical way of making CMFB loops stable.*

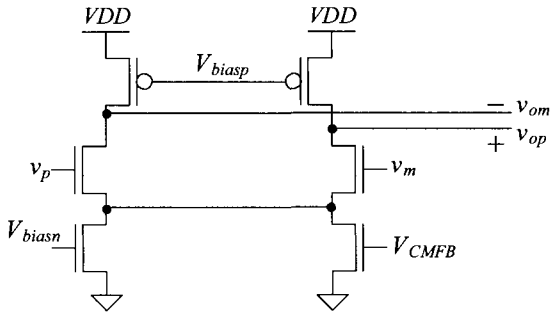
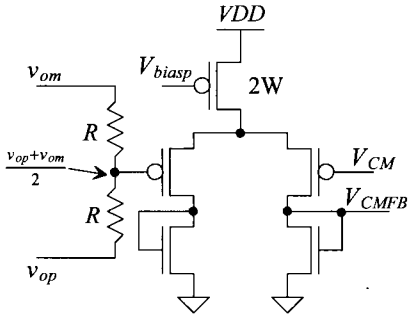


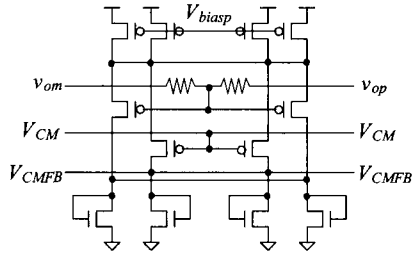
Figure 26.13 Reducing the forward gain of the CMFB loop.

Extending the CMFB Amplifier Input Range

The problem with the previous CMFB amplifier topologies based on a diff-amp is the diff-amp's limited input range. It's desirable to have a CMFB amplifier that functions over the entire range of possible amplifier output voltages. Towards this goal, consider the conceptual schematic in Fig. 26.14a. The resistors average the two outputs. This average is compared with the common-mode voltage (or a bias voltage as used in Fig. 26.8). Figure 26.14b shows the practical implementation of the amplifier for symmetry (at the cost of extra power dissipation). The practical problem with this topology is the



(a) Using resistors to average differential output signals.



(b) Symmetrical implementation of the CMFB circuit in (a).

Figure 26.14 Increasing CMFB amplifier input range.

loading by the resistors. If we were to connect this CMFB amplifier in the circuit configuration of Fig. 26.8, the resistors, unless they are huge (>100k) would load the differential amplifier and lower its gain. This topology is used, most often, on the output of an op-amp that has output buffers (and can thus drive resistive loads).

When using resistors for averaging in high-speed applications, we may have some parasitic effects that should be considered. The output signals have to charge, through the averaging resistors, the input capacitance of the MOSFET, as seen in Fig. 26.15. To ensure that the balancing action works at high speeds, capacitors (shown dashed in the figure) can be added, shunting the resistors. These capacitors can be very important if the size of the resistors is increased to reduce their loading on the output of the amplifier.

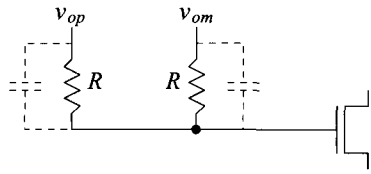


Figure 26.15 Adding parasitic capacitances across the resistors to compensate for the input capacitance of the MOSFET.

Dynamic CMFB

Figure 26.16 shows a switched-capacitor (SC) implementation of a CMFB circuit. The clocks, as in all SC circuits, are nonoverlapping (never high at the same time) clock signals, as seen in Fig. 25.28. The SC resistors are formed with the C_1 capacitors. The C_2 capacitors are used for the high-speed averaging just discussed (the dashed capacitors in Fig. 26.15). The SC resistors, as we'll see in a moment, perform both the averaging and the differencing needed in a CMFB amplifier. If the ϕ_2 controlled switches connected to amplifier's outputs, v_{op} and v_{om}, are transmission gates, the circuit can provide balancing from *VDD* to ground.

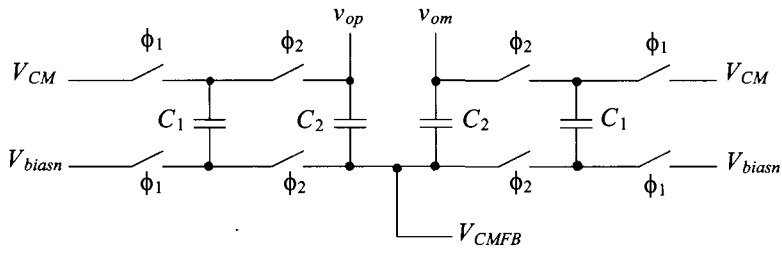


Figure 26.16 A switched-capacitor CMFB circuit.

To describe the operation of this circuit, consider the case when ϕ_1 is high. During this time, the total charge stored on both C_1 capacitors is

$$q_1 = 2 \cdot (V_{biasn} - V_{CM}) \cdot C_1 \tag{26.4}$$

When the ϕ_1 switches shut off, the ϕ_2 switches turn on. The total charge on both capacitors is then

$$q_2 = (V_{CMFB} - v_{op}) \cdot C_1 + (V_{CMFB} - v_{om}) \cdot C_1. \tag{26.5}$$

The change in V_{CMFB} is proportional to difference in q_1 and q_2 or

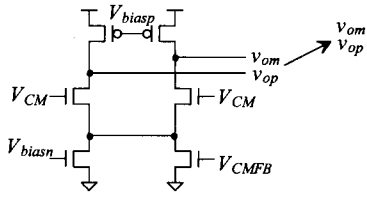
$$\Delta V_{CMFB} \cdot 2(C_1 + C_2) \propto (q_1 - q_2) \tag{26.6}$$

This equation is important because it shows the CMFB voltage will continue to change until the two charges, q_1 and q_2 , are equal. Note that if v_{op} and v_{om} are balanced around V_{CM} , their net contributions, when ϕ_2 goes high, to V_{CMFB} are zero. Looking at the difference in the charges, we get

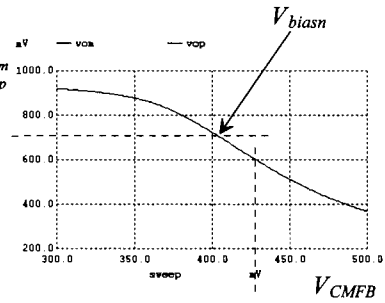
$$q_1 - q_2 = 2C_1\left(V_{biasn} - V_{CMFB} + \frac{v_{op} + v_{om}}{2} - V_{CM}\right) \tag{26.7}$$

This equation is quite interesting. Ideally, V_{CMFB} is equal to V_{biasn} , and the average of the outputs is equal to the common-mode voltage. If the actual value of V_{CMFB} , for balanced outputs, is 10 mV offset from V_{biasn} , then the average of the outputs will be 10 mV offset from V_{CM}. The offsets can occur because of improper device sizing (under ideal conditions the currents don't sum correctly) or mismatches.

As an example of where this offset can come from, consider the amplifier seen in Fig. 26.17 (also in Figs. 26.6 and 26.13). As seen in Fig. 26.6a, when V_{CMFB} is V_{biasn} or roughly 400 mV, the outputs of the diff-amp are 700 mV. As seen in Fig. 26.10 and the associated discussions, it can be useful, for next stage biasing, if the outputs are set to V_{biasp} (600 mV). From Fig. 26.17, the value of V_{CMFB} at this output voltage is roughly 425 mV or a 25 mV offset.



NMOS 10/1
PMOS 20/1
Bias circuit from Fig. 26.3



Value of CM feedback voltage when the outputs are 600 mV.

Figure 26.17 Plotting the output voltages as a function of the CM feedback voltage.

26.3 Basic Op-Amp Design

Reviewing the data in Table 9.2, we see that the open circuit gains are 25 (NMOS) and 50 (PMOS). In this chapter we both increased the biasing current and reduced the channel length from the values used in Table 9.2. Each of these changes has the effect of reducing the MOSFET's open circuit gain. If, for example, the open circuit gains are both now 10, then a common-source amplifier with current source load will have a gain of 5. A cascode amplifier will have a gain of 25, and a two-stage op-amp using a cascoded first-stage a gain of only 125. In other words, we adjusted our biasing for high-speed operation but we are going to face some issues with getting large open-loop gain.

This is a good time to remember the useful simulation netlists that we've developed. Figure 26.18 shows the IV curves, output resistance, and transconductance for a 10/1 NMOS and a 20/1 PMOS based on Figs. 9.31 to 9.33. Notice in (a) that the NMOS's drain current at a V_{GS} of 400 mV and a V_{DS} of 100 mV is approximately 13 μA. The PMOS's drain current under the same conditions, (b), is closer to 9 μA. In (c) and

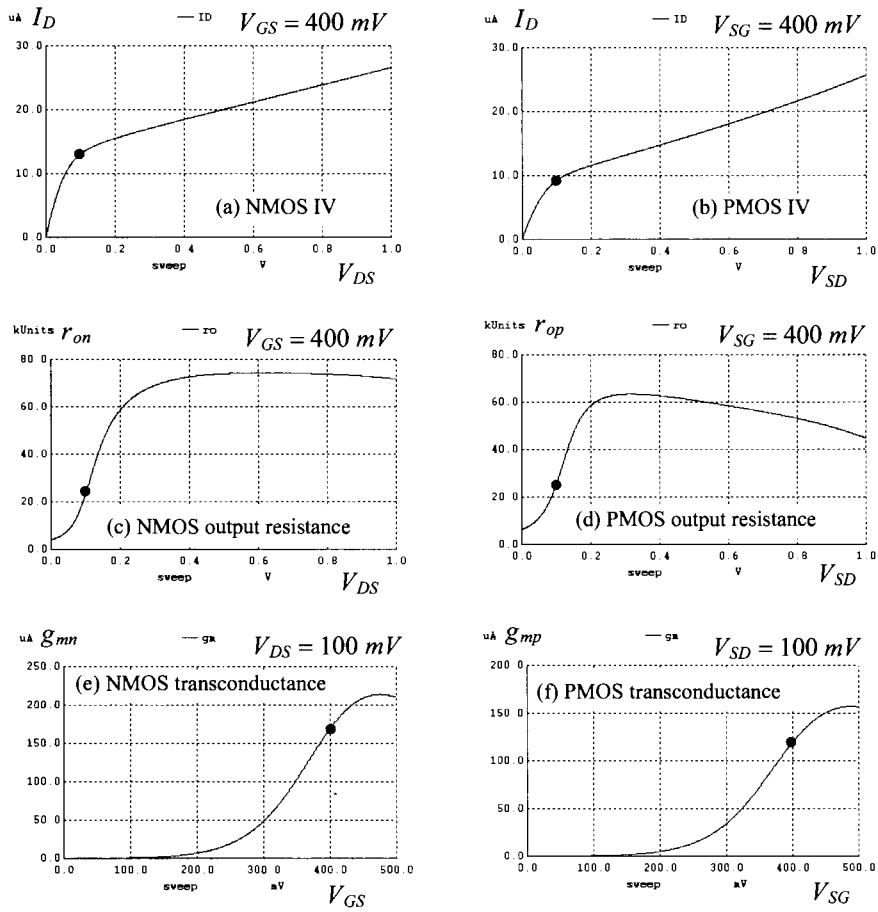


Figure 26.18 Characteristics of NMOS (10/1) and PMOS (20/1) devices.

(d), at a V_{DS} of 100 mV, the output resistance is only 25k. Using the transconductances in (e) and (f), the open circuit gains are, roughly, 4.375 (NMOS) and 3.125 (PMOS). In the actual circuits, the biasing points will vary (but in any case the gain of single stages will be low).

The Differential Amplifier

Figure 26.19 shows a cascode load diff-amp based on the topology seen in Fig. 26.7. Seen in the figure are typical values for the voltages in the circuit assuming gate-source voltages of 400 mV and, for the bottom two rows of NMOS devices, drain-source voltages of 100 mV. Notice how we used V_{biasn} to bias the second row of PMOS devices, which puts 200 mV across the drain-source voltages of the PMOS devices. This results in larger gain and reduced output swing. Diff-amp output swing is not an issue if this amplifier is used as the first-stage in a two-stage op-amp.

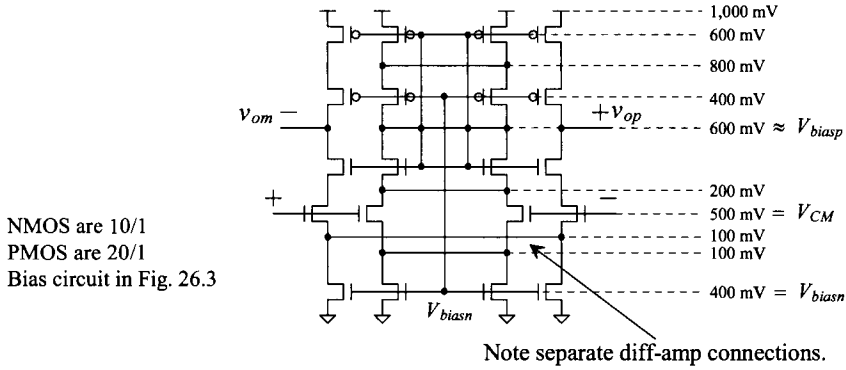


Figure 26.19 Fully-differential cascode diff-amp.

Figure 26.20 shows how the output voltages of the diff-amp in Fig. 26.19 vary with changes in V_{CM}. A 200 mV change in the common-mode voltage results in a, roughly, 50 mV change in the diff-amp's common-mode output voltages. Looking at Fig. 26.1, we see that the change in the drain current will be, again roughly, ± 5 μA around the quiescent value set with V_{CM} equal to 500 mV.

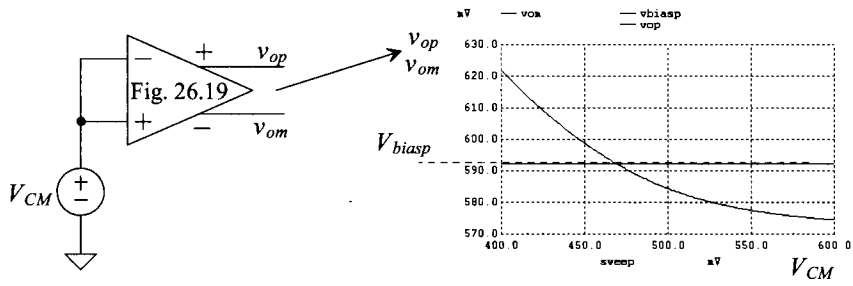


Figure 26.20 Varying the common-mode voltage and looking at the output.

Figure 26.21 shows the DC characteristics of the diff-amp. The gain is approximately 40. An important concern is how the mismatches in the MOSFETs used in the diff-amp affect the operation and biasing of the amplifier. Before discussing this issue, let's add the second stage and CMFB circuitry to form an op-amp. Note that, with a diff-amp gain of 40, and a second stage gain of 10, our op-amp's open loop gain will only have a value in the hundreds.

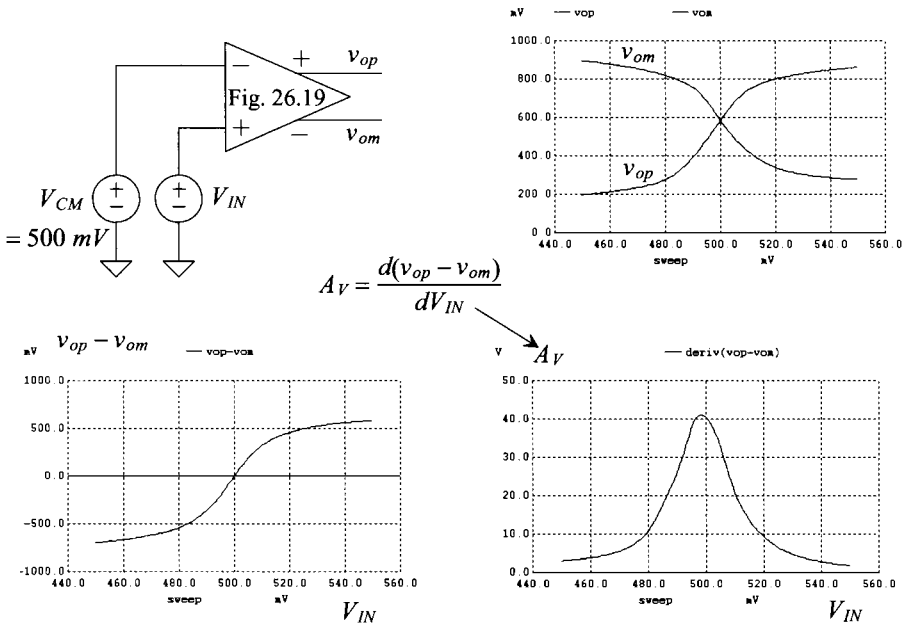
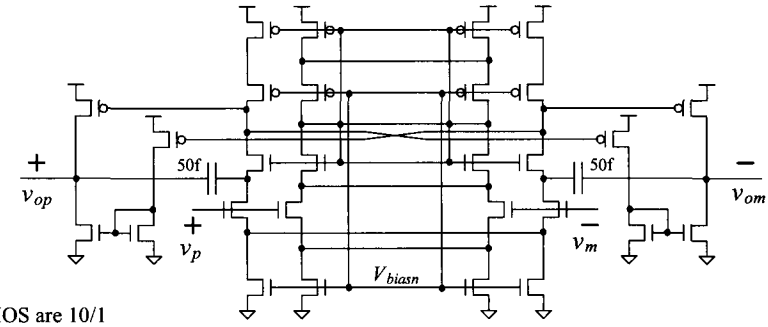


Figure 26.21 DC behavior and gain of the diff-amp in Fig. 26.19.

Adding a Second Stage (Making an Op-Amp)

Figure 26.22 shows a two-stage op-amp without CMFB circuit. The second stage of the op-amp operates class AB, as seen in Fig. 26.2, and the associated discussion. We've spent a considerable amount of time discussing how the output voltages of the diff-amp are approximately V_{biasp}. It should be clear after studying the op-amp in Fig. 26.22 why this is important. This voltage sets the quiescent current flowing in the output stages. There are eight vertical branches in this op-amp, so we can estimate the current pulled from *VDD* under quiescent conditions as 160 μA.

We used 50 fF capacitors for compensation in this op-amp. We can estimate the slew-rate limitations caused by the diff-amp driving the compensation capacitor, Eq. (22.34), as $20\ \mu A/50\ fF = 400\ mV/ns$. Using a class AB output stage, we don't have slew-rate limitations associated with driving a load capacitance from a constant current source. As discussed at the beginning of the chapter, the output MOSFET's drain currents can be pulsed to a value greater than 100 μA. When the op-amp is driving a 250 fF capacitive load, the speed limitations associated with charging the load capacitance are similar to the limitations we get when the diff-amp drives the compensation capacitor.



NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.3

Figure 26.22 Basic two-stage op-amp without CMFB.

Figure 26.23 shows the DC characteristics of the op-amp in Fig. 26.22 where, once again, we've held the inverting op-amp input at the common-mode voltage and swept the voltage on the noninverting input. Notice how the outputs swing all the way from ground to *VDD* (= 1V). Further notice how the differential output voltage swings from −1 to +1 V (a doubling in the output swing as discussed in Sec. 25.2.) The op-amp's DC gain is approximately 500 without a DC load. Notice how the two op-amp outputs cross at 400 mV (not at V_{CM} where they should). We'll discuss the CMFB in a moment.

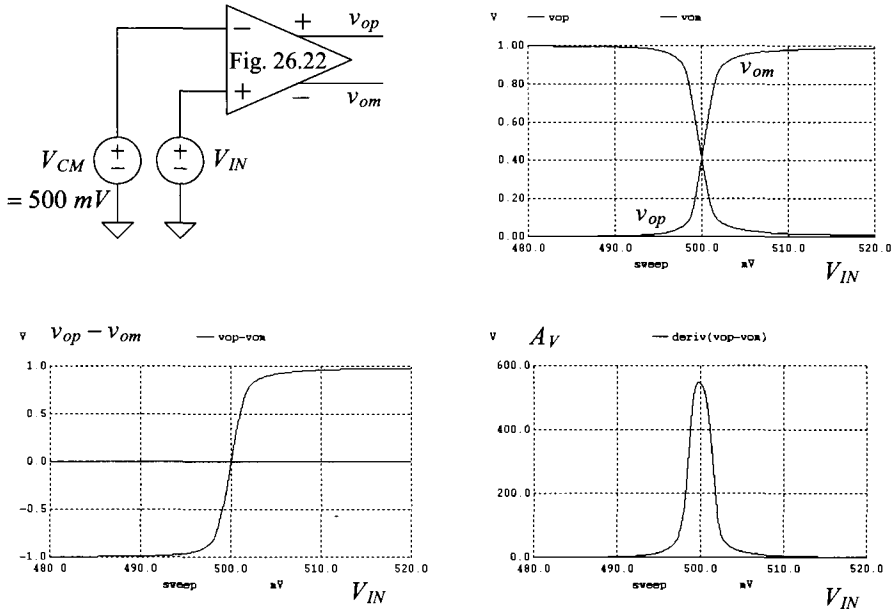


Figure 26.23 DC behavior and gain of the op-amp in Fig. 26.22.

Step Response

To determine both the stability of the op-amp in Fig. 26.22 and the settling time under certain loading conditions, consider the configuration seen in Fig. 26.24. We used relatively small resistors, 20k, in this circuit to reduce the RC time constant associated with the outputs of the op-amp charging the input capacitance of the op-amp. If, for example, the input capacitance of the op-amp is 25 fF (from parasitics and the MOSFETs used on the op-amp's input), then the RC time associated with charging this capacitance through a 20k resistor is 0.5 ns. As seen in Fig. 26.24, the settling time is approximately 2.5 ns so this RC time can have a significant effect on the settling time and stability of the circuit (important).

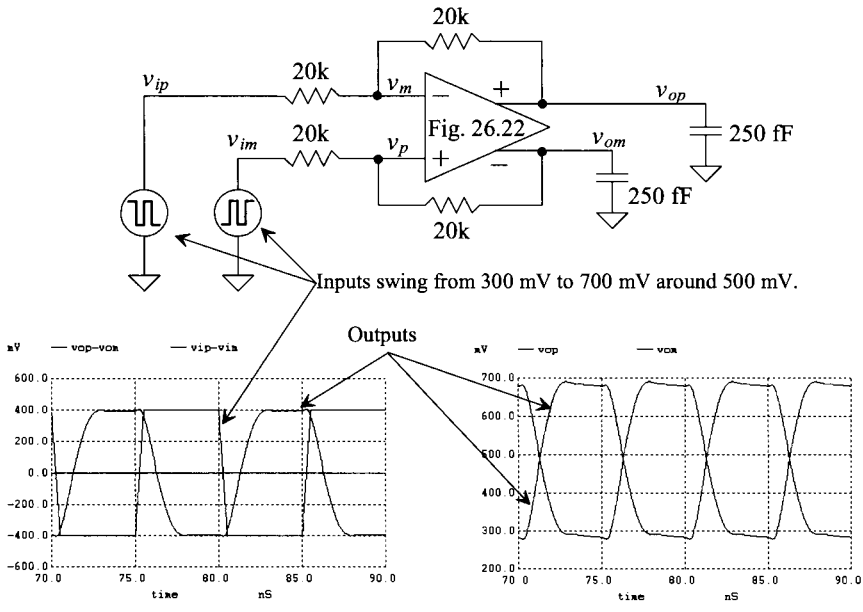


Figure 26.24 Step response of the op-amp in Fig. 26.22 driving 250 fF load capacitors and 20k feedback resistors.

Notice how, in Fig. 26.24, we used input signals that don't swing rail-to-rail. Since we don't have a CMFB circuit in the op-amp, the exact common-mode output voltage is an unknown. It may be 400 mV or it may be 600 mV. We get some help in setting the circuit's output common-mode level by using input signals with common-mode voltages of 500 mV and DC feedback. Looking at the simulation results in Fig. 26.24, we might get a false sense of not needing a CMFB circuit. To illustrate this is indeed a false sense, consider the sample-and-hold seen in Fig. 26.25 (see also Fig. 25.19). When the ϕ_1 switches are closed, the op-amp's inputs and outputs should be held to $V_{CM} \pm V_{OS}$ (the op-amp is placed in the follower configuration). As seen in the figure, the outputs during this time are driven close to 400 mV. On closer inspection, we see the output common-mode level is wandering downwards until eventually the op-amp shuts off.

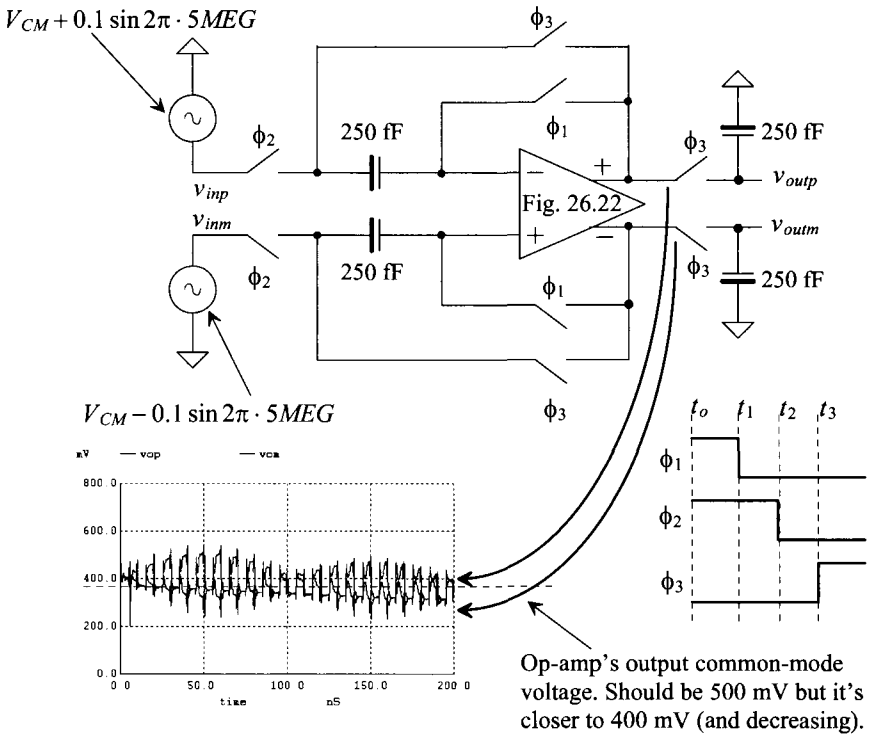


Figure 26.25 A sample-and-hold circuit. Notice how the output common-mode voltage is wandering.

Adding CMFB

Figure 26.26 shows how we can modify the basic op-amp to allow for a CMFB signal input. If the outputs of the op-amp (their average or common-mode voltage) are too high,

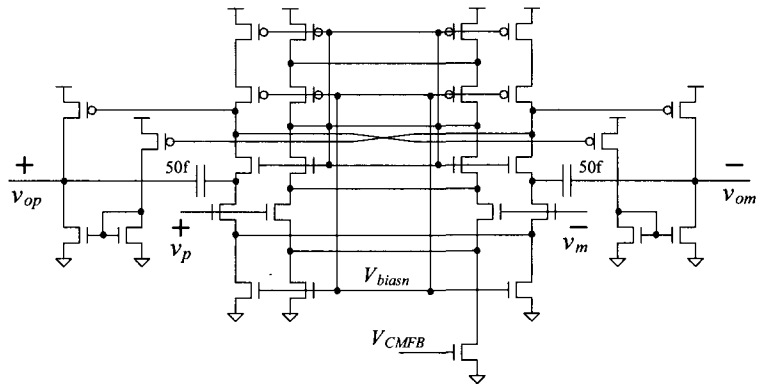


Figure 26.26 Modifying the op-amp for a CMFB input signal.

V_{CMFB} goes up. This causes the output voltage of the diff-amp to go up (increasing V_{CMFB} causes the bias current in the center MOSFETs of the diff-pair to increase). An increase in the diff-amp's output voltage lowers the quiescent current flowing in the output buffers, causing the output voltage to move downwards. This is a good time to remember one of the fundamentals from Ch. 20, namely, if two MOSFET gate-source voltages are equal and they have the same drain current, then their drain-source voltages must be equal. For the output buffer in Fig. 26.26, this means that as we reduce the drain currents flowing in the output buffer (by driving V_{CMFB} high), the gate-source voltages of the NMOS devices decrease. Because of the fundamental concept just mentioned, this causes the output voltages of the op-amp to decrease. Figure 26.27 shows the op-amp's output voltage change with V_{CMFB}. For stability concerns, it's of interest to determine the gain from the CMFB input to the outputs. From the simulation, the gain is approximately 25 (about 10 times less than the differential gain). The lower forward CMFB gain allows us to use a diff-amp with a current mirror load for the CMFB amplifier (discussed next).

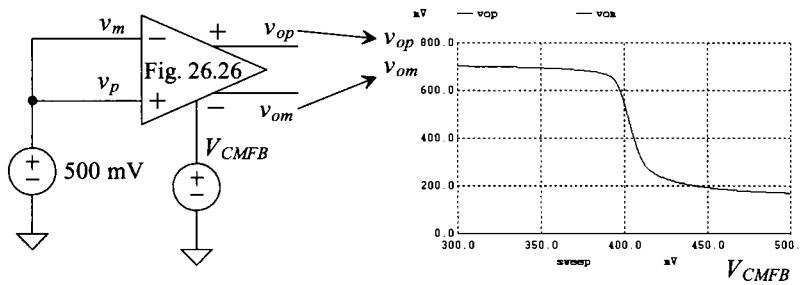


Figure 26.27 The CMFB input to output relationship. The gain is approximately 25 (considerably less than the forward differential gain).

CMFB Amplifier

Now that we know how our CMFB signal, V_{CMFB}, in the op-amp of Fig. 26.26 affects the output voltages and that the gain this signal sees is approximately 25 ($v_{op,n}/V_{CMFB}$), we need to discuss the CMFB amplifier. Consider the two diff-amps seen in Fig. 26.28. In the top diff-amp, gate-drain-connected loads are used. As seen in the simulations, the gain from the averaged input, V_{CMA}, to the diff-amp's output, V_{CMFB} is considerably less than 1 (and so the CMFB is guaranteed to be stable). Unfortunately, the CMFB amplifier's output voltage isn't high enough. (As seen in Fig. 26.27, we need approximately 400 mV.) The diff-amp's tail current can be increased in size (use at least two PMOS for the tail current) to increase the output voltage. However, the low gain, say around 0.3, combined with the CMFB gain through the op-amp, again around 25, means that the CMFB loop's overall gain is only around 7. This isn't large enough to precisely balance the outputs. Using the diff-amp with current mirror load, Fig. 26.28b, gives a gain of approximately 8. This combined with the op-amp's CMFB gain gives an overall CMFB loop gain of 200. This is less than the op-amp's differential gain (so we can use the same compensation capacitors to stabilize the CMFB loop), Fig. 26.23, and large enough to precisely balance the op-amp's outputs.

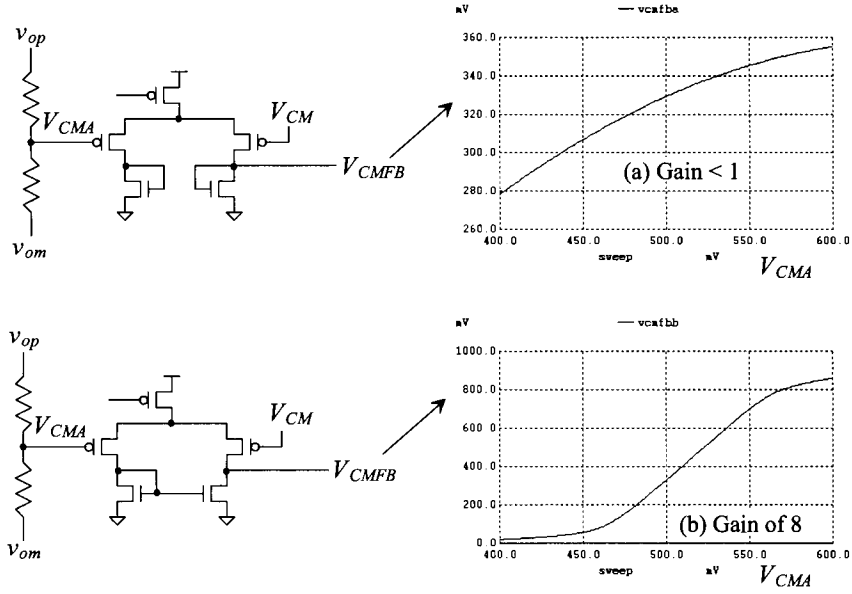


Figure 26.28 Gains of CMFB amplifiers.

The Two-Stage Op-Amp with CMFB

Figure 26.29 shows the complete schematic of the op-amp. Notice that we've doubled the width of the MOSFETs in the output buffer. The added loading from the CMFB averaging resistors will lower the open-loop gain. To compensate for this reduction, the

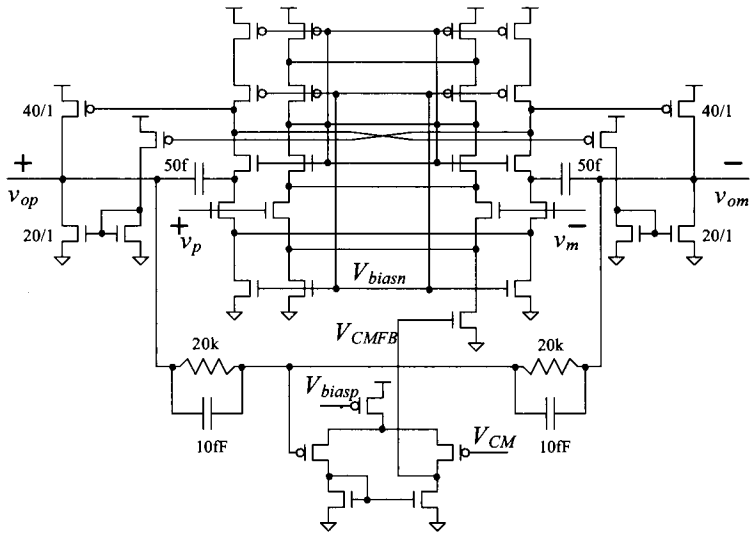


Figure 26.29 Complete schematic of op-amp with CMFB.

drive strength of the MOSFETs on the output of the op-amp was increased. Figure 26.30 shows the DC behavior of the op-amp when placed in the configuration seen in Fig. 26.23. Notice that the outputs cross at the ideal common-mode voltage of 500 mV. The gain is reduced because of the loading by the 20k resistors in the CMFB circuit (and so the gain can be increased by increasing the values of the resistors in the CMFB circuit). However, **we see a problem** with these simulation results. The outputs are only swinging from 200 to 800 mV (not from 0 to *VDD* as possible with a push-pull output stage). Further, we can estimate the current pulled from *VDD* for the op-amp in Fig. 26.29 by counting the number of branches in the op-amp (noting that the output stage counts twice because we've doubled the widths of these devices). Including the CMFB amplifier, there are 11 branches. If the bias current through each branch is 20 μA and the current pulled by the bias circuit is 50 μA, then we would expect the op-amp to pull 270 μA (perhaps even a little less because many of the MOSFETs are biased near the triode region). When we look at the simulation results that generated Fig. 26.30, we see that the current is closer to 500 μA (way off indicating, again, that we've got a problem).

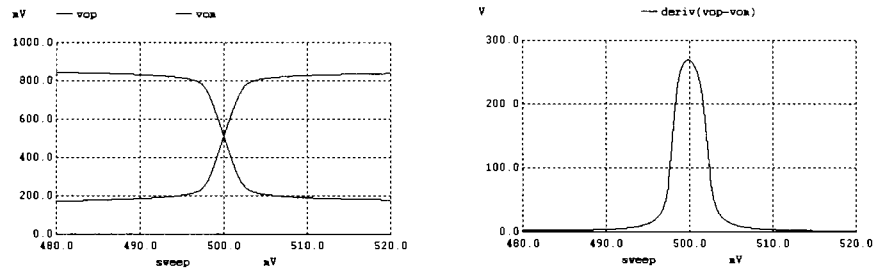


Figure 26.30 Simulating the operation of the op-amp in Fig. 26.29.

Origin of the Problem

The origin of the problem (that is, the op-amp drawing too much current and the output swing not reaching the rails) can be traced to the output buffer. We spent a considerable amount of time discussing how we want to set the outputs of the diff-amp to V_{biasp}. When we look at the simulations, we see the diff-amp's outputs are considerably less than the ideal 600 mV of V_{biasp}. To understand why, let's look at the output buffer in Fig. 26.31. Since the problems appear with the addition of the CMFB circuit, we assume that the two gates of the PMOS devices are moving at the same potential (tied together), that is, that the inputs to the buffer are moving with the diff-amp's output common-mode level. When the output of the diff-amp is V_{biasp} (600 mV), 20 μA flows in all of the MOSFETs. (To keep things simpler, we don't include the doubling in the widths used in the op-amp output devices.) The gate potentials of the NMOS are, roughly, V_{biasn} (400 mV). Because of the symmetry of the circuit, this means that the output is also at 400 mV. To increase the output voltage to 500 mV, we must drop the potential on the gates of the PMOS until the gate-drain-connected NMOS has a V_{GS} of 500 mV (again because of the symmetry). This increases the current (significantly) flowing in the output buffer, lowers its gain, and reduces the linear output swing. The overdrive voltages essentially change from the desired 100 mV when 20 μA of current flows to 200 mV when the output is driven to 500 mV.

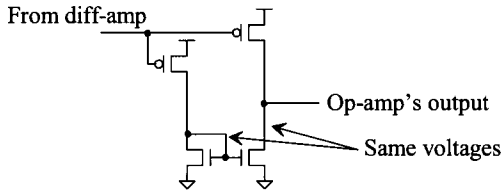


Figure 26.31 Output buffer used in the op-amp of Fig. 26.29.

Figure 26.32 shows one solution to this problem. We've added a device to cascode the output buffer's NMOS (the one connected to the output terminal). The speed shouldn't be affected by the addition of the device (which operates near or in the triode region). The added device allows the op-amp's output to swing more freely (but the current still won't be precisely set). The added device won't affect the output swing range of the op-amp. Figure 26.33 shows the op-amp with modified output buffer.

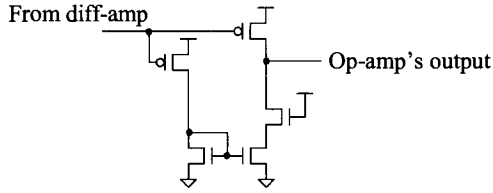


Figure 26.32 Adding a device to allow the output voltage to swing.

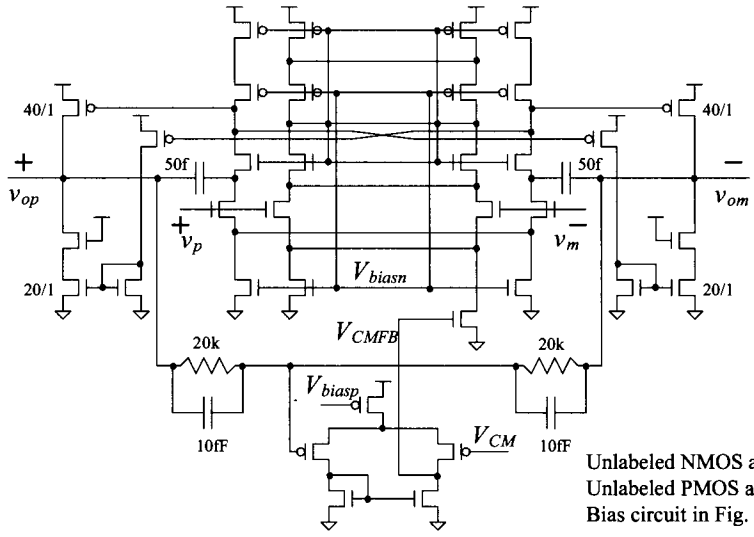


Figure 26.33 Op-amp with modified output buffer.

Simulation Results

Figures 26.34 to 26.36 show simulation results based on the circuit topologies in Figs. 26.23 to 26.25, respectively, using the op-amp in Fig. 26.33. In Fig. 26.34 we see that the outputs now swing close to the power supply rails (unlike what we saw in Fig. 26.30). Also, the gain is higher. Figure 26.35 shows the step response of the amplifier in the topology seen in Fig. 26.24. Finally, Fig. 26.36 shows the outputs of the sample-and-hold in Fig. 26.25 using the op-amp in Fig. 26.33.

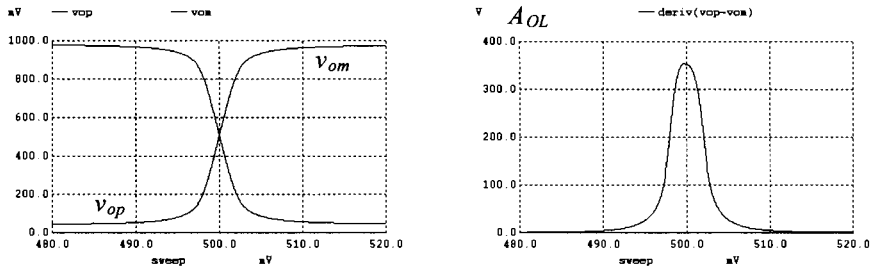


Figure 26.34 Resimulating the op-amp in Fig. 26.33 in the configuration seen in Fig. 26.23.

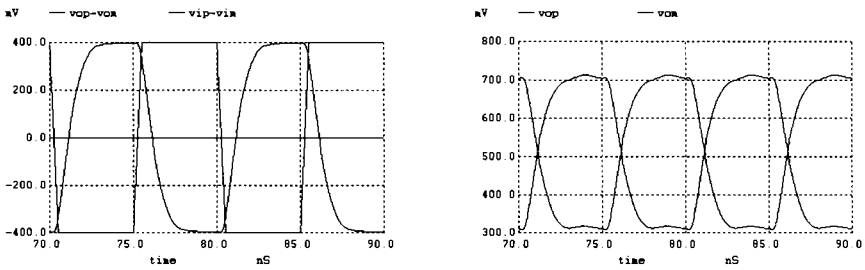


Figure 26.35 Regenerating the simulation results using the topology in Fig. 26.24 with the op-amp in Fig. 26.33.

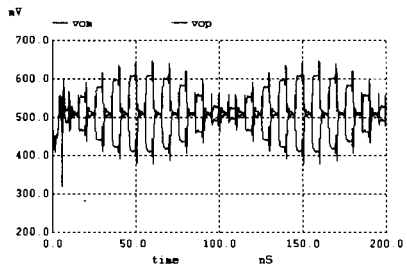


Figure 26.36 Using the op-amp in Fig. 26.33 in the sample-and-hold circuit of Fig. 26.25. Figure shows the outputs of the op-amp.

Using MOSFETs Operating in the Triode Region

For the output buffer in Fig. 26.32, we added a transistor in the drain portion of the circuit. We might wonder if we can accomplish better control of the current flowing in the output buffer by adding circuitry to the source side of the buffer. Towards answering this question, consider the portion of the output buffer seen in Fig. 26.37. If both outputs are at V_{CM}, the gate-source voltages of M2 and M3 are the same and so are the gate-source voltages of M1 and M4. If one output goes high and the other output goes low (and the outputs are centered around V_{CM}), then the net drain current of each M3 is constant. If one output goes below the threshold voltage of an NMOS device, then the balancing stops working. The practical problem of using triode-operating MOSFETs (in a CMFB circuit or any type of amplifying configuration) is that the gain through a MOSFET operating in the triode region is low (so it's difficult to provide control).

A portion of the output buffer.

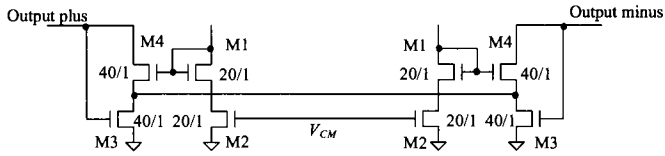


Figure 26.37 Using triode-operating MOSFETs to balance the outputs (bad).

Start-up Problems

Examine the circuit in Fig. 26.38 using the op-amp in Fig. 26.33. Because the op-amp's inputs are at 0 V, the diff-amps on the input of the op-amp are off. This causes the gates of the PMOS devices in the output buffer to be pulled to *VDD*. The circuit remains in this state and doesn't move the outputs or the inputs up to V_{CM}. To avoid this start-up problem, we need to ensure that there is some DC path to *VDD* or V_{CM} to "start-up" the op-amp.

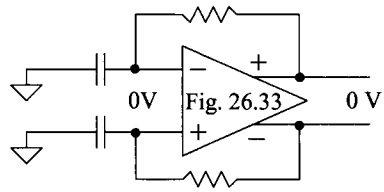


Figure 26.38 The op-amp in Fig. 26.33 won't turn on in this topology.

Lowering Input Capacitance

Consider connecting the gates of the NMOS diff-amp used for biasing to V_{CM} (see the bold line in Fig. 26.39). This reduces the input capacitance of the op-amp and shouldn't affect the normal operation as long as the common-mode voltage of the op-amp (the gates

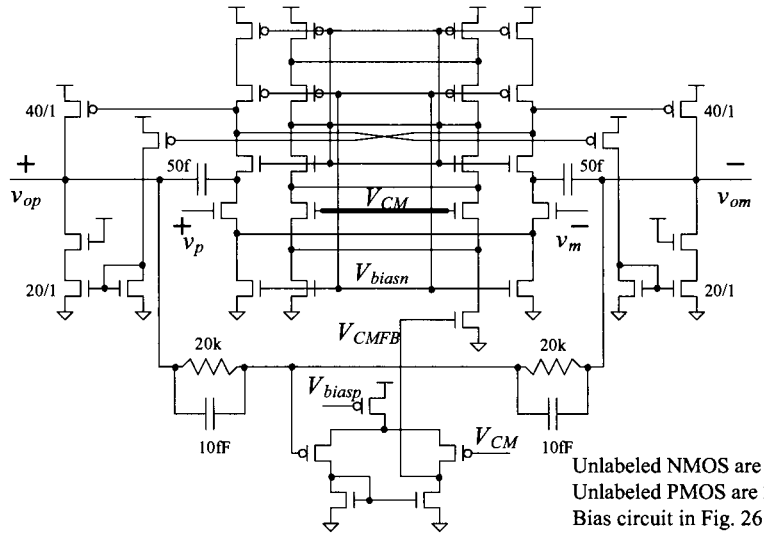


Figure 26.39 Connecting the bias circuit diff-amp's inputs to the common-mode voltage.

of the other diff-amp) is V_{CM}. Simulating the operation of the op-amp in Fig. 26.39 to generate the data in Figs. 26.34 to 26.36 (in the same topologies), we see no change in the simulation data (the netlists used to verify this statement can be found at cmosedu.com).

Looking at Fig. 26.39, we might now wonder why we need two biasing branches down the middle of the op-amp. Further, looking at the voltages in Fig. 26.19, we might wonder if we can make the op-amp more tolerant to changes in *VDD*. The way the op-amp is biased now the open-loop gain drops significantly if *VDD* drops to 900 mV.

Making the Op-Amp More Practical

As just mentioned, having two identical branches down the middle of our op-amp wastes power (although it is useful for a symmetrical layout). We can cut one of the branches out of the design and reduce the power dissipated by the op-amp. We might further wonder if using V_{biasn} for biasing the cascode PMOS current sources is such a good idea. Reviewing Fig. 26.4, we see that V_{biasn} essentially stays at 400 mV after the reference turns on (*VDD* gets above a certain value). In a practical op-amp, we want this voltage to decrease as *VDD* drops in an effort to keep the PMOS devices operating in the saturation region.

Examine the op-amp in Fig. 26.40. We've added a wide-swing bias circuit, see Fig. 20.38, and cut out one of the biasing branches used in the op-amp seen in Fig. 26.39. The power dissipation remains essentially the same as in the previous op-amp topologies. Note how we apply the CMFB to one side of the bias circuit (not to the 10/3 wide-swing bias branch). Further notice how we've reduced the gain of the CMFB loop by using two 10/2 MOSFETs. It may be a good idea to reduce the strength of the CMFB loop even further by increasing the lengths of the NMOS devices. For example, we might change these devices from 10/2 to 10/4. The ability to drive V_{CMFB} considerably above V_{biasn} eliminates the concern that the NMOS device can sink the current needed to bias the circuit at the correct point (and why the CMFB loop can so easily become unstable).

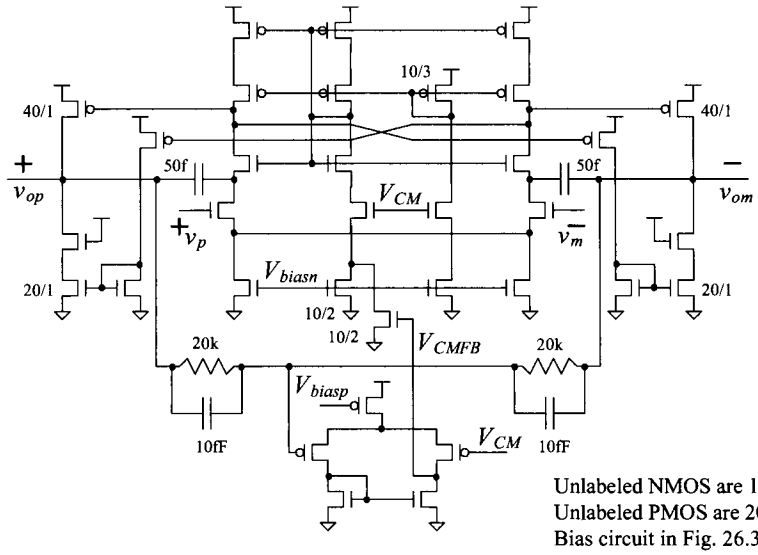


Figure 26.40 Making the op-amp more practical.

A more practical problem is the change in the MOSFET's drain currents with drain-source voltages. For example, looking at Figs. 26.18a and b, we see that it's possible for the NMOS's drain current to be twice the PMOS's drain current for the same gate-source voltages. This can cause op-amp failure in the CMFB circuit. If, for example, the current flowing in the 10/2 MOSFET connected to V_{biasn} is larger than the current sourced by the PMOS, the voltage V_{CMFB} goes to zero and the CMFB loop doesn't work properly. A good "rule-of-thumb" is for the fixed current flowing in the CMFB-controlled bias circuit to be 25–50% of the total expected current.

Increasing the Op-Amp's Open-Loop Gain

The op-amp that we've developed in this section has an open-loop gain in the hundreds. As we'll see in Ch. 29 (Eq. [29.59]), the open-loop gain of the op-amps used in a data converter has a direct effect on the maximum attainable resolution. Towards increasing the gain of the op-amp, let's use the gain-enhancement (GE) techniques presented in Sec. 24.4.

Figure 26.41 shows how we should *not* implement GE. An amplifier with fully-differential outputs, like the amplifier in Fig. 26.7, regulates the drains of the top PMOS devices. We know that this is bad because we would need a CMFB circuit to balance the outputs of the added amplifier.

Figure 26.42 shows how we can add GE to the op-amp developed in this section. Notice that GE is implemented with amplifiers having single-ended outputs. When designing the added amplifiers, as discussed in Sec. 24.4, the bandwidth isn't important for high-speed operation. The lengths of the MOSFET in the added amplifiers can be increased to reduce power and boost gain. An important concern is the added amplifier's input common-mode range.

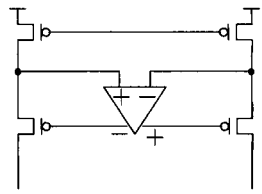


Figure 26.41 How not to implement GE in an op-amp (unless the added amplifier employs CMFB).

The practical problem with the topology seen in Fig. 26.42 is the implementation of the CMFB. With the GE added to the op-amp we now have four additional feedback loops. Variations in V_{CMFB} affect all GE loops in addition to the CMFB through the op-amp. Making these loops stable becomes extremely challenging. What we need is to implement the CMFB without including the diff-amp and GE amplifiers. We can only do this by controlling the output buffer common-mode level, Fig. 26.43. This circuit includes the output buffer we used in Fig. 26.37. Now, however, we add an amplifier in series with the triode-operating MOSFETs to boost the CMFB gain (so that the outputs can be balanced around V_{CM}). The problem with this approach is that the CMFB isn't compensated using the same capacitors as the differential forward signal path (i.e., no Miller effect). We must be concerned with CMFB stability.

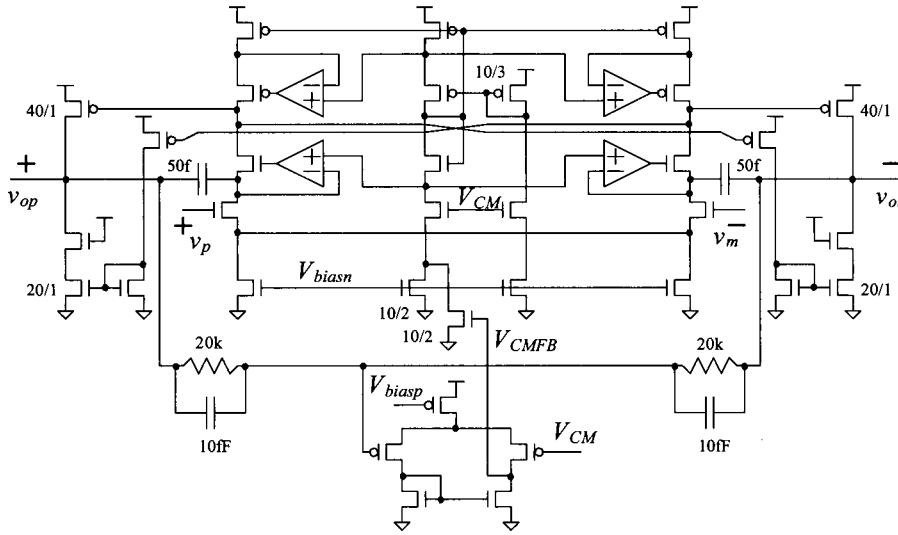


Figure 26.42 Adding gain-enhancement to the op-amp.

Let's discuss the op-amp design in Fig. 26.43. We begin by showing the DC behavior of the op-amp (to show that the outputs are indeed balanced). Figures 26.44a and (b) show the DC behavior and gain of the op-amp in Fig. 26.43 in the topology seen in Fig. 26.24. Again note that by increasing the values of the 20k resistors used to average

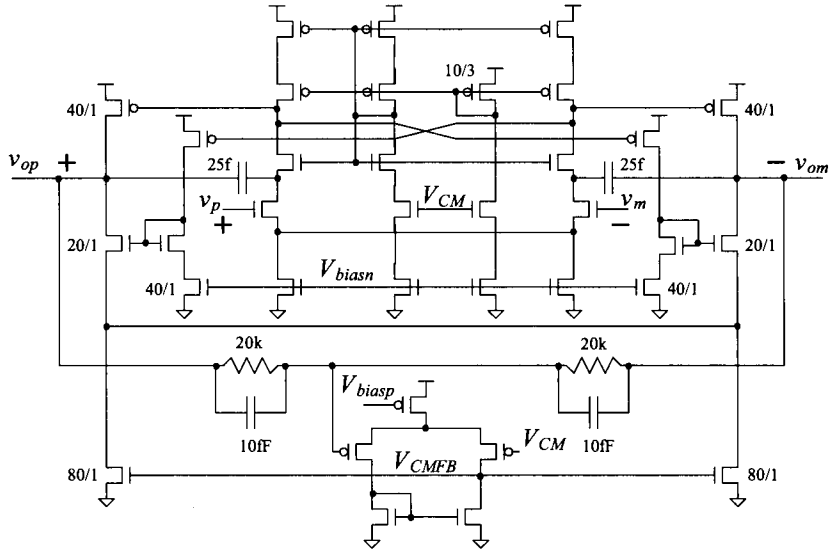
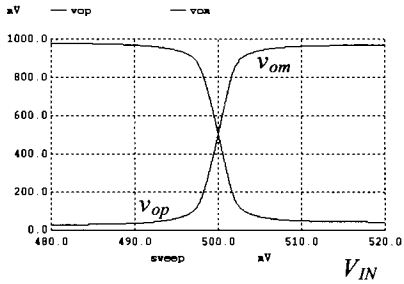
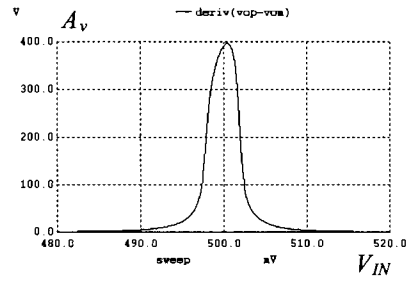


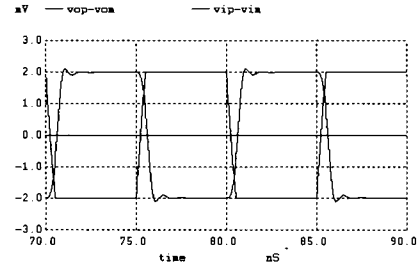
Figure 26.43 Providing CMFB through just the output buffer. Using an amplifier with triode-operating MOSFETs for CMFB (good).



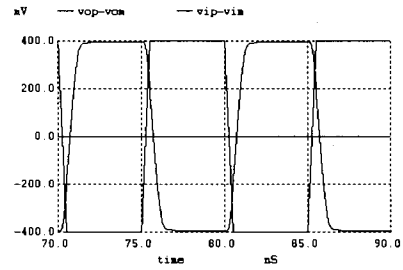
(a) DC behavior



(b) Op-amp gain



(c) Small-signal step response



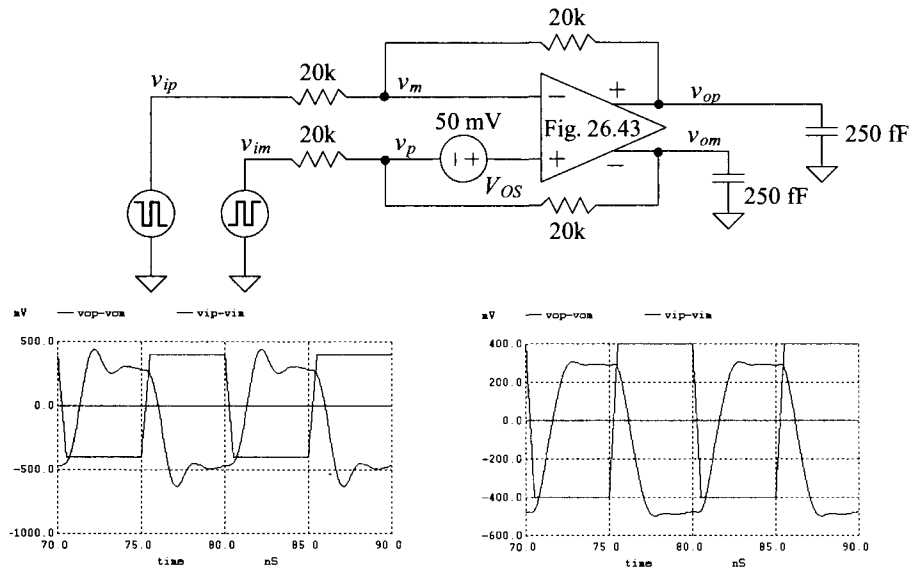
(d) Large-signal step response

Figure 26.44 Behavior of the op-amp in Fig. 26.43 (see text).

the outputs we can increase the DC gain of the op-amp. Because the forward differential path compensation (now) doesn't include the CMFB path, we've reduced the compensation capacitors from 50 fF to 25 fF (there are practical issues with this change that we'll discuss next). Note that the widths of the added triode-operating MOSFETs are increased to ensure that they operate well within the triode region and don't significantly affect the output drive capability of the op-amp. Figures 26.44c and (d) show the small- and large-signal step responses (see Fig. 26.24). The settling times are approximately 1–2 ns. The current drawn from *VDD* (including the the bias circuit current) is approximately 250 μA (200 μA for the op-amp alone).

Offsets

We said in Sec. 26.2 that we want to add offsets of 50 mV in series with the gates of our MOSFETs to see if the op-amp "breaks." Consider the addition of an input-referred offset voltage in the schematic seen in Fig. 26.45. This offset is used to model the overall offset voltage of the op-amp (see Fig. 24.4). If we look at the effects of the offset on the circuitry in Fig. 26.43, we see that one of the NMOS devices in the diff-pair will have a higher overdrive voltage (larger g_m) than the other NMOS device. Since the unity-gain frequency of an op-amp is given by $g_m/2\pi C_c$, the effect is a shift in the unity-gain frequency (and potential instability). As seen in Fig. 26.45, using the 25 fF compensation capacitors destabilizes the op-amp (as indicated by the ringing). Increasing the compensation capacitor's value (back) to 50 fF makes the step response cleaner. We could argue that 50 mV is an unrealistically high offset voltage, so it's better to leave the capacitors at 25 fF (and this may be the case). However, in a practical CMOS process, the op-amp's characteristics shift with the process shifts (and temperature). It's better to overcompensate than to have an unstable op-amp.



25 fF compensation capacitors

50 fF compensation capacitors

Figure 26.45 How an offset can affect the step response (compensation).

Op-Amp Offset Effects on Outputs

Notice, in Fig. 26.45, that an offset shifts the differential output signal by twice the offset voltage. The individual op-amp output voltages remain centered around V_{CM}. To describe this in more detail, consider the test setup seen in Fig. 26.46. We know the CMFB forces

$$\frac{v_{op}+v_{om}}{2}=V_{CM} \text{ or } v_{op}=2V_{CM}-v_{om} \tag{26.8}$$

Further, assuming large op-amp open-loop gain,

$$v_p+V_{OS}=v_{pos}\approx v_m \tag{26.9}$$

Equating currents, we can write

$$\frac{V_{CMI}-v_p}{R_{in}}=\frac{v_p-v_{om}}{R_f} \text{ or } \frac{V_{CMI}-v_m+V_{OS}}{R_{in}}=\frac{v_m-V_{OS}-v_{om}}{R_f} \tag{26.10}$$

and

$$\frac{V_{CMI}-v_m}{R_{in}}=\frac{v_m-v_{op}}{R_f} \tag{26.11}$$

Subtracting Eq. (26.11) from Eq. (26.10), we get

$$\frac{V_{OS}}{R_{in}}=\frac{-V_{OS}+v_{op}-v_{om}}{R_f} \tag{26.12}$$

or

$$v_{op}-v_{om}=V_{OS}\cdot\left(\frac{R_f}{R_{in}}+1\right) \tag{26.13}$$

The voltages on the outputs of the op-amp are then

$$v_{op}=\frac{V_{OS}}{2}\cdot\left(1+\frac{R_f}{R_{in}}\right)+V_{CM} \text{ and } v_{om}=V_{CM}-\frac{V_{OS}}{2}\cdot\left(1+\frac{R_f}{R_{in}}\right) \tag{26.14}$$

The op-amp's input voltages are

$$v_m\approx v_p+V_{OS}=\frac{V_{OS}}{2}+V_{CM}\cdot\left(\frac{R_{in}}{R_{in}+R_f}\right)+V_{CMI}\cdot\left(\frac{R_f}{R_{in}+R_f}\right) \tag{26.15}$$

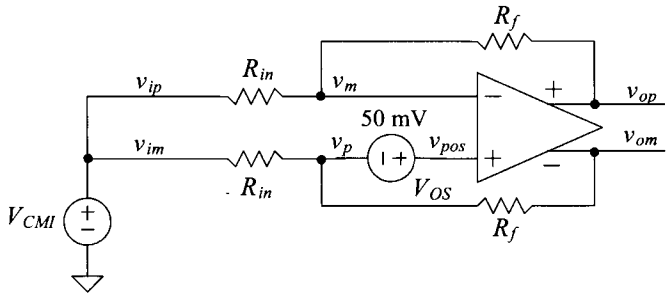


Figure 26.46 How an offset voltage causes an imbalance in the outputs.

If the input signal's common-mode voltage, V_{CMI}, is the same as the op-amp's common-voltage, V_{CM}, and V_{OS} is zero, then both op-amp inputs are held at V_{CM}. If $V_{CM} = V_{CMI}$ but the offset isn't zero, then $v_m = V_{OS}/2 + V_{CM}$ and $v_p = V_{CM} - V_{OS}/2$. Neglecting the offset voltage, if the input signal's common mode voltage isn't V_{CM}, then the op-amp's input common-mode voltage ($v_p = v_m$) will be different from the ideal value of V_{CM}. This can shut the op-amp off and cause undesirable behavior.

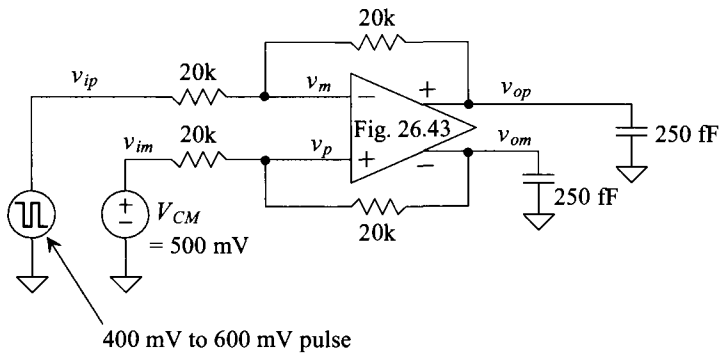


Figure 26.47 Problems with single-ended input signals.

Single-Ended to Differential Conversion

Even if the input signals are referenced around V_{CM} and the op-amp is offset free, we can still have problems. Consider the circuit in Fig. 26.47. In this circuit the input signal is single-ended. The other input to the op-amp is tied to V_{CM}. Even though the input is balanced around 500 mV, it is not a truly differential signal. When the input signal is up at 600 mV, the effective input common-mode voltage, V_{CMI}, is 550 mV (the average of the two inputs). When the input signal is at 400 mV, V_{CMI} is 450 mV. Figure 26.48 shows the simulation results using the circuit in Fig. 26.47. These results are very interesting. Consider what's happening between 70 and 75 ns. During this time, v_{ip} is 600 mV and v_{im} is 500 mV (and so $v_{ip} - v_{im} = 100\ mV$). The op-amp's inputs move above the ideal 500 mV, as seen in the figure. This has the effect of increasing the transconductance of the diff-amp (the diff-amp's tail current is operating near/in the triode region so the tail

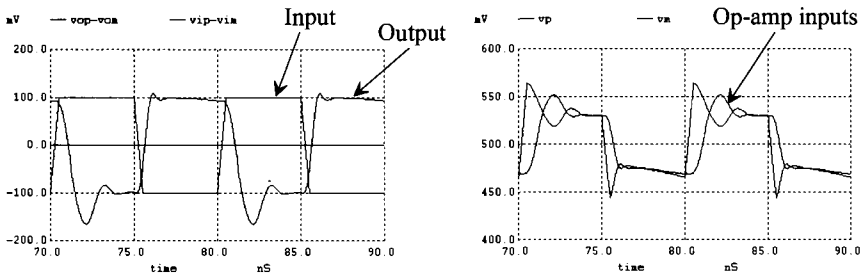


Figure 26.48 Simulating the operation of the circuit in Fig. 26.47.

current increases as the input common-mode voltage goes up). The increase in the diff-amp's g_m causes the unity gain frequency to increase and, with a fixed compensation capacitor, the phase margin to decrease (causing overshoot and ringing in the circuit's step response). Next consider what happens between 75 and 80 ns. The input signal switches to $400\,mV - 500\,mV = -100\,mV$ and the op-amp's inputs drop down to around 475 mV. This causes the diff-amp's g_m to decrease and the op-amp to slow down (become more stable). However, at such a low input common-mode voltage the gain of the op-amp will drop and the outputs may wander. (See Sec. 30.3.1 for design information).

CMFB Settling Time

If we look at the voltage, V_{CMFB}, in the op-amps in Fig. 26.40 or 26.43, we may see that they aren't settling as quickly as the differential mode signals. Is this bad? As seen in Eq. (26.13), variations in V_{CMI} don't (ideally) affect the differential output signal. However, if the variations in V_{CMFB} and thus V_{CMI} are large, one of the output signals can saturate at close to *VDD* or ground (the op-amp's gain drops), affecting the differential signal path.

CMFB in the Output Buffer (Fig. 26.43) or the Diff-Amp (Fig. 26.40)?

In this section we've presented the design of op-amps using continuous-time CMFB. Various design trade-offs and topologies were presented. At this point a good question is: "Which CMFB scheme is better?" Controlling the output common-mode level through the output buffer (Fig. 26.43) is simple, easy to ensure stability, and fairly robust. However, consider what happens if the op-amp in Fig. 26.43 is used in the topology in Fig. 26.46 (without an offset). If V_{CMI} is ground, then, according to Eq. (26.15), the input voltages to the op-amp will move to 250 mV while the outputs of the op-amp remain at 500 mV. Thinking about this for a moment and neglecting the fact that an op-amp input common-mode voltage of 250 mV will shut the op-amp off, we see that the outputs of the op-amp must source a current back through the feedback resistors to the inputs. Further, anytime $V_{CMI} < V_{CM}$, the PMOS in the output buffer must source a DC current back to the inputs. Similarly, if $V_{CMI} > V_{CM}$, the NMOS in the output buffer must sink a current from the inputs of the op-amp. When using CMFB in the output buffers, we have no way of increasing the quiescent or DC current flowing in the output buffer to source/sink current from the input source (or to a DC load connected to ground). The output voltage of the diff-amp in the op-amp of Fig. 26.43 biases, or sets, the quiescent current in the output buffer. The CMFB scheme used in the output buffer simply adjusts the drive strength of the NMOS (in the output buffer) to set the op-amp's output common-mode level.

Using the CMFB scheme in Fig. 26.40, we can adjust the output voltage of the diff-amp (and ultimately the op-amp's output voltage) and thus the bias current in the output buffer (both the NMOS and the PMOS connected to the output buffer). However, if the output buffer must source/sink a significant amount of current, we can have problems with this topology too. For example, if the diff-amp's output voltage increases (turning off the PMOS in the output buffer and attempting to pull the op-amp's outputs down) while the NMOS devices connected to the outputs are sinking significant current, then it's possible that the outputs will get pulled upwards and the CMFB will fail (likely causing the gain of the op-amp to drop and the outputs to have limited swing).

To ensure the most robust op-amp design (biasing tolerant to offsets and easy to compensate the CMFB loops), CMFB circuits can be placed around both op-amp stages. This method is used in our last op-amp design example discussed next.

26.4 Op-Amp Design Using Switched-Capacitor CMFB

In this section we turn our attention towards op-amp designs for switched-capacitor (SC) circuits. We'll develop an op-amp design based on the topologies discussed in the last section. In this section, however, we'll use SC CMFB instead of continuous-time CMFB. Again, we'll use the nanometer CMOS process with minimum lengths and (roughly) 100 mV overdrive voltages (for drain currents of 20 μA, see Fig. 26.18). We'll stick with two-stage designs because of the low open-circuit gains present when doing high-speed design.

Clock Signals

The SPICE listing for the clock signals used in the simulations in this section is seen below. Note that the 100 MHz phi1 and phi2 clocks are used with the NMOS transistors (phi1 and phi2 are not high at the same times), while the complements of these clock signals are used with the PMOS switches (not low at the same times).

```
*Clock Signals
Vphi1   phi1    0 DC 0  Pulse   0 1 0  200p  200p 4n 10n
Vphi1b  phi1b   0 DC 0  Pulse   1 0 0  200p  200p 4n 10n
Vphi2   phi2    0 DC 0  Pulse   0 1 5n 200p 200p 4n 10n
Vphi2b  phi2b   0 DC 0  Pulse   1 0 5n 200p 200p 4n 10n
R1      phi1    0       1MEG
R2      phi1b   0       1MEG
R3      phi2    0       1MEG
R4      phi2b   0       1MEG
```

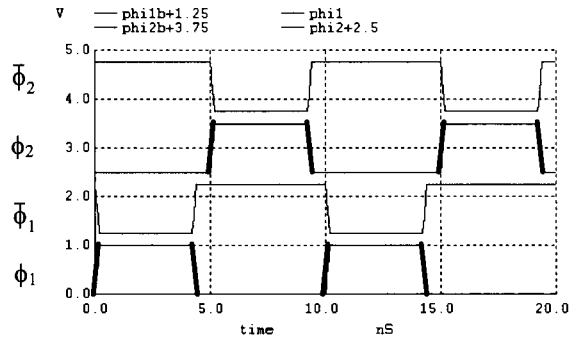


Figure 26.49 Generating nonoverlapping clocks for SC circuits.

Switched-Capacitor CMFB

Figure 26.50 shows the SC CMFB circuit from Fig. 26.16 along with a symbolic representation. We've selected 10 fF capacitors for the high-speed averaging capacitors. The kT/C noise associated with these capacitors is a common-mode signal and so it shouldn't affect the differential-mode signal. We don't want these capacitors to be too large because they will load the output of the amplifier. We made the switched-capacitors associated with the differencing and averaging 50 fF so that the changes in V_{CMFB} during one clock cycle won't be too large due to differences between the ideal V_{CMFB} and the actual V_{CMFB}. When the average of the outputs, v_{op} and v_{om}, is above their ideal value, the

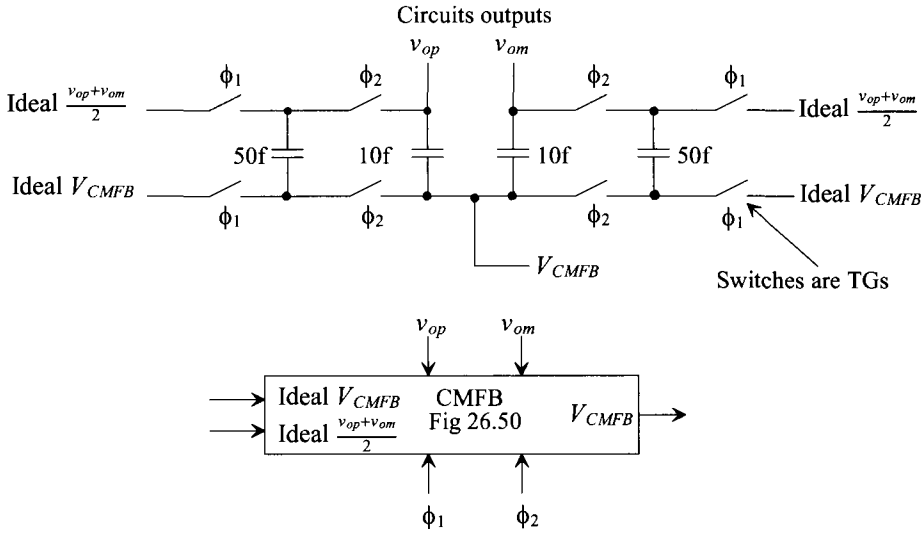


Figure 26.50 A switched-capacitor CMFB circuit (see Fig. 26.16). Switches implemented with transmission gates.

CMFB circuit's outputs moves upwards. It's important that this causes the average value of the outputs to move downwards. In other words, we've got to ensure that negative feedback is used in the CMFB loop.

Figure 26.51 shows some simulation results using the SC CMFB in Fig. 26.50. The ideal V_{CMFB} is 400 mV. The ideal average output, $\frac{v_{op}+v_{om}}{2}$, is 500 mV (V_{CM}). Prior to 150 ns, both v_{op} and v_{om} are 500 mV. At 150 ns, these two voltages jump (in the simulation) to 700 mV (they jump 200 mV away from the ideal average output of 500 mV). The voltage, V_{CMFB}, also jumps at this time. The key point to notice is that V_{CMFB} moves in the same direction as do changes in the output common-mode voltage. Knowing this is important when we are ensuring that our CMFB loop employs negative feedback.

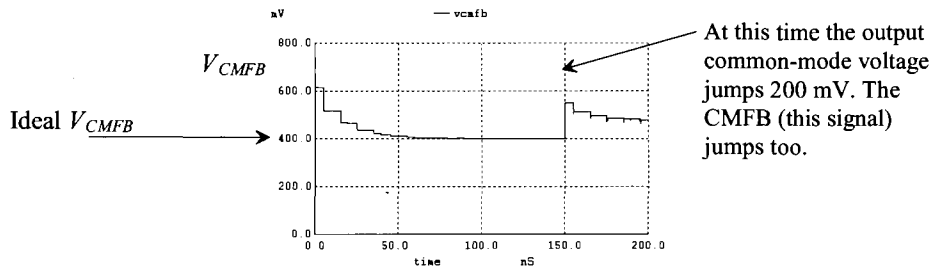


Figure 26.51 How the common-mode feedback signal increases to pull the outputs down.

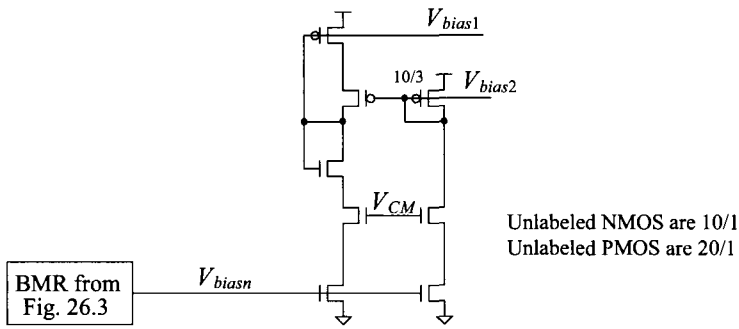


Figure 26.52 Biasing circuit for the op-amp developed in this section.

The Op-Amp's First Stage

As just mentioned, the output of the SC CMFB circuit, V_{CMFB} , moves in the same direction as movement in the average of the amplifier's outputs, v_{op} and v_{om} (the output common-mode level). Keeping this in mind, consider the bias circuit and diff-amp schematics seen in Figs. 26.52 and 26.53. We've separated the bias circuit out from the diff-amp, see Fig. 26.43, for a couple of reasons. To begin, an increase in the CMFB signal in Fig. 26.43 caused the outputs of the diff-amp to increase. As just mentioned, we want the diff-amp's outputs to move in the opposite direction of V_{CMFB}. Moving the CMFB-controlled MOSFET into the tail current of the diff-amp provides this control. Next, our bias circuit may now be shared with several op-amps. The benefit of sharing the bias circuit is a reduction in power dissipation.

Before adding the CMFB circuit, let's look at a SC circuit using an op-amp. Reviewing the sample and hold in Fig. 26.25, we see that when the ϕ_1 switches are closed, the op-amp's inputs and outputs are at (ideally) V_{CM}. The op-amp, during this time, is in

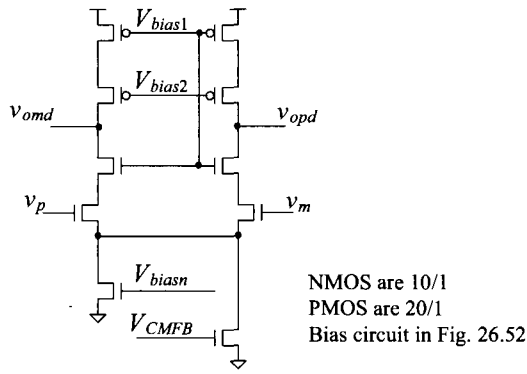


Figure 26.53 Diff-amp used with the bias circuit of Fig. 26.52.

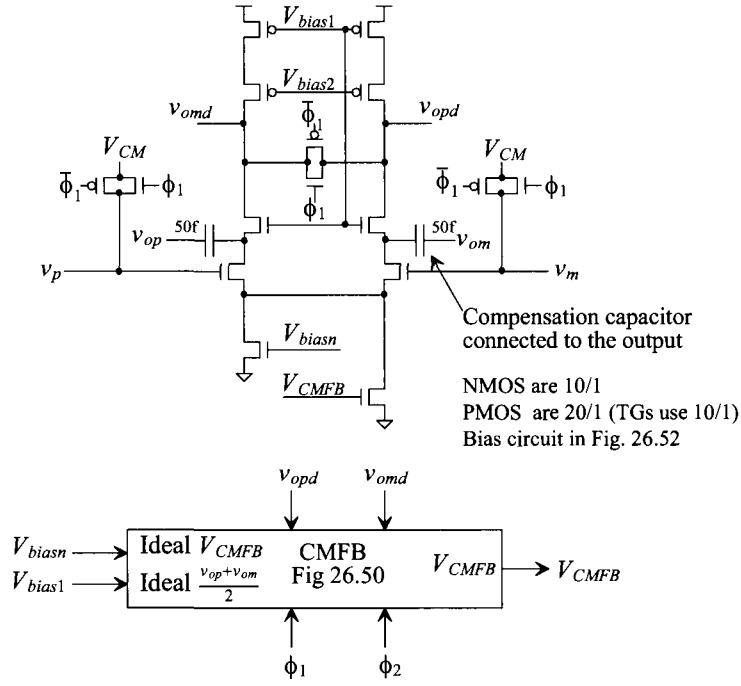


Figure 26.54 First-stage diff-amp with SC CMFB.

the unity-follower configuration. Instead of placing the op-amp in the follower configuration during this time, let's: 1) short the inputs to op-amp (Fig. 26.54) to V_{CM}, 2) short the outputs of the diff-amp (the inputs to the output buffer) together, 3) use a SC CMFB circuit around the diff-amp to ensure a balance condition (and to set the diff-amp's output voltage to V_{bias1}), 4) short the outputs of the op-amp together (so now both the output buffers inputs are shorted and outputs are shorted), and 5) use a SC CMFB around the output buffer to ensure balanced outputs. In other words, during ϕ_1, the differential inputs are shorted together. At the same time, the outputs of the op-amp are shorted together.

Figure 26.55 shows the simulated output of the diff-amp in Fig. 26.54. The SC CMFB circuit sets the outputs of the diff-amp at V_{bias1} or roughly 600 mV. By shorting the two diff-amp outputs together and connecting the inputs to V_{CM} , we are ensuring that even with horrible mismatch, the outputs of the diff-amp will be equal and can be used to bias the output buffer. If, for example, the diff-pair shows a 50 mV mismatch (V_{OS}) then, when ϕ_1 is high, the drain currents in each side of diff-amp are set differently (making this scheme very tolerant to offsets). When ϕ_1 goes low and the op-amp is placed in a feedback configuration, each of the diff-amp's inputs will move (in opposite directions) by $V_{OS}/2$ (and so this topology doesn't store the op-amp's offset voltage).

Note that an important concern, as discussed in the last section, is the input common-mode voltage of the diff-amp. If, for example, the input common-mode voltage

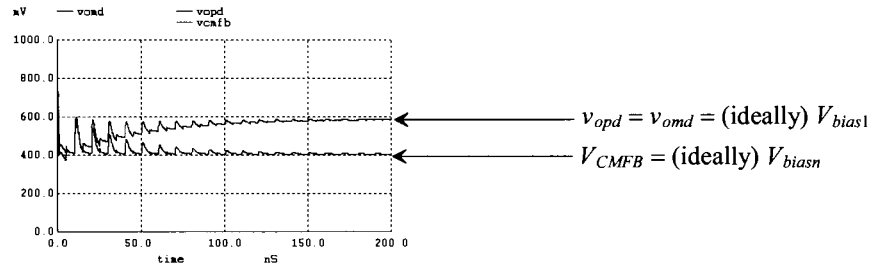


Figure 26.55 Simulating the operation of the circuit in Fig. 26.54.

drops from 500 mV, in Fig. 26.54, to 400 mV the NMOS devices will start shutting off. The op-amp will not settle or behave properly.

The Output Buffer

Figure 26.56 shows a schematic of the output buffer and SC CMFB stage. The nodes v_{omd} and v_{opd} are connected to the diff-amp outputs in Fig. 26.54. When ϕ_1 is high, the outputs of the buffer are shorted together. The SC CMFB is used to set the outputs to the common-mode voltage during this time. Figure 26.57 shows the simulation results for both stages of the op-amp (the op-amp is made with Figs. 26.54 and 26.56) with the inputs and outputs floating. When ϕ_1 is high, the inputs to the op-amp are connected to V_{CM}.

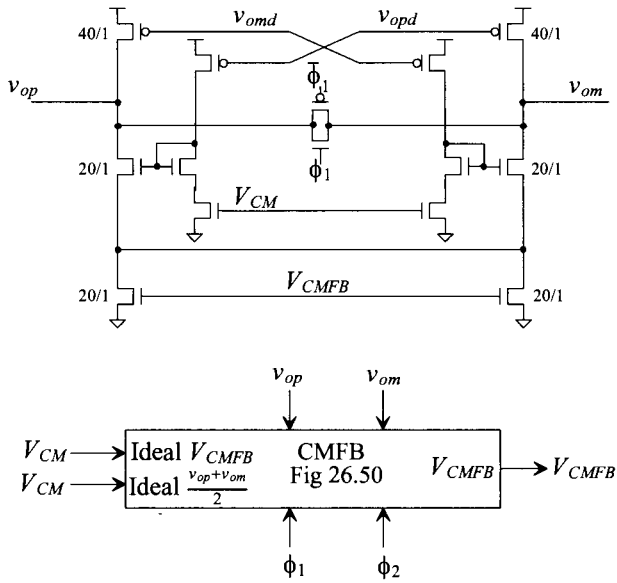


Figure 26.56 Output buffer and CMFB.

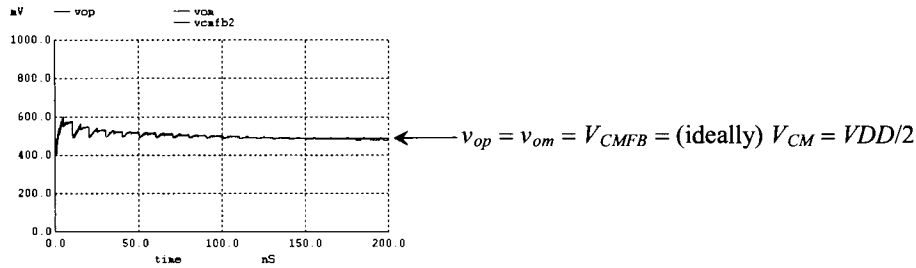


Figure 26.57 Simulating the operation of the op-amp (Figs. 26.54 and 26.56).

Is shorting the outputs of the buffer (or diff-amp) necessary? If the op-amp is operating open-loop (when ϕ_1 goes high), we don't want the outputs to float. By shorting the diff-amp and output buffer output terminals together, we ensure that they are set to a known value. If we were to use this op-amp in a SC integrator, we wouldn't short the inputs of the diff-amp to V_{cm}, the outputs of the diff-amp together, or the output buffer outputs together since there is always feedback around the op-amp. In other words, the same op-amp topology can be used in a SC integrator but without the three TGs seen in Figs. 26.54 and 26.56.

An Application of the Op-Amp

An application of the op-amp we've just developed is seen in Fig. 26.58. This is the sample and hold developed earlier (Figs. 25.15 and 26.25) except that now, during ϕ_1 (high) the inputs to the op-amp are shorted to V_{CM} (Fig. 26.54) and the outputs are shorted together (Fig. 26.56). When ϕ_2 goes high (ϕ_1 is low since the two clocks are nonoverlapping), the op-amp moves into the follower configuration and holds its outputs at the value of the inputs when the ϕ_1 switches shut off.

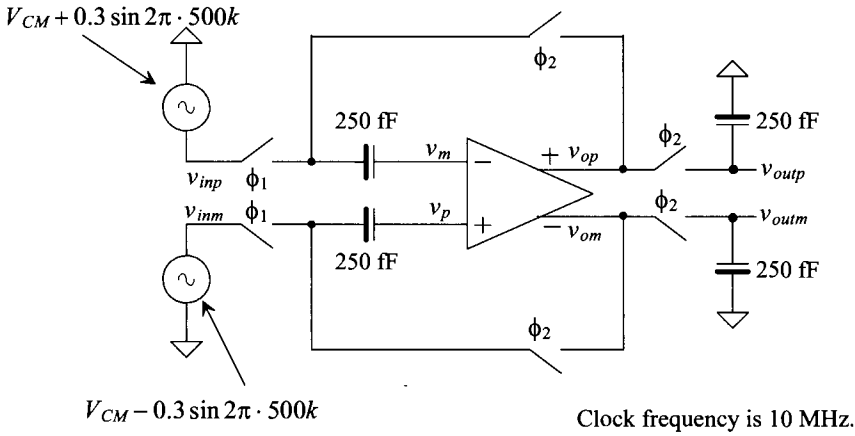
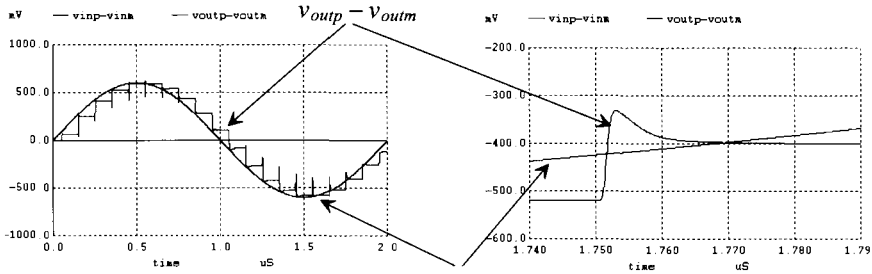
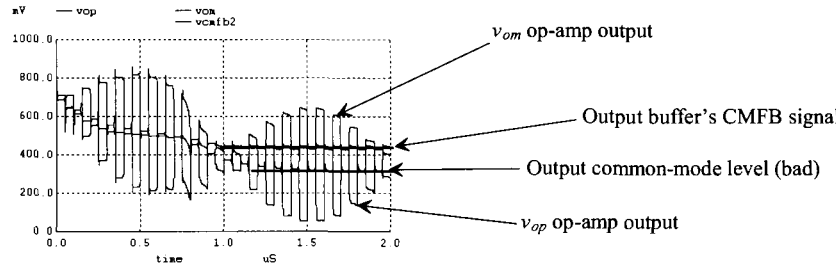


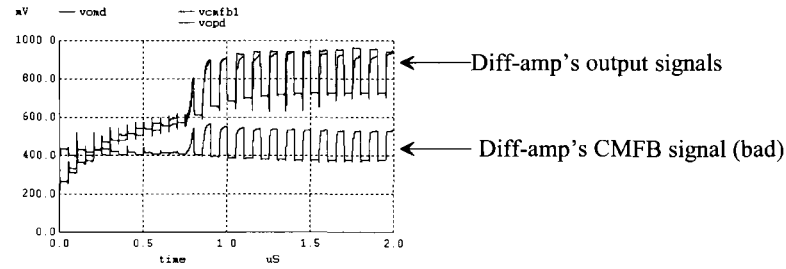
Figure 26.58 Simulating the operation of the op-amp formed with the diff-amp in Fig. 26.54 and buffer in Fig. 26.56.



(a) Circuits inputs and outputs (b) Slow settling time



(c) Op-amp's output and buffer's CMFB signal



(d) Diff-amp's outputs and CMFB signal

Figure 26.59 Simulating the operation of the circuit in Fig. 26.58 with the op-amp made with the diff-amp in Fig. 26.54 and the output buffer in Fig. 26.56.

Simulation Results

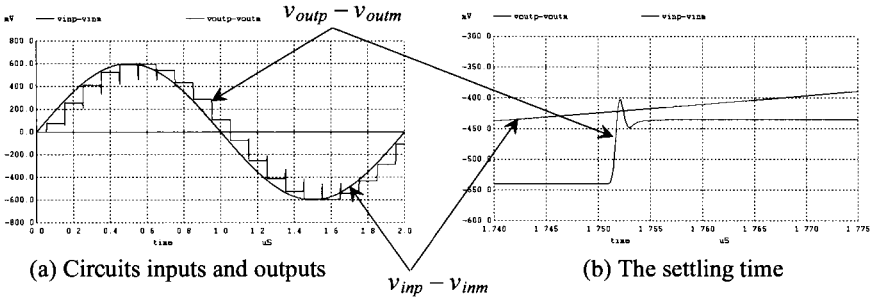
The simulation results are seen in Fig. 26.59. To ensure that we see the full settling behavior of the op-amp and any other issues or concerns, we use a slow clock (10 MHz) for the initial simulations. As we gain confidence that our op-amp is settling correctly and stable, we can increase the clock frequency and the input signal frequency to see how the sample and hold performs. The main thing that's different with this design compared to previous designs is that the op-amp isn't operating with feedback all of the time. When the op-amp does get put into a feedback configuration (ϕ_2 goes high), there will be a start-up time (e.g., the inputs of the op-amp will move away from V_{CM} because of the op-amp's offset).

Returning to the simulation results in Fig. 26.59, we see, in (b), that the settling time is quite long (approximately 10 ns). Letting the simulation run for a longer period of time, we see that the settling time increases and, ultimately, that the op-amp stops functioning correctly. In (c) we see the problem: the outputs of the op-amp aren't balanced around V_{CM}. Further, movement downwards causes the common-mode voltage on the input of the diff-amp to drop. The result is that the input diff-amp starts to shut off. The voltage across the diff-amp's tail current source drops and makes it difficult to control the diff-amp's output common-mode level. As seen in (d), the diff-amp's CMFB signal is increasing in an attempt to increase the current flowing in the diff-amp and pull the diff-amp's output voltages downwards. However, because the common-mode voltage on the input of the diff-amp has decreased, the voltage across the tail currents is small (tens of mV). For example, if the input common-mode voltage drops from 500 mV (V_{CM}) to 450 mV and the V_{GS} of the input diff-amp is 400 mV, then only 50 mV is left to drop across the tail current sources (one biased with V_{biasn} and the other with V_{CMFB}). We've discussed this problem earlier.

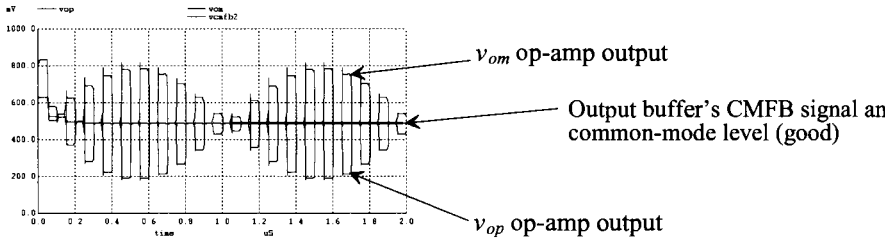
We can do one of two things to make this decrease in input common-mode voltage less of a problem: 1) reduce the diff-amp's bias current or 2) increase the widths of the input diff-pair. In both cases we need to increase the voltage dropped across the tail current sources by decreasing the V_{GS} of the NMOS diff-pair (the inputs to the diff-amp are, ideally, at V_{CM}). If we decrease the bias current, the g_m of the diff-pair decreases and so does the speed of the op-amp (remembering $f_{un} = g_m/2\pi C_c$). By increasing the width of the diff-pair, we increase g_m and thus the unity-gain frequency of the op-amp. The issue with increasing the width of the diff-pair is that the overdrive voltage for these MOSFETs decreases and thus so does their f_T. If we keep the increase in the width to a modest level, the parasitic pole associated with these diff-pair MOSFETs shouldn't, in any significant way, affect the stability of the op-amp.

Figure 26.60 shows the operation of the op-amp made with the diff-amp in Fig. 26.54 and the output buffer in Fig. 26.56 if we increase the widths of the diff-pair from 10 to 40. We also changed the MOSFETs in the biasing circuit Fig. 26.52 with gates connected to V_{CM} to have widths of 40 to maintain symmetry (important for reducing the offset voltage). To further increase the speed we also reduced C_c by 4 (from 50 to 12.5 fF) and increased the widths of the devices in the output buffer by 4 (to move f_2 up and away from f_{un}). The settling time, as seen in (b), is < 3 ns. Note that increasing the g_m of the output buffer by using wider devices (more current) increases f_2 allowing a corresponding increase in f_{un}. This is an **important** technique for increasing the speed of an op-amp.

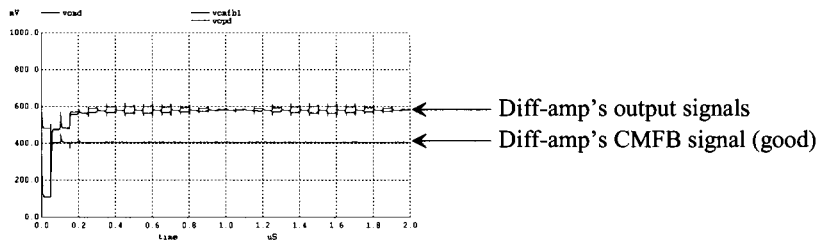
Reviewing the op-amp designs in the last section, we see that their performance may also be improved by a modest increase in the widths of the diff-pair and output buffer. However, as just mentioned, we have to be careful to maintain symmetry. For example, if we take the op-amp in Fig. 26.43, increase the widths of the first stage diff-pair from 10 to 40, and simulate, we see that the outputs don't swing all the way up (or down) to the correct values. Further investigation reveals that the diff-pair moved into the triode region. To move the MOSFETs back into the saturation region, we must also increase the widths of the MOSFETs in the bias circuit (with gates at V_{CM}) from 10 to 40. This adjusts the bias voltages for the NMOS/PMOS diff-amp loads. By providing the CMFB back through the diff-amp (instead of through the output buffer), we can adjust the diff-amp's output voltage. Thus the op-amp is more tolerant to issues in the bias circuit.



(a) Circuits inputs and outputs (b) The settling time



(c) Op-amp's output and buffer's CMFB signal



(d) Diff-amp's outputs and CMFB signal

Figure 26.60 Regenerating the data in Fig. 26.59 after increasing the widths of the input diff-pair and output buffer by 4 while reducing the compensation capacitors by 4 (from 50 to 12.5 fF).

A Final Note Concerning Biasing

In (most) of the designs presented in this chapter, we biased the gates of the NMOS cascode devices in the diff-amp's load at the same (ideally) voltage as the diff-amp's output. For example, in Fig. 26.53, the gate of the NMOS device is tied to V_{bias1}, while its drain (the output of the diff-amp) is also (ideally) at V_{bias1}. This selection is fine for learning design. It minimizes power by avoiding an extra bias reference circuit. However, if *VDD* starts to drop the drain-source voltages across the diff-pair and tail current sources can drop to the point where the op-amp shuts off. Again, increasing the widths of the diff-pair helps with this concern. Also, *VDD* noise can be more of a concern since we usually want the NMOS devices' gates referenced to ground (V_{bias1} is referenced to *VDD*).

A more general, and better, solution is to bias the gates of the NMOS with a gate-drain-connected NMOS, as seen in Figs. 22.30, 26.62, and 26.63. This allows the gate voltage of the NMOS to move to a higher voltage than its drain (allowing the

op-amp to function with lower *VDD*). For example, the diff-amp in Fig. 26.53 has a DC output voltage of roughly 600 mV (= V_{bias1}). A more appropriate voltage for the gate of the NMOS device is 800 mV. Remembering that the gate-source voltages of the NMOS diff-pair (Fig. 26.18) are roughly 400 mV puts the drains of the diff-pair at 400 mV. The result: *VDD* is more evenly divided across the devices in the diff-amp.

ADDITIONAL READING

[1] V. S. L. Cheung, H. C. Luong, M. Chan, and W. H. Ki, "A 1-V 3.5mW CMOS Switched-Opamp Quadrature IF Circuitry for Bluetooth Receivers," *Symp. VLSI Circuits Dig.* 16, pp. 140–143, June 2002.

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[12] R. Castello and P. R. Gray, "A high-performance micropower switched-capacitor filter," *IEEE Journal of Solid-State Circuits,* vol. 20, pp. 1122–1132, Dec. 1985.

[13] T. C. Choi, R. T. Kaneshiro, R. Broderson, and P. R. Gray, "High-Frequency CMOS Switched Capacitor Filters for Communication Applications," *IEEE Journal of Solid State Circuits,* vol. SC-18, pp. 652–664, December 1983.

[14] D. Senderowicz, S. F. Dreyer, J. H. Huggins, C. F. Rahim, and C. A. Laber, "A family of differential NMOS analog circuits for a PCM codec filter chip," *IEEE Journal of Solid-State Circuits,* vol. 17, pp. 1014–1023, December 1982.

PROBLEMS

Unless otherwise indicated, use the 50 nm CMOS process from the examples in this chapter, the biasing circuit in Fig. 26.3, and 10/1 NMOS and 20/1 PMOS.

26.1 Using simulations, determine the transition frequencies, f_T , for the NMOS and PMOS devices seen in Fig. 26.1 at the nominal operating conditions indicated in the figure. Show that by increasing the MOSFET's overdrive voltage, the f_Ts of the MOSFETs increases.

26.2 Simulate the operation of the two-stage op-amp in Fig. 26.2. Show that the quiescent current in the output buffers is considerably below the desired 20 μA. (Note that the inputs of the op-amp should be held at V_{CM} in the simulation to keep the diff-amp conducting current.) Does this affect the speed of the output buffer? Why or why not?

26.3 Plot reference current against resistor value for the BMR seen in Fig. 26.3. Use simulations to determine the I_{REF} for each value of resistance.

26.4 Comment on the benefits and/or concerns with the CMFB input connections seen in Fig. 26.61. Use simulations to support your answers. Note the similarity to the way CMFB was implemented in Fig. 26.17.

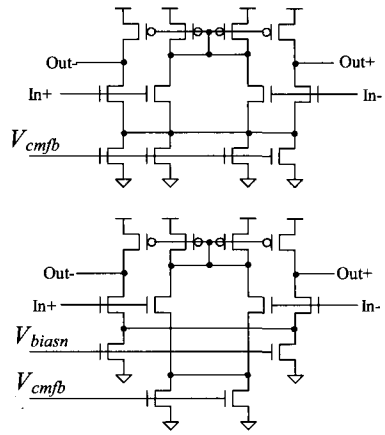

Figure 26.61 Circuits for Problem 26.4.

26.5 Verify, using simulations, that the circuit in Fig. 26.9 does indeed amplify the difference between V_{biasp} and the average on the + inputs of the amplifier.

Comment on the operation of the circuit, making sure it is clear that the limitations, uses, and operation of the amplifier are understood.

26.6 Simulate the operation of the CMFB circuit in Fig. 26.16.

26.7 Is *VDD* divided evenly amongst the drain-source voltages of the MOSFETs in Fig. 26.19? Suggest a method to better divide *VDD* amongst the MOSFETs used in the diff-amp.

26.8 Suggest a simple method to speed up the step response of the op-amp in Fig. 26.22 in the circuit of Fig. 26.24. Verify the validity of your suggestion using SPICE simulations.

26.9 Suggest an alternative method to the one seen in Fig. 26.32 for controlling the output buffer's current. Using the modification, regenerate the results seen in Fig. 26.36.

26.10 Is the CMFB loop stable in the op-amp of Fig. 26.40? Use the large-signal test circuit seen in Fig. 26.24 (at a slower frequency) and simulations to look at the stability of this loop. Suggest, and verify with simulations, methods to improve the stability of the CMFB loop.

26.11 Repeat Problem 26.10 for the op-amp in Fig. 26.43.

26.12 As discussed at the end of the chapter and in Fig. 26.59 and the associated discussion, the input common-mode voltage which drops below V_{CM}, can shut off the op-amp's input diff-amp and cause problems. The diff-amp's NMOS devices have a nominal V_{GS} of 400 mV, leaving only 100 mV across the diff-amp's tail current. Show, using the op-amp in Fig. 26.39 in the configuration seen in Fig. 26.24 with an input common-mode voltage less than 500 mV (the input pulse waveforms average to a voltage less than V_{CM}), the resulting problems. Show that increasing the widths of the NMOS diff-pair (and the mirrored NMOS in the bias circuit with gates tied to V_{CM}) from 10 to 30 helps to increase the operating range (four MOSFET widths are increased from 10 to 30). What happens if only the diff-pair widths (two MOSFETs) are increased?

26.13 Repeat Problem 26.12 for the op-amp in Fig. 26.40. What happens if the input common-mode voltage becomes greater than 500 mV?

26.14 Repeat Problem 26.12 for the op-amp in Fig. 26.43. What happens if the input common-mode voltage becomes greater than 500 mV? Why does the op-amp in Fig. 26.40 perform better with variations in the input common-mode voltage than the op-amp in Fig. 26.43?

26.15 Design and simulate the operation of an op-amp using gain-enhancement (Fig. 26.42) and with an open-loop DC gain greater than 2,000, based on the topologies seen in Figs. 26.40 or 26.43. Simulate the operation of your design and generate outputs like those seen in Fig. 26.44.

26.16 Figure 26.62 shows an op-amp based on the topology seen in Fig. 26.40 but biased for lower *VDD* operation. Select the size of the added gate-drain connected MOSFET to allow for proper operation. Simulate the operation of the design showing the DC gain and large signal step responses (as in Fig. 26.34 and 26.35).

26.17 Repeat Problem 26.16 for the op-amp in Fig. 26.43.

26.18 Using the diff-amp in Fig. 26.63 in the configuration seen in Fig. 26.54 (with SC CMFB) and the output buffer in Fig. 26.56 (again with SC CMFB), regenerate the waveforms seen in Fig. 26.60.

26.19 A switched-capacitor integrator is an example of a circuit that uses an op-amp that can't have the outputs of its diff-amp or output buffer shorted when ϕ_1 goes high. Using the diff-amp in Fig. 26.63 (with SC CMFB) and the output buffer in Fig. 26.56 without the switches (again with SC CMFB), demonstrate the operation of a SC integrator.

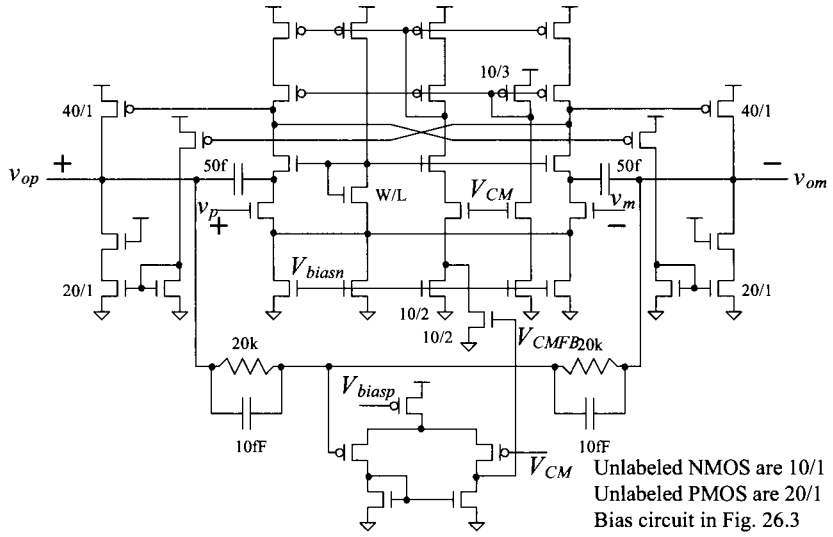

Figure 26.62 An op-amp with better biasing (but more power) for lower VDD operation.

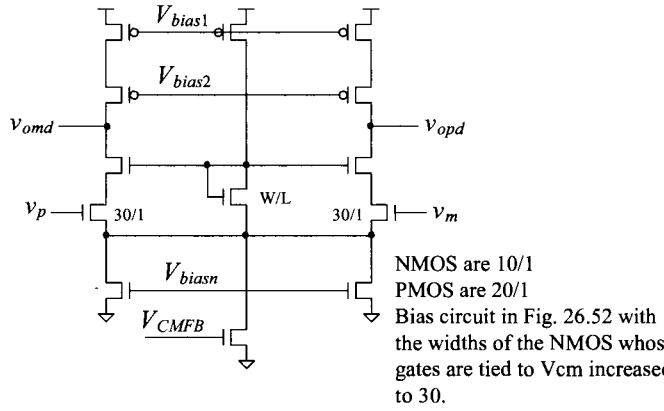

Figure 26.63 Modifying the diff-amp seen in Fig. 26.53 for wider swing operation.