Chapter

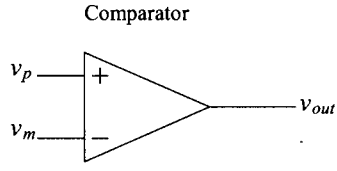
27

Nonlinear Analog Circuits

In this book we've studied digital circuits (two discrete amplitude levels) and linear analog circuits (circuits whose input signals are linearly related to the circuits' output signals). In this chapter, we discuss several circuits that are not purely analog or digital. We term these circuits *nonlinear analog circuits* (the inputs are not linearly related to the outputs). In particular, we discuss voltage comparator analysis and design, adaptive biasing, and analog multiplier design.

27.1 Basic CMOS Comparator Design

The schematic symbol and basic operation of a voltage comparator are shown in Fig. 27.1. The comparator can be thought of as a decision-making circuit. If the +, v_p, input of the comparator is at a greater potential than the –, v_m, input, the output of the comparator is a logic 1, whereas if the + input is at a potential less than the – input, the output of the comparator is at a logic 0. Although the basic op-amps developed in Ch. 24 can be used as a voltage comparator, in some less demanding low-frequency or speed applications, we do not consider the op-amp as a comparator. Instead, in this chapter, we discuss practical comparator design and analysis where propagation delay and sensitivity are important.



$v_p > v_m$ then $v_{out} = VDD$ = logic 1

$v_p < v_m$ then $v_{out} = 0$ = logic 0

Figure 27.1 Comparator operation.

A block diagram of a high-performance comparator is shown in Fig. 27.2. The comparator consists of three stages: the input preamplifier, a positive feedback or decision stage, and an output buffer. The pre-amp stage (or stages) amplifies the input signal to improve the comparator sensitivity (i.e., increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage (*this is important*, see the discussion in Sec. 16.2.1). The positive feedback stage determines which of the input signals is larger. The output buffer amplifies this information and outputs a digital signal. Designing a comparator can begin with considering input common-mode range, power dissipation, propagation delay, and comparator gain.

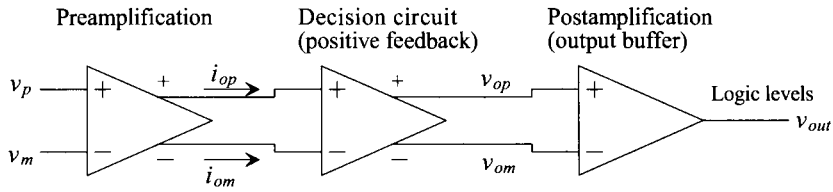


Figure 27.2 Block diagram of a voltage comparator.

Preamplification

For the preamplification (pre-amp) stage, we chose the circuit of Fig. 27.3. For this first section we'll use the long-channel CMOS process to illustrate the design procedures (since long-channel MOSFETs follow the square-law equations). This circuit is a differential amplifier with active loads. The sizes of M1 and M2 are set by considering the diff-amp transconductance, g_m, and the input capacitance. The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the sizes of M1 and M2. Notice that there are no high-impedance nodes in this circuit, other than the input and output nodes. This is important to ensure high speed. Using the sizes given in the schematic, we can relate the input voltages to the output currents (noting i_{op} and i_{om} are the small-signal AC currents in the circuit) by

$$i_{op} = \frac{g_m}{2}(v_p - v_m) + \frac{I_{SS}}{2} = I_{SS} - i_{om} \tag{27.1}$$

Noting that if $v_p > v_m$, then i_{op} is positive i_{om} is negative ($i_{op} = -i_{om}$).

Decision Circuit

The decision circuit is the heart of the comparator and should be capable of discriminating mV-level signals. We should also be able to design the circuit with some hysteresis (see Ch. 18) for use in rejecting noise on a signal. The circuit that we use in the comparator under development is shown in Fig. 27.4. The circuit uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain of the decision element.

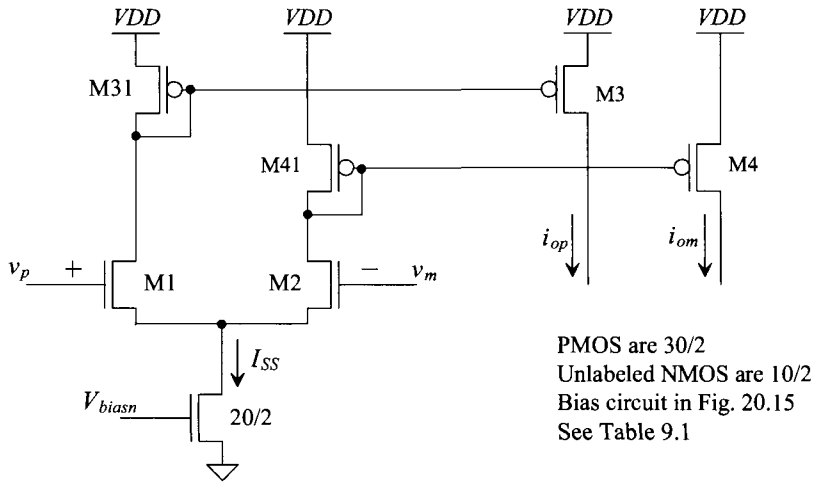


Figure 27.3 Preamplification stage of comparator.

Let's begin by assuming that i_{op} is much larger than i_{om} so that M5 and M7 are on and M6 and M8 are off. We also assume that $\beta_5 = \beta_8 = \beta_A$ and $\beta_6 = \beta_7 = \beta_B$. Under these circumstances, v_{om} is approximately 0 V and v_{op} is

$$v_{op} = \sqrt{\frac{2i_{op}}{\beta_A}} + V_{THN} \tag{27.2}$$

If we start to increase i_{om} and decrease i_{op}, switching starts to take place when the gate-source voltage of M8 is equal to V_{THN}. As we increase M8's V_{GS} beyond V_{THN} (by further increasing i_{om} with the corresponding decrease in i_{op}), M6 starts to take current away from M5. This decreases the drain-source voltage of M5/M6 and thus turns M7 off.

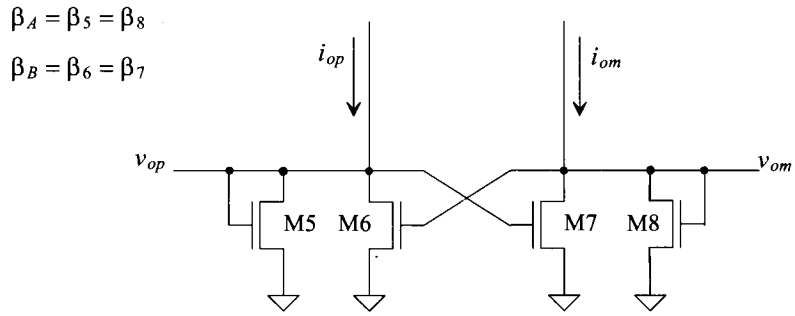


Figure 27.4 Positive feedback decision circuit.

When M8 is just about to turn on (M8's V_{GS} is approaching V_{THN} but the drain currents of M8 and M6 are still zero), the current flowing in M7 is

$$i_{om} = \frac{\beta_B}{2}(v_{op} - V_{THN})^2 \tag{27.3}$$

and the current flowing in M5 is

$$i_{op} = \frac{\beta_A}{2}(v_{op} - V_{THN})^2 \tag{27.4}$$

Noting that the current in M7 (at the switching point) mirrors the current in M5, we can write

$$i_{op} = \frac{\beta_A}{\beta_B} \cdot i_{om} \tag{27.5}$$

If $\beta_A = \beta_B$, then switching takes place when the currents, i_{op} and i_{om}, are equal. Unequal βs cause the comparator to exhibit hysteresis. Relating these equations to Eq. (27.1) yields the switching point voltages (review Ch. 18), or

$$V_{SPH} = v_p - v_m = \frac{I_{SS}}{g_m} \cdot \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} \text{ for } \beta_B \geq \beta_A \tag{27.6}$$

and

$$V_{SPL} = -V_{SPH} \tag{27.7}$$

Consider the following example.

Example 27.1

For the circuit shown in Fig. 27.5, estimate and simulate the switching point voltages for two designs: (1) $W_5 = W_6 = W_7 = W_8 = 10$ with $L = 1$ and (2) $W_5 = W_8 = 10$ and $W_6 = W_7 = 12$ with $L = 1$.

For the first case (using the data in Table 9.1)

$$\beta_A = \beta_B = 120 \frac{\mu A}{V^2} \cdot \frac{10}{1} = 1.2\ mA/V^2$$

so that, as seen in Eq. (27.6) $V_{SPH} = V_{SPL} = 0$. In other words, the comparator does not exhibit hysteresis. Simulation results are shown in Fig. 27.6. The input v_m is set to 2.5 V, while the v_p input is swept from 2.48 to 2.52 V. Note that the amplitudes of v_{op} and v_{om} are limited.

For the second case

$$\beta_A = 120 \frac{\mu A}{V^2} \cdot \frac{10}{1} \text{ and } \beta_B = 120 \frac{\mu A}{V^2} \cdot \frac{12}{1}$$

or $\beta_B = 1.2\beta_A$. Using Eqs. (27.6) and (27.7) with $I_{SS} = 40$ μA and $g_m = 150$ μA/V (again, see Table 9.1), we get

$$V_{SPH} = -V_{SPL} = \frac{I_{SS}}{g_m} \cdot \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} = \frac{40}{150} \cdot \frac{1.2 - 1}{1.2 + 1} = 24\ mV$$

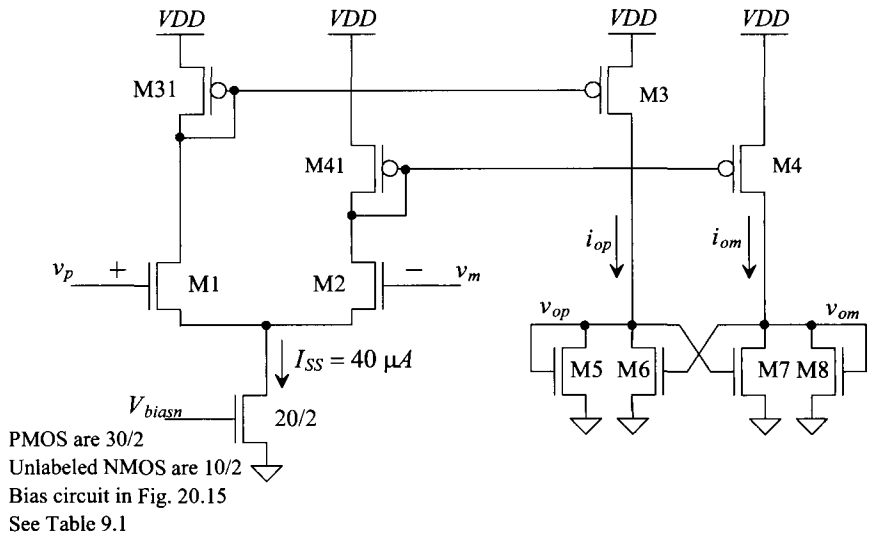
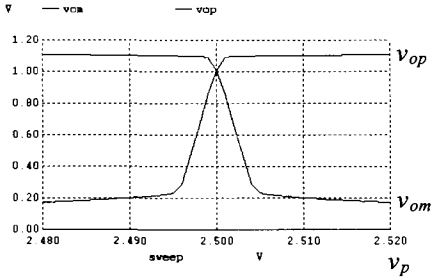
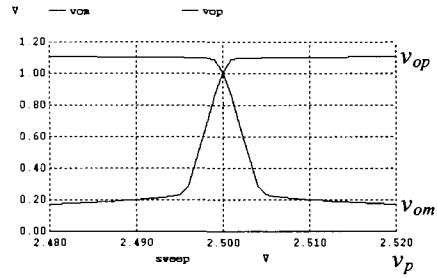


Figure 27.5 Schematic of the pre-amp and decision circuit used in Ex. 27.1.



(a) Minus input held at 2.5 V while the positive input is swept from 2.4 to 2.6 V.



(b) Minus input held at 2.5 V while the positive input is swept from 2.52 to 2.4.

Figure 27.6 The outputs of the decision circuit in Fig. 27.5 without hysteresis.

The simulation results are shown in Fig. 27.7. Figure 27.7a shows a sweep of v_p from 2.4 to 2.6 V, with v_m held at 2.5 V. Since V_{SPH} is 24 mV, the decision circuit switches states when v_p is 24 mV above v_m (i.e., when v_p = 2.524 V). The case of v_p being swept from 2.6 to 2.4 V is shown in part (b) of the figure. Switching occurs in this situation when v_p is approximately 2.476 V, or 24 mV, less than 2.5 V. ■

Output Buffer

The final component in our comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or *VDD*). The output buffer should accept a differential input signal

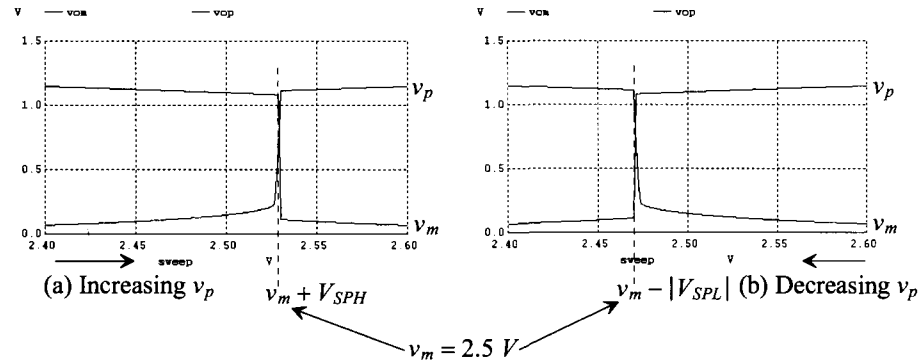


Figure 27.7 Simulating the pre-amp and decision circuit with hysteresis.

and not have slew-rate limitations. We might try to use a NAND SR latch as seen back in Fig. 16.35. However, with process shifts we might run into the situation where the switching points of the gates aren't centered in the middle of the limited swing of the decision circuit's outputs. For a general comparator design, we'll use a diff-amp to help regenerate the digital output signals. For a simple design for the output buffer, we can use the self-biased diff-amp seen back in Fig. 18.17. To move the decision circuit's output swing into the common-mode range of the diff-amp, we can add a gate-drain connected device as seen in Fig. 27.8. An inverter was added on the output of the amplifier as an additional gain stage and to isolate any load capacitance from the self-biasing differential amplifier. This comparator works very well. However, the current in the self-biased stage can be (relatively) huge. This can be a problem if power is a concern (as it is in the Flash ADC discussed in Ch. 29).

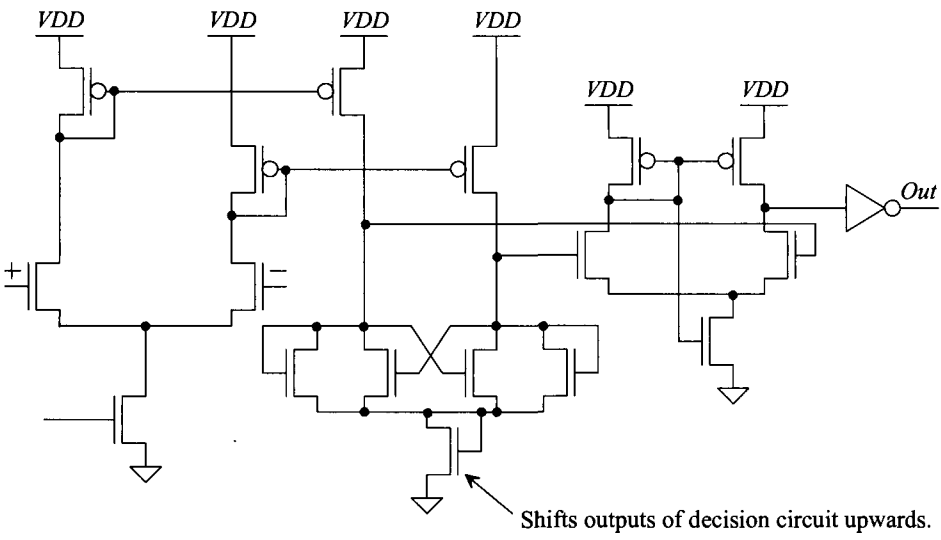


Figure 27.8 Using a self-biased diff-amp for the output buffer.

Figure 27.9 shows a comparator design with both a PMOS and NMOS diff-amp feeding the decision circuit (for input common-mode range beyond the power supply rails). The output buffer is a PMOS diff-amp driving an inverter. While this op-amp won't be as fast as the op-amp seen in Fig. 27.8, it is a good general purpose design. The current drawn from *VDD* will be considerably less than the design in Fig. 27.8. Note that the output currents of the PMOS diff-amp, on the input of the comparator, are added to the NMOS (current) outputs to ensure that current is always sourced to the decision circuit. We might be tempted to connect the PMOS diff-amp directly to the decision circuit. However, this would result in a larger minimum input common-mode voltage.

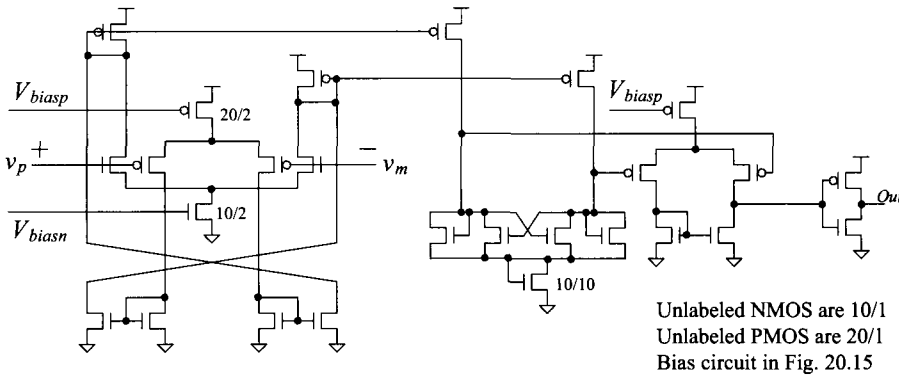


Figure 27.9 General-purpose comparator with rail-to-rail input common-mode range.

27.1.1 Characterizing the Comparator

Comparator DC Performance

Figure 27.10 shows the DC simulated performance of the comparator in Fig. 27.9. The positive comparator input is swept from 0 to *VDD* (= 5 V) while the negative input is stepped for each simulation from 0 to 5 in 500 mV increments (to show wide input common-mode range). Also seen in this figure is the comparator's current draw from *VDD*. Included in this current is the current supplied to the bias circuit.

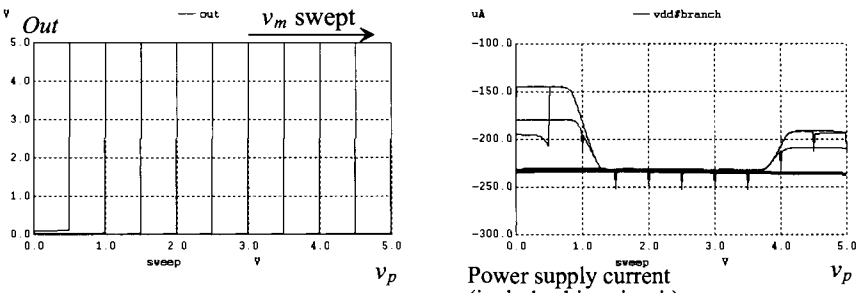


Figure 27.10 DC performance of the comparator in Fig. 27.9

If we take the derivative of these transfer curves, the gain of the comparator and thus the smallest difference that can be discriminated between v_p and v_m becomes known. We have to be careful here with the step size used in the DC simulation. If, for example, we were to use a step size of 1 mV, then the maximum gain we get from the simulation is 1,000. Figure 27.11 shows the expanded view of the comparator with the minus input held at 2.5 V while the positive input is swept from 2.499 to 2.501 V. The offset seen in the figure is a systematic offset (as discussed earlier). The gain of the comparator is, roughly, 175,000. Notice that the comparator was designed without hysteresis. However, in a practical comparator mismatch in the decision circuit results in hysteresis (and so if hysteresis isn't desired, the layout of the decision circuit is critical and may require common-centroid techniques).

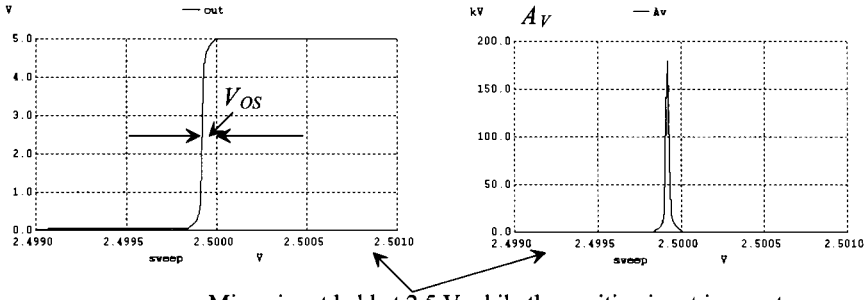


Figure 27.11 The gain of the comparator in Fig. 27.9

Transient Response

The transient response of a comparator can be significantly more difficult to characterize than the DC characteristics. Let's begin by considering v_m = 2.5 V DC, with the v_p input to the comparator a 10 ns wide pulse and an amplitude varying from 2.45 to 2.55 V. This is termed a narrow pulse with a 50 mV overdrive; we are driving the + input of the comparator 50 mV over the negative input. The simulation results for these inputs are shown in Fig. 27.12. If the pulse amplitude or width is reduced much beyond this, the comparator does not make a full transition. Notice how we only show simulation data after 120 ns. This was done to ensure the bias circuit had time to start-up and stabilize before changing the inputs of the comparator.

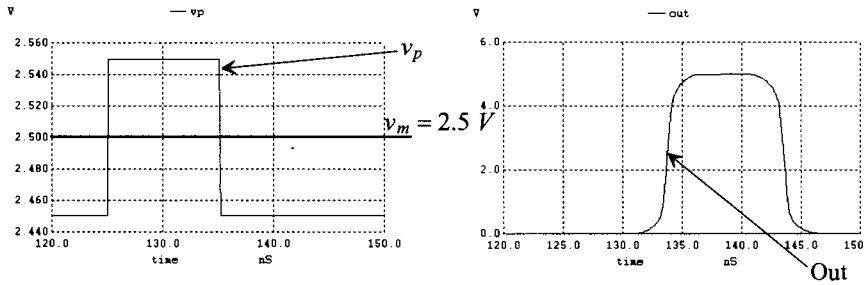


Figure 27.12 Transient response of the comparator in Fig. 27.9.

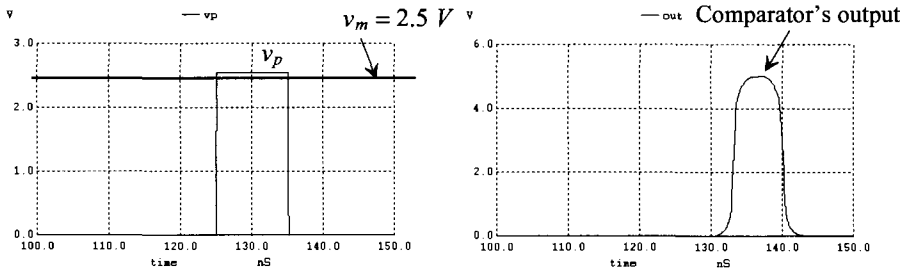


Figure 27.13 Transient response of the comparator in Fig. 27.9 with one side of the pre-amp initially shut off.

Although these results are interesting, they are not practically useful in some situations. In few cases will the comparator discriminate between signals similar to what is seen in Fig. 27.12. A better indication of comparator performance is to apply a signal that starts at a voltage where one side of the differential amplifier is cut off and to finish at a voltage slightly larger than the reference voltage (2.5 V in the above example), Fig. 27.13. In applying a 0 to 2.6 V pulse to the v_p input, the left side of the diff-amp is initially off and then on. The internal comparator nodes must be charged over a wider voltage range with a 0–2.6 V input when compared to the 2.45–2.55 V example of Fig. 27.12. In order to keep one side of the pre-amp from turning off, the circuit of Fig. 27.14 can be used. The added MOSFET ensures that the voltage between the drains of M31 and M41 don't deviate too much. This configuration is sometimes referred to as a clamped input stage. Note that the size of the added MOSFET should be as small as possible to avoid unneeded loading in the diff-amp (which slows down the comparator's performance).

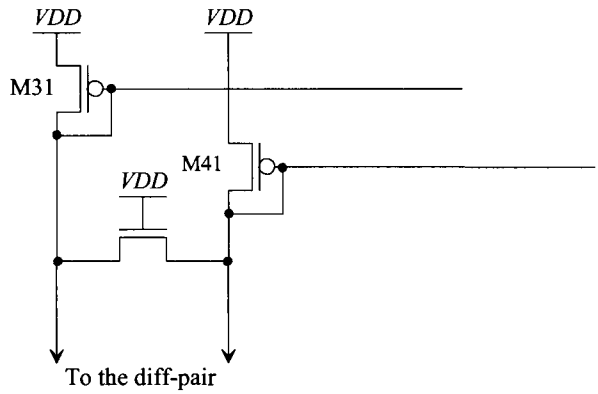


Figure 27.14 Adding a balancing resistor to the input stage of a comparator. See Fig. 27.5

Propagation Delay

Ideally, the propagation delay (the time difference between the input, v_p, crossing the reference voltage, v_m, and the output changing logic states) is zero. For the comparator of Fig. 27.9 with simulation results shown in Fig. 27.12, the delay of the comparator is approximately 9 ns (or less with an overdrive). This should be compared with the delay of an op-amp used as a comparator, which may be several hundred nanoseconds (because of the compensation capacitor). Another interesting fact about comparator design is that the delay of a comparator can be reduced by cascading gain stages. In other words, the delay of a single high-gain stage is in general longer than the delay of several low-gain stages. Improvements in comparator sensitivity and speed can be directly related to improvements in the preamplifier. A derivation (similar to that given in Ch. 11 for minimum delay through an inverter string driving a load capacitance, C_L) of the number of stages, N, needed in a preamplifier to reach minimum delay for a given load capacitance and input capacitance results in

$$N = \ln \frac{C_L}{C_{in}} \tag{27.8}$$

In the derivation of this equation, it was assumed that the driving resistance of any stage is $1/g_{mn}$ (the transconductance of the n^{th} differential amplifier stage). In practice, Eq. (27.8) is of little use because one side of the differential amplifier can be off. For this reason (and others such as size and power draw), comparators with more than two or three pre-amp stages are not common.

Minimum Input Slew Rate

The last characteristic we discuss is the minimum input slew rate of a comparator. If the input signals to the comparator vary at a slow rate (e.g., a sine wave generated from the AC line), the output of the comparator may very well oscillate resulting in an output with a metastable state. If a comparator is to be used with slowly varying signals, or in a noisy environment, the decision circuit should have hysteresis. The minimum input slew rate is difficult to simulate with SPICE because of the slow and fast varying signals present at the same instant of time in the circuit. This same situation (metastability) can also occur if the input overdrive is small. The result, for this case, however, is an increase in the delay time of the comparator.

27.1.2 Clocked Comparators

We developed "sense amplifiers" in Sec. 16.2.1. The sense amplifier can be used as a clocked comparator, that is a comparator whose outputs change on the rising (or falling) edge of a clock. Consider the clocked comparator in Fig. 27.15. This circuit is directly taken from Figs. 16.32 and 16.35. It works very well for signal differences that are tens of millivolts. When *clock* is low, the inputs to the NAND SR latch are pulled high. The outputs of the comparator don't change. When *clock* goes high, the two inputs are compared causing the output of the circuit to register which one is higher. As discussed in detail back in Ch. 16, the minimum input voltages for this comparator are above the threshold voltage of the NMOS devices. Further if the input signals get too large, MB1 and MB2 move deep into the triode region. The small differences in their channel resistances adversely affect the quality of the comparator's decisions. Let's modify this topology for better sensitivity, wider input signal swing, and better immunity to kickback.

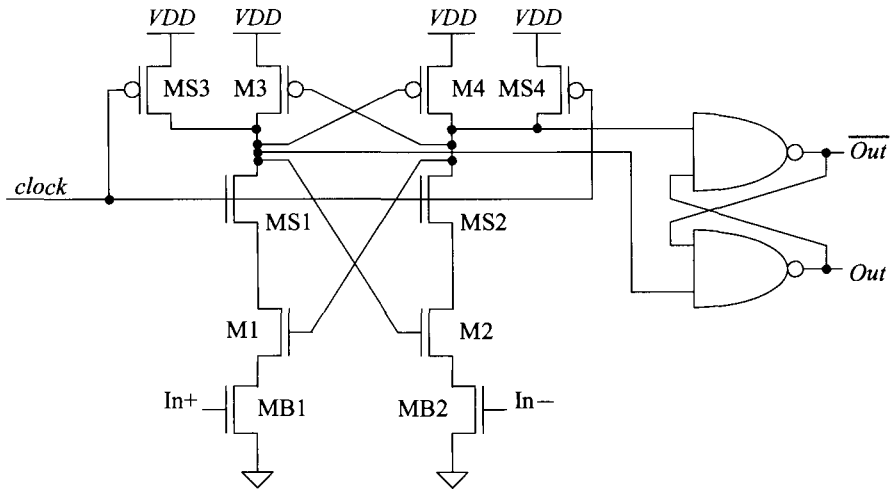


Figure 27.15 A clocked comparator based on Figs. 16.32 and 16.35.

Our modification is seen in Fig. 27.16. Instead of biasing the PMOS and NMOS diff-amps with a bias circuit, here, to be different, we simply use long-length MOSFETs. The bias currents aren't too critical in this application (like they are in an op-amp design). We can still use a bias circuit if controlling the bias current is, for some reason, important. We've removed the triode-operating MOSFETs MB1 and MB2 from the basic cross-coupled latch section. Now we are steering currents from one side of the latch to the other. The differences in the currents causes the latch to switch dependent on the input signals. Note that if either of the diff-amps isn't present in the comparator or if one is off because the comparator's input common-mode voltage is too high or too low, the comparator still works as desired. Only one diff-amp is needed to create the imbalance. Also note, again, that the SR latch is used to make the outputs of the circuit change on the rising edge of the clock signal. If the outputs of the comparator can go high, for a particular application, when the clock signal is low then the NAND gates can be removed.

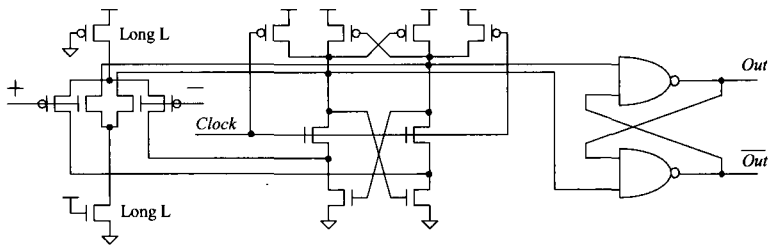


Figure 27.16 Wide-swing clocked comparator. Outputs change on the rising edge of the clock signal.

27.1.3 Input Buffers Revisited

When we discussed input buffers back in Ch. 18 we used a self-biased design for the highest speed (see Fig. 18.17 and the associated discussions). As discussed in Ch. 18, it's desirable to have symmetrical propagation delays independent of input slew-rate, amplitudes, or direction (high-to-low or low-to-high). Towards the more ideal input buffer, consider using two NMOS self-biased buffers in parallel, as seen in Fig. 27.17. Here, to maintain good symmetry, we've split the current sources in half and used one side to generate a common-mode feedback signal to balance the outputs. To reduce the power dissipation in the buffer, the triode-operating MOSFETs can have their lengths increased. Further, for rail-to-rail input common-mode range, we can place the PMOS version of this buffer in parallel with the NMOS version seen in Fig. 27.17, as we did in Fig. 18.23. This input buffer can be very useful for low-skew, high-speed design.

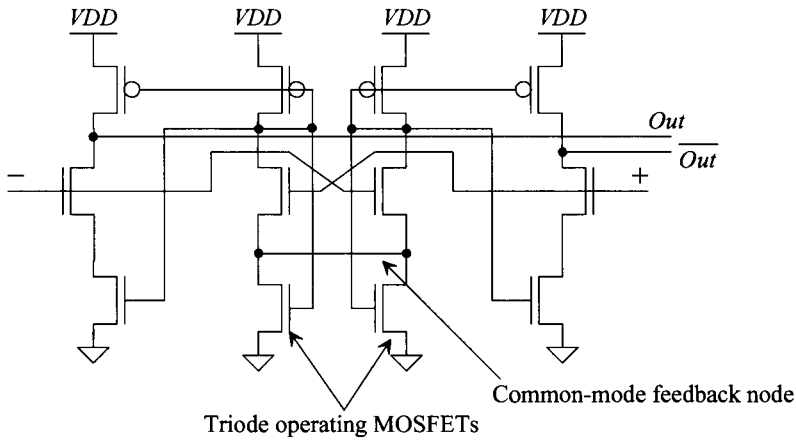


Figure 27.17 A fully-differential input buffer based on the topology discussed in Sec. 18.17.

27.2 Adaptive Biasing

Adaptive biasing can reduce power dissipation in an amplifier while at the same time increasing output current drive capability. Figure 27.18 can be used to help illustrate the idea. When v_{I1} and v_{I2} are equal, the current sources I_{SS1} and I_{SS2} are zero (an open). The diff-amp DC tail current is simply I_{SS}, the same as an ordinarily biased diff-amp. If v_{I1} becomes larger than v_{I2}, the current source I_{SS1} increases above zero, effectively increasing the diff-amp DC bias current. Similarly, if v_{I2} becomes larger than v_{I1}, the current source I_{SS2} increases above zero. The diff-amp output current is normally limited to I_{SS} when one side of the diff-amp shuts off. However, now that the maximum output current is limited to either $I_{SS} + I_{SS1}$ or $I_{SS} + I_{SS2}$. Power dissipation can be reduced using an adaptive bias, and slew-rate problems can be eliminated.

If $v_{I1} = v_{I2}$ then $I_{SS1} = I_{SS2} = 0$.

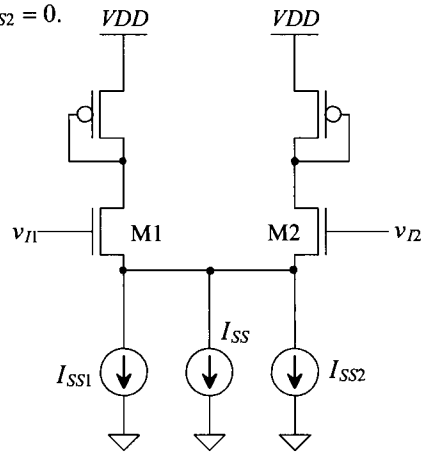


Figure 27.18 Adaptively biased diff-amp.

The current diff-amp of Fig. 27.19 can be used to implement the current source I_{SS1} or I_{SS2}. If the currents I_1 and I_2 are equal, then zero current flows in M3 and M4. Also, if I_2 is greater than I_1, zero current flows in M3 and M4. If I_1 is larger than I_2, the difference between these two currents $(I_1 - I_2)$ flows in M3. Since M4 is K times wider than M3, a current of $K(I_1 - I_2)$ flows in M4 (normally $K < 1$). Two of these diff-amps are needed to implement the adaptive biasing of the diff-amp of Fig. 27.18.

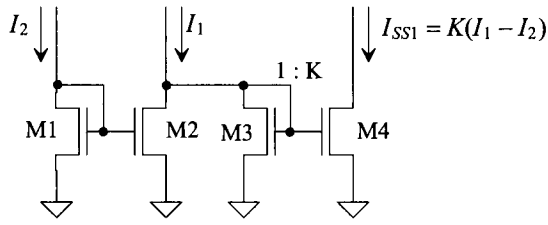


Figure 27.19 Current diff-amp used in adaptive biasing.

Figure 27.20 shows the implementation of adaptive biasing into the diff-amp of Fig. 27.18. P-channel MOSFETs are added adjacent to M3 and M4 to mirror the currents through M1 and M2 (I_1 and I_2). The maximum total current available through M1 occurs when M2 is off. Positive feedback exists through the loop M1, M3, M5–M7. Initially, when M2 shuts off, the current in M1 and M3 is I_{SS}. This is mirrored in M5 and M6, and thus I_{SS1} becomes $K \cdot I_{SS}$. At this particular instance in time, the tail current, which flows through M1, is now $I_{SS} + K \cdot I_{SS}$. However, provided the MOSFETs M1, M3–M7 remain in

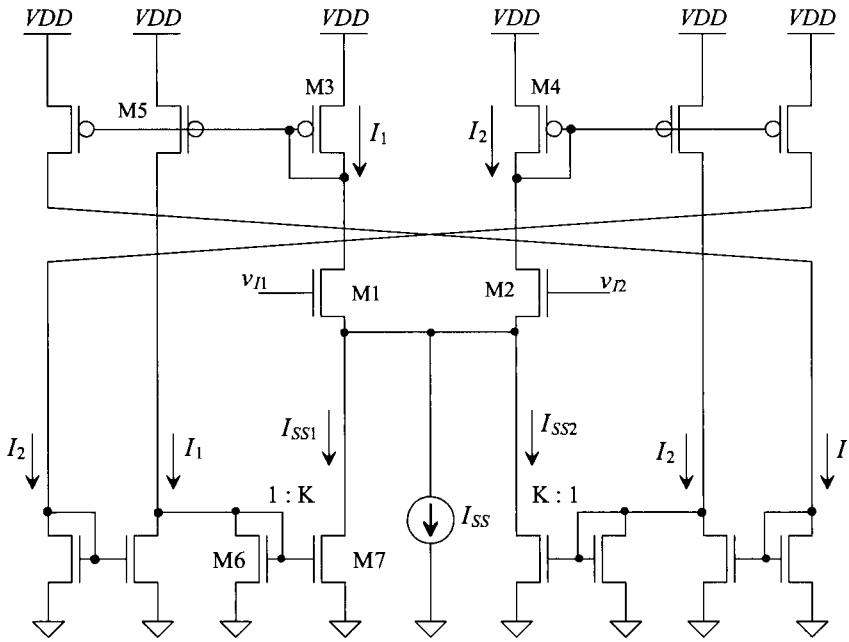


Figure 27.20 Adaptively biased diff-amp.

saturation, this current circles back around the positive feedback loop and increases by K. This continues, resulting in a final or total tail current of

$$I_{tot} = I_{SS} \cdot (1 + K + K^2 + K^3 + ...) \tag{27.9}$$

If $K < 1$, this geometric series can be written as

$$I_{tot} = \frac{I_{ss}}{1 - K} \tag{27.10}$$

Setting $K = 0$ (MOSFET M7 doesn't exist) results in no adaptive biasing and a total tail current of I_{SS}. Setting $K = 1/2$ (M7 half the size of M6) results in a total available tail current of $2 \cdot I_{SS}$. Because the tail current limits the slew rate, when the diff-amp is driving a capacitive load, making K equal to one eliminates slew-rate limitations while at the same time not increasing static power dissipation. In practice, shutting off one side of the diff-pair, M1/M2, is difficult since the adaptive biasing has the effect of lowering the source potentials of the diff-pair, keeping both MOSFETs on. Adaptive biasing can be used in a comparator where M1 or M2 can shut off. However, the static power dissipation will be large; therefore, there is no benefit over the comparators discussed earlier in the chapter. When applying adaptive biasing to an OTA design, the value of K should be unity or less. [Using a K of 1 or 2 can still result in a finite I_{tot} since the MOSFETs have a finite output resistance and the MOSFETs in the diff-pair will not shut off, as was assumed in the derivation of Eq. (27.10)].

A final example of an adaptive voltage-follower amplifier is shown in Fig. 27.21. This amplifier can only source current to a load. If v_{in} and v_{out} are equal, the current that flows in M1 and M2 is $I_{SS} + I_{D6}$. If v_{in} is increased, the current in M1 and M3 increases. This causes the currents in M4–M6 to increase, effectively increasing the tail current of the diff-pair. The result is a large current available to drive the load. Note that M7 can be sized larger than the other MOSFETs to increase maximum output current.

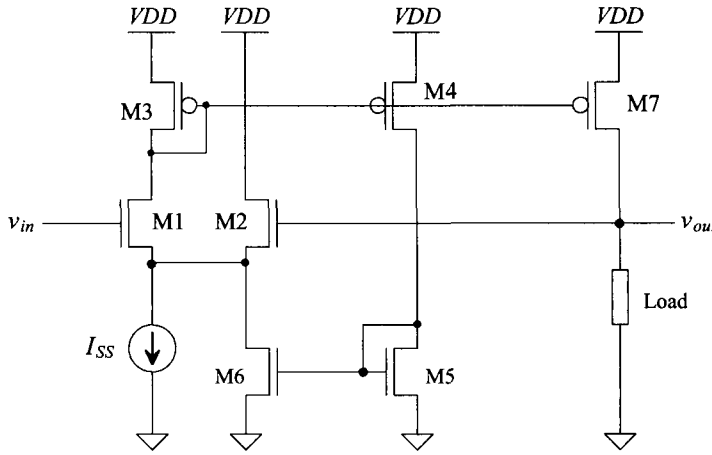


Figure 27.21 Adaptive voltage follower.

27.3 Analog Multipliers

Analog multipliers find extensive use in communication systems. Figure 27.22 shows the voltage characteristics of a four-quadrant multiplier. This multiplier is termed a four-quadrant multiplier because both inputs can be either positive or negative around a common-mode voltage, V_{CM}. The ideal output of the multiplier is related to the inputs by

$$v_{out} = K_m \cdot v_x v_y \tag{27.11}$$

where K_m is the multiplier gain with units of V^{-1}. In reality, imperfections exist in the multiplier gain, resulting in offsets and nonlinearities. The output of the multiplier can be written as

$$v_{out} = K_m(v_x + V_{OSx})(v_y + V_{OSy}) + V_{OSout} + v_x^n + v_y^m \tag{27.12}$$

where V_{OSx}, V_{OSy}, and V_{OSout} are the offset voltages associated with the x-, y-inputs, and the output, respectively. The terms v_x^n and v_y^m represent nonlinearities in the multiplier. Normally, these nonlinearities are specified in terms of the total harmonic-distortion or by specifying the maximum deviation in percentages between a straight line and the actual characteristic curves shown in Fig. 27.22 over some range of input voltages. Although many different techniques exist for implementing analog multipliers in CMOS, we concentrate on a technique useful in high- and low-frequency multiplication.

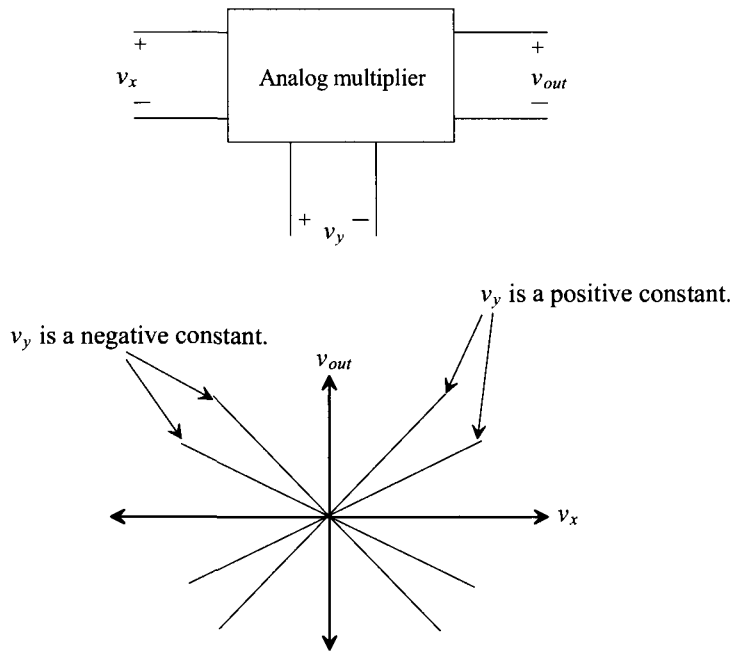


Figure 27.22 Operation of a four-quadrant analog multiplier.

27.3.1 The Multiplying Quad

A CMOS multiplier employing a multiplying quad (M1–M4) is shown in Fig. 27.23. The multiplying quad operates in the triode region, and thus MOSFETs M1–M4 can be thought of as resistors. For the moment we will not consider the biasing of the quad. The negative output voltage of the multiplier is given by

$$v_{om} = -R \cdot (i_{D1} + i_{D2}) \tag{27.13}$$

while the positive output voltage is

$$v_{op} = -R \cdot (i_{D3} + i_{D4}) \tag{27.14}$$

The output voltage of the multiplier is

$$v_{out} = v_{op} - v_{om} = R \cdot (i_{D1} + i_{D2} - i_{D3} - i_{D4}) \tag{27.15}$$

A simplified schematic of the multiplying quad with biasing is shown in Fig. 27.24. The op-amp inputs are at an AC virtual ground and at a DC voltage of V_{CM} (the op-amp output common-mode voltage). In order to minimize the DC input current on the x-axis inputs, the common-mode DC voltage on this input is set to V_{CM}. The DC biasing voltage on the y-input is set to a value large enough to keep the quad in triode. The input signals have been broken into two parts (e.g., $v_x/2$ and $-v_x/2$) to maintain generality. In practice, the minus inputs can be connected directly to the bias voltages at the cost of

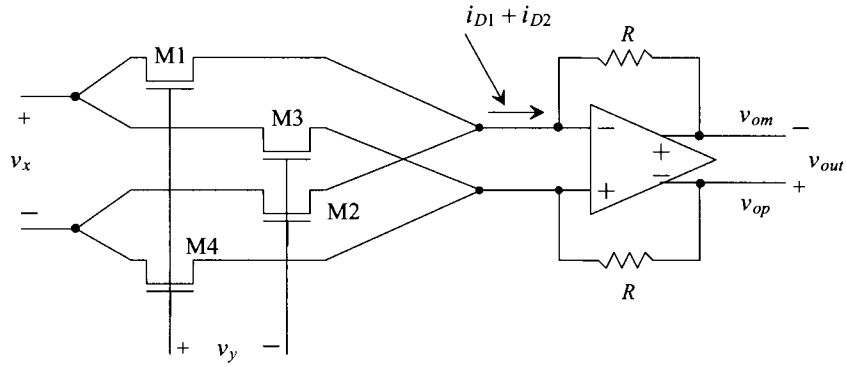


Figure 27.23 CMOS analog multiplier.

large-signal linearity. (The input is not truly differential in this situation.) However, as discussed earlier, a fully differential system has much better coupled noise immunity.

Using Eq. (9.12) and noticing that the DC gate-source voltage of all MOSFETs is the same, the drain currents can be written as

$$i_{D1} = \beta_1 \left[\left(V_{GS} + \frac{v_y}{2} - V_{THN1} \right) \left(\frac{v_x}{2} \right) - \frac{1}{2} \left(\frac{v_x}{2} \right)^2 \right] \tag{27.16}$$

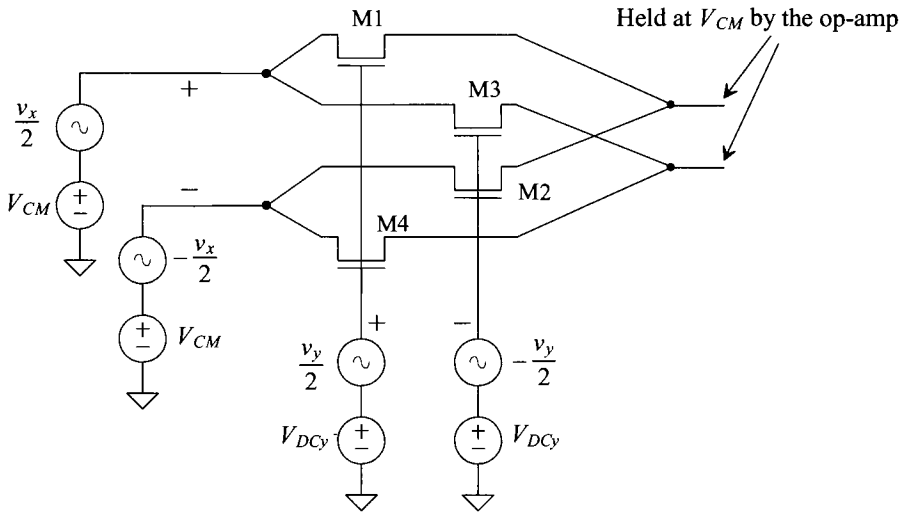


Figure 27.24 Biasing of the multiplying quad.

$$i_{D2} = \beta_2\left[\left(V_{GS} - \frac{v_y}{2} - V_{THN2}\right)\left(-\frac{v_x}{2}\right) - \frac{1}{2}\left(-\frac{v_x}{2}\right)^2\right] \quad (27.17)$$

$$i_{D3} = \beta_3\left[\left(V_{GS} - \frac{v_y}{2} - V_{THN3}\right)\left(\frac{v_x}{2}\right) - \frac{1}{2}\left(\frac{v_x}{2}\right)^2\right] \quad (27.18)$$

$$i_{D4} = \beta_4\left[\left(V_{GS} + \frac{v_y}{2} - V_{THN4}\right)\left(-\frac{v_x}{2}\right) - \frac{1}{2}\left(-\frac{v_x}{2}\right)^2\right] \quad (27.19)$$

We can design so that $\beta = \beta_1 = \beta_2 = \beta_3 = \beta_4$. We can use Eq. (27.15) together with Eqs. (27.16)–(27.19) to rewrite the output voltage of the multiplier as

$$v_{out} = R\beta \cdot \left(\frac{v_x}{2}\right)\left[\frac{v_y}{2} - V_{THN1} + \frac{v_y}{2} + V_{THN2} + \frac{v_y}{2} + V_{THN3} + \frac{v_y}{2} - V_{THN4}\right] \quad (27.20)$$

We can see that if $V_{THN1} = (V_{THN2}$ or $V_{THN3})$ and $V_{THN4} = (V_{THN3}$ or $V_{THN2})$, this equation can be rewritten as

$$v_{out} = R\beta \cdot v_x v_y \quad (27.21)$$

The source of a MOSFET (the terminal we label "source" depends on which way current flows in the MOSFET) in the multiplying quad is connected either to the op-amp or to the x inputs. When the sources of the MOSFETs are connected to the op-amp, all of the MOSFETs in the multiplying quad have the same threshold voltage. (Since the source of each MOSFET is tied to the same potential, the body effect changes each MOSFET's threshold voltage by the same amount.) If the positive x-input is sinking a current, then the sources of M1 and M3 are the "+" x-input and thus $V_{THN1} = V_{THN3}$. In any case, the threshold voltages of the MOSFETs cancel and Eq. (27.21) holds. Comparing Eqs. (27.21) and (27.11) results in defining the gain of this multiplier as

$$K_m = R \cdot \beta \quad (27.22)$$

Simulating the Operation of the Multiplier

Simulating the performance and understanding the analog multiplier operation is an important step in the design process. The design of a multiplier consists of designing the op-amp, selecting the sizes of the multiplying quad, and designing the biasing network. Because we covered the design of differential input/output op-amps in the last chapter, it is not covered here. In order to simulate the performance of a multiplier in SPICE without including the limitations of the op-amp, the simple model shown in Fig. 27.25 is used. The sum of the multiplying factors associated with the voltage-controlled voltage sources, E1 and E2, is the open-loop gain of the op-amp. A typical SPICE statement for these VCVS (voltage-controlled voltage source) where the op-amp open loop gain is 20,000 is

```
E1      Voplus 8 4 3    1E4
E2      8 Vominus 4 3  1E4
```

where the nodes correspond to those labeled in Fig. 27.25.

The next problem we encounter in simulating the operation of the multiplier is implementing the differential voltages (e.g., $\pm\ v_x/2$), in addition to the DC biasing voltages. The setup shown in Fig. 27.26 is used to implement the biasing and the differential voltage sources. The op-amp common-mode output voltage, V_{CM}, and the x

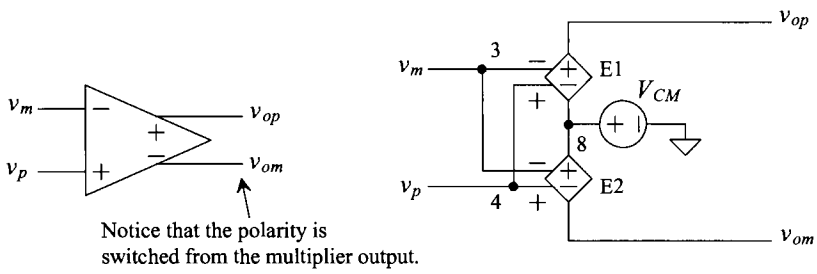


Figure 27.25 SPICE modeling a differential input/output op-amp with common-mode voltage.

input voltage are set to 1.5 V. The lower this voltage, the easier it is to bias the multiplying quad into the triode region. On the other hand, a reduction in the value of V_{CM} limits the op-amp output voltage swing and thus the multiplier output range. The size of the multiplying quad was set to 10/2. The larger the *W/L* ratio of the MOSFETs used in this quad, the easier it is to keep the quad in the triode region. On the other hand, using a large *W/L* increases the required input current. The channel length can be increased to ensure the device operates as a long-channel device and follows Eq. (9.12). Since the quad is part of the feedback around the op-amp, long-channel devices do not affect the

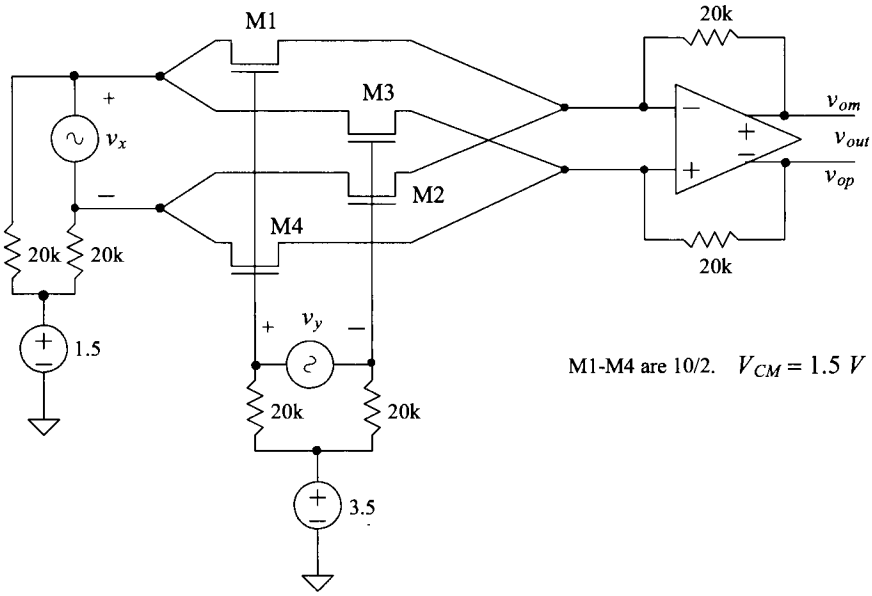


Figure 27.26 SPICE simulation schematic.

speed. The DC voltage at the y-inputs was set to 3.5 V as a compromise between keeping the multiplying quad in triode and the y-input voltage range. The gain of the multiplier in Fig. 27.26 is, from Eq. (27.22) and Table 6.2,

$$K_m = 20k \cdot 120\frac{\mu A}{V^2} \cdot \frac{10}{2} = 12\ V^{-1}$$

A DC sweep showing the operation of the multiplier is shown in Fig. 27.27. The x-input, v_x, was swept from –1 to +1, while at the same time the y-input was stepped from –1 to 1 V in 0.5 V increments. Keeping in mind that the output of the multiplier is $v_{op} - v_{om}$, we can understand the data presented in Fig. 27.27 by considering points A and B. At point A, the y-input is 1 V while the x-input is 0.25 V. The output voltage of the multiplier is the product of the multiplier gain and these two voltages (i.e., 12·1·0.25 = 3 V). The output voltage at point B is 12·0.5·(–0.3) = –1.8 V. Note that this figure was generated using an almost ideal op-amp. The characteristics do not show the limitations of the op-amp. In particular, the limited output swing.

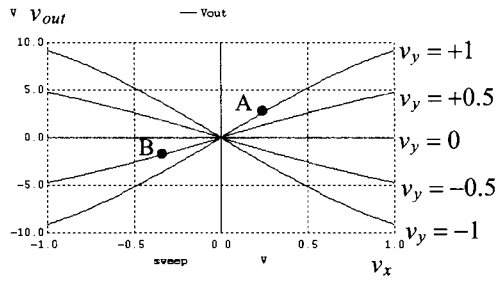


Figure 27.27 DC characteristics of the multiplier of Fig. 26.26.

27.3.2 Multiplier Design Using Squaring Circuits

An analog multiplier can be designed based on the difference between the sum of two voltages squared and the difference of two voltages squared, or

$$V_o = (V_1 + V_2)^2 - (V_1 - V_2)^2 = 4V_1V_2 \qquad (27.23)$$

The basic sum-squaring and difference-squaring circuits are shown in Fig. 27.28. MOSFETs M1 and M4 are source-followers, while MOSFETs M2 and M4 are called squaring MOSFETs. This circuit is designed so that $\beta_1 = \beta_4 = \beta_{14}$, $\beta_2 = \beta_3 = \beta_{23}$, and $\beta_{14} >> \beta_{23}$. This makes almost all of the DC bias currents, I_{S12} and I_{S34}, flow in the MOSFETs M1 and M4, respectively. The squaring current, I_{SQ}, assuming that zero current flows through the resistor when both inputs are zero volts (or whatever the common-mode voltage when a single supply is used), is given by

$$I_{SQ(a)} = \frac{\beta_{23}}{4}(V_1 + V_2)^2 \qquad (27.24)$$

Similarly, the squaring current in the difference-square circuit of Fig. 27.28b is given by

$$I_{SQ(b)} = \frac{\beta_{23}}{4}(V_1 - V_2)^2 \qquad (27.25)$$

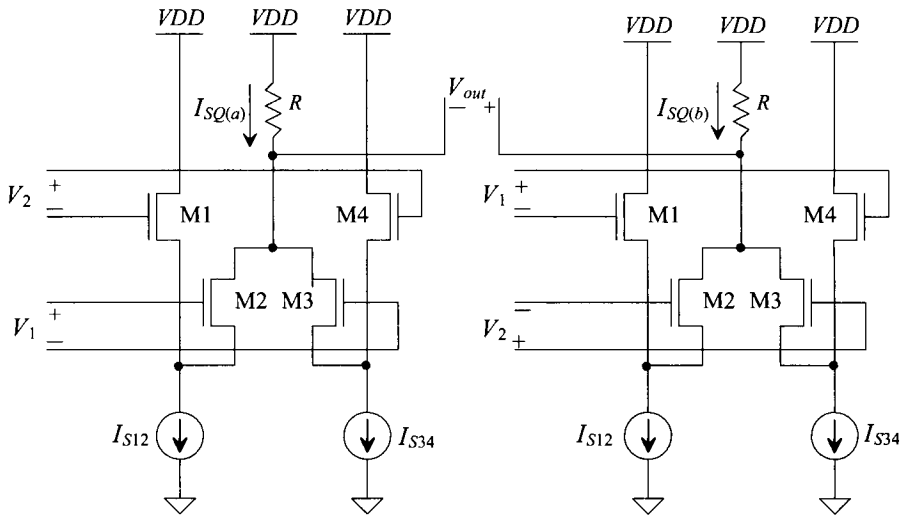


Figure 27.28 (a) Sum-squaring circuit and (b) difference squaring circuit.

The output voltage of the sum-square circuit is given by

$$V_{o-} = VDD - I_{SQ(a)}R \tag{27.26}$$

while the output voltage of the difference-square circuit is given by

$$V_{o+} = VDD - I_{SQ(b)}R \tag{27.27}$$

A multiplier is formed by taking the difference between these voltages. The output voltage of the multiplier of Fig. 27.27 is given by

$$V_{out} = V_{o+} - V_{o-} = R\frac{\beta_{23}}{4}\left[(V_1 + V_2)^2 - (V_1 - V_2)^2\right] \tag{27.28}$$

or, using Eq. (27.23)

$$V_{out} = R\beta_{23} \cdot V_1 V_2 \tag{27.29}$$

The fundamental concern with using this type of multiplier is the fact that modern short-channel CMOS devices don't follow the square-law equations (Eq. [27.24]) we used to derive this result.

ADDITIONAL READING

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PROBLEMS

27.1 Using the long-channel CMOS process, compare the performance (using simulations) of the comparator in Fig. 27.8 with the comparator in Fig. 27.9. Your comparison should include DC gain, systematic offset, delay, sensitivity, and power consumption.

27.2 Show, using simulations, how the addition of a balancing resistor in Fig. 27.14 can be used to improve the response seen in Fig. 27.13.

27.3 Simulate the operation of the comparator in Fig. 27.15 in the short-channel CMOS process. Determine the comparators sensitivity and the kickback noise.

27.4 Repeat problem 27.3 for the comparator in Fig. 27.16. Show that the input common-mode range of the comparator in Fig. 27.16 extends beyond the power supply rails.

27.5 Simulate the operation of the input buffer in Fig. 27.17 in the short-channel CMOS process. How sensitive is the buffer to input slew-rate? How symmetrical are the output rise and fall times? Suggest, and verify with simulations, a method to reduce the power consumed by the input buffer.

27.6 Design a low power clocked comparator for use with a Flash ADC (discussed in Ch. 29). Use the short-channel CMOS process and a clocking frequency of 250 MHz estimate the power dissipated by 256 of these comparators.