Chapter

2

Sampling and Aliasing

The block diagram for one example of a mixed-signal circuit design used to process analog signals is seen in Fig. 2.1. The system's input and output are continuous-time (analog) signals. The input signal is applied to an analog filter, called an anti-aliasing filter (AAF) that limits the input spectral content to avoid aliasing (discussed in Section 2.1) when the signal is sampled and held using the sample-and-hold, S/H (also called a zero-order hold, ZOH), circuit. The output of the S/H is connected to the analog-to-digital converter (ADC) where it is converted to a digital word that changes with time. The digital word is then passed through a digital signal processing (DSP) block where it is manipulated (e.g. lowpass filtered using a digital filter like the one seen in Fig. 1.16). The output of the DSP block is connected to a digital-to-analog converter (DAC) that changes the digital words back into an analog voltage. At this point the signal does have a changing amplitude but it is still discrete in time (jagged as seen in Fig. 2.1). The output of the DAC is fed to a reconstruction filter (RCF) to smooth it out. We'll see that this step removes the spectral content above the Nyquist frequency, f_n or $f_s/2$.

Note that analog circuits are an important component of this system. The AAF and RCF must be completely analog in design. Further, the ADC and DAC may contain precise analog circuits.

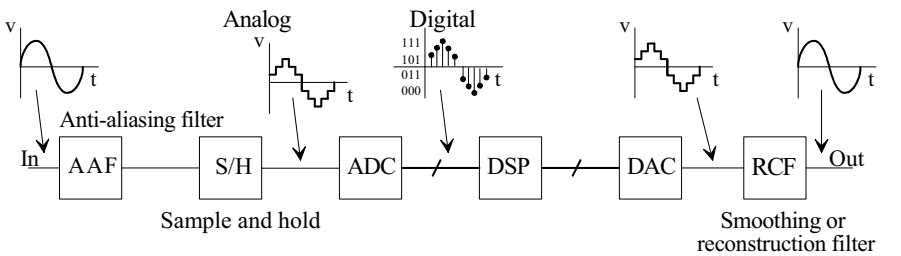

Figure 2.1 Signals resulting from A/D and D/A conversion in a mixed-signal system.

2.1 Sampling

In this section we discuss how sampling a signal changes its spectrum. Impulse sampling, decimation, the sample-and-hold (S/H), the track-and-hold (T/H), interpolation, and *K*-path sampling methods are discussed.

2.1.1 Impulse Sampling

Consider the sampling block diagram shown in Fig. 2.2. Let's assume that we apply a sinewave input, $x(t)$, to this sampling gate of the form, $V_p \sin(2\pi f_{in} \cdot t)$ (for the moment, a single frequency input). The output of the sampling gate (a.k.a. sampler), $y(t)$, is the product of the input and a sampling unit impulse signal (Dirac delta function), $\delta(t - nT_s)$ or

$$y(t) = \sum_{n=-\infty}^{\infty} V_p \sin(2\pi f_{in} \cdot t) \cdot \delta(t - nT_s) \tag{2.1}$$

Noting that the frequency of the input is f_{in} while the sampling frequency is $f_s (= 1/T_s)$, the spectrum of the input signal is seen in Fig. 2.3a. Note that the Fourier series representation of the series of sampling impulses above is

$$\sum_{n=-\infty}^{\infty} \delta(t - nT_s) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} e^{j2\pi n \cdot t/T_s} = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} e^{j2\pi n f_s \cdot t} \tag{2.2}$$

If we take the Fourier transform of the input signal after sampling (we take the Fourier transform of Eq. [2.1]), that is, we look at the spectrum on the output of the sampler, we get

$$Y(f) = \frac{V_p}{2jT_s} \sum_{k=-\infty}^{\infty} \int_{-\infty}^{\infty} [e^{j2\pi(f_{in}+kf_s)t} - e^{-j2\pi(f_{in}-kf_s)t}] \cdot e^{-j2\pi f \cdot t} \cdot dt \tag{2.3}$$

or, knowing the Fourier transform of $e^{j2\pi f_o \cdot t}$ is $\delta(f - f_o)$

$$Y(f) = \frac{V_p}{2jT_s} \cdot \sum_{k=-\infty}^{\infty} [\delta(f - f_{in} - kf_s) - \delta(f + f_{in} - kf_s)] \tag{2.4}$$

The sampled spectrum is repeated, at intervals of f_s, as seen in Fig. 2.3b (the one-sided spectrum is shown, which is what we will use throughout the book). Note that if an ideal lowpass filter (LPF) is applied to the output spectrum of the sampler (the output of the

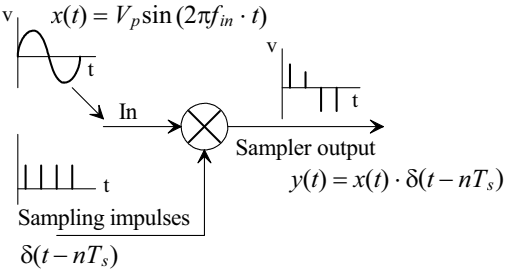

Figure 2.2 Impulse sampling a signal.

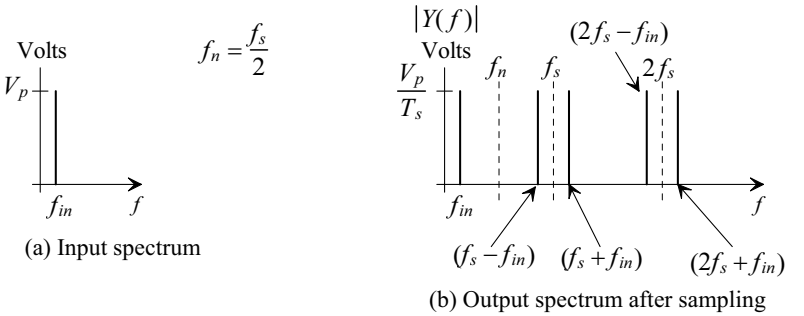

Figure 2.3 One-sided spectrum of a sinewave (a) before and (b) after sampling.

sampler is connected to an ideal LPF) with a bandwidth greater than f_{in} (and lower than f_n [the Nyquist frequency]), then the higher-order frequency components can be removed so that only f_{in} remains (this is our smoothing or reconstruction filter shown in Fig. 2.1).

Example 2.1

A sampling gate is strobed with an impulse train running at a frequency of 100 MHz (f_s = 100 MHz and the time in between the impulses, T_s, is 10 ns). Sketch the resulting output frequency spectrum if a 60 MHz sinewave is applied to the sampler. Also, sketch the time domain input and output of the sampler.

The resulting frequency spectrum is shown in Fig. 2.4. Notice how connecting the output of the sampler through an LPF, with an ideal abrupt cutoff frequency of f_n, results in an output sinewave with a frequency of 40 MHz. In order to avoid this situation, that is, to avoid ending up with the wrong, or alias, signal after sampling and reconstructing, we need to ensure that the signal frequencies applied to the sampler are less than $f_s/2$ (the Nyquist frequency, again, f_n). Reviewing Fig. 2.1, we see that this is the purpose of the antialiasing filter (AAF). Notice how, ideally, both the AAF and RCF (reconstruction filter) in Fig. 2.1 are both ideal LPFs with a cutoff frequency equal to half the sample frequency (the Nyquist frequency). Figure 2.5 shows the time domain sketch of the sampler's output. ■

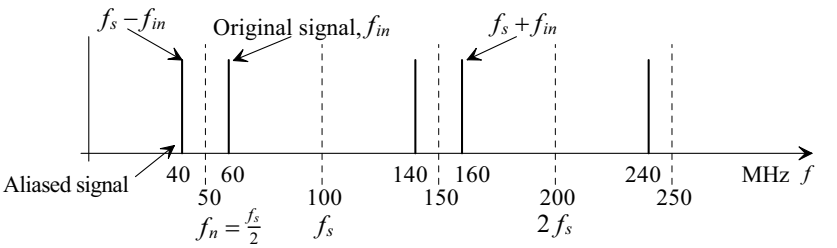

Figure 2.4 Spectrum of a 60 MHz sinewave sampled at 100 MHz.

It should be clear from the preceding discussion that: (1) sampling a signal results in a reproduction of the sampled signal's spectrum at DC, f_s, $2f_s$, $3f_s$, etc., (2) the input signal's spectrum should have no significant spectral content above f_n in order to avoid

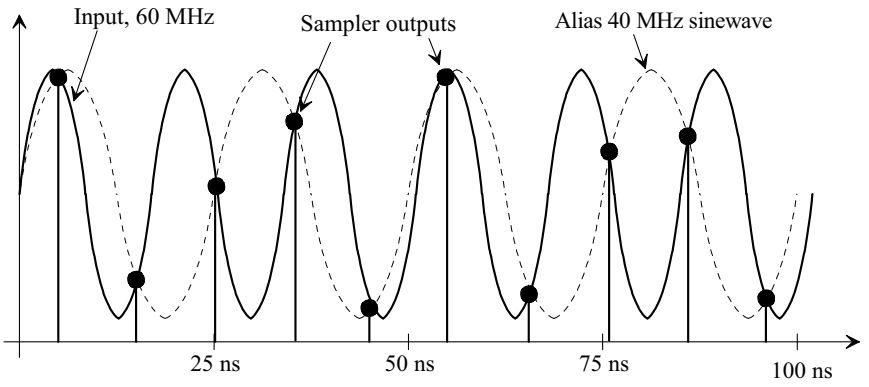

Figure 2.5 Time domain input and output for Ex. 2.1.

aliasing, (3) to avoid aliasing both filtering the input signal using an AAF and increasing the sampling frequency should be used, and (4) to reproduce the sampled signal from the output of the sampler (which is nonzero only during the sampling impulse times) a lowpass RCF should be used.

Note that our discussion illustrates the operation of a sampling gate driven with impulse signals. As shown in Fig. 2.1, a practical system would have other building blocks. We would rarely, if ever, sample a signal and then reconstruct it without processing it first.

A Note Concerning the AAF and the RCF

Before going any further, we should discuss the ideal characteristics of the AAF and the RCF. The ideal characteristics of these filters are shown in Fig. 2.6. Note that both of these filters must be analog by design. The ideal cutoff frequency for the filters can be no greater than f_n (assuming the sampling rate on the input of the system is the same as the sampling rate on the system's output) and the filters should ideally have linear phase. Let's discuss these two ideal characteristics.

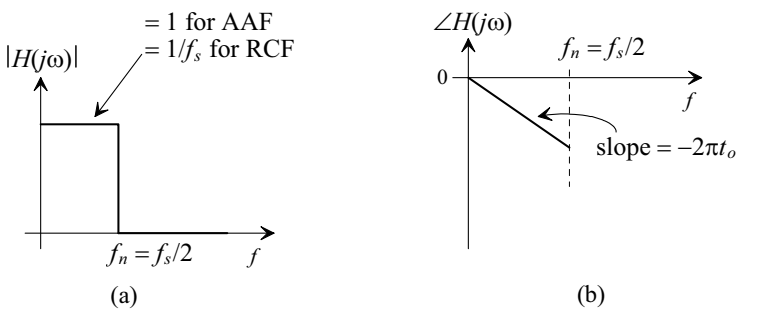

Figure 2.6 (a) Ideal magnitude and (b) phase responses for the AAF and RCF.

The ideal magnitude response, shown in Fig. 2.6a, passes all spectral content below the Nyquist frequency while removing all signals above this frequency. The ideal phase response, shown in Fig. 2.6b, provides a constant delay, t_o, to all signals below f_n. In other words, the filters remove all unwanted signals while not distorting the wanted signals.

Time Domain Description of Reconstruction

In this section we show why the filter shown in Fig. 2.6, an ideal brick wall lowpass filter with linear phase response, is the ideal RCF on the output of our impulse sampler. Shown in Fig. 2.7 is a 20 MHz sinewave sampled at 100 MHz. Suppose we want to reconstruct the original input 20 MHz sinewave from the sampler output (the weighted impulse functions). After reconstruction, the output of the RCF should be a single-tone, 20 MHz sinewave (it should be an exact replica of the sampler input). To determine what happens when the output of our sampler is applied to the ideal RCF, we need to determine the time-domain response of the RCF when its input signal is an impulse.

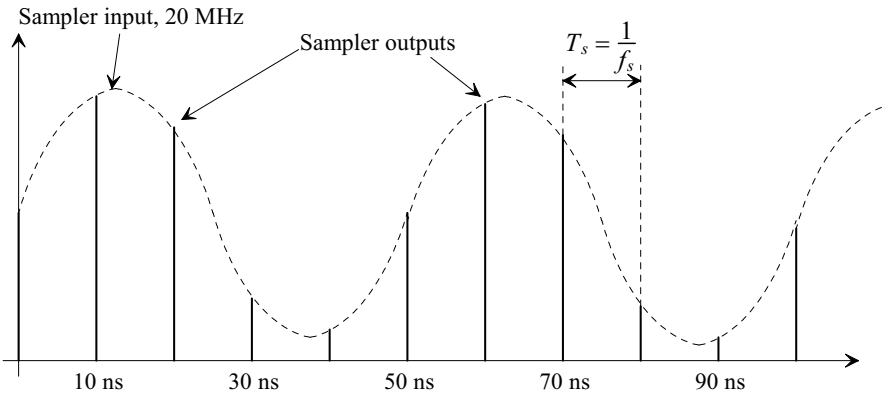

Figure 2.7 Impulse sampling, at 100 MHz, a sinewave at 20 MHz.

The transfer function of a system is the Fourier transform of the system's time domain impulse response (what we are trying to find here). In other words, to determine the transfer function of the system, we apply an impulse to the input of the system (a very large amplitude, very short time duration pulse, Fig. 2.8). We then look at the system's output in the time domain. Taking the Fourier transform of this output gives the system's

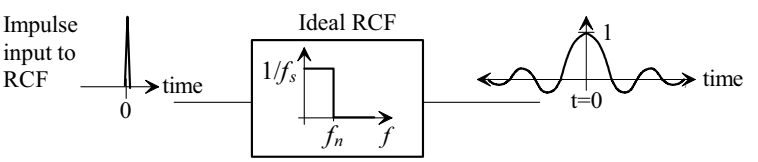

Figure 2.8 Time domain impulse response of the ideal RCF.

transfer function. Therefore (in the reverse order), to determine the time-domain impulse response of the ideal RCF, given the transfer function, we take the inverse Fourier transform of the transfer function. The ideal RCF's transfer function (Fig. 2.6) can be defined by

$$|H(f)| = 1/f_s \text{ for } |f| < f_n \text{ else } |H(f)| = 0 \tag{2.5}$$

The time-domain impulse response is then given, remembering $2f_n = f_s$, by

$$h(t) = \int_{-f_n}^{f_n} \frac{1}{f_s} \cdot e^{j\cdot 2\pi\cdot f\cdot t} \cdot df = \frac{e^{j\cdot 2\pi\cdot f_n\cdot t} - e^{-j\cdot 2\pi\cdot f_n\cdot t}}{j\cdot 2\pi\cdot f_s\cdot t} =$$

$$\frac{\sin 2\pi f_n\cdot t}{\pi f_s\cdot t} = \frac{\sin \pi f_s\cdot t}{\pi f_s\cdot t} = Sinc(\pi f_s\cdot t) \tag{2.6}$$

where

$$\frac{\sin x}{x} \equiv Sinc(x) \tag{2.7}$$

The time-domain impulse response of our ideal RCF is shown in Fig. 2.9. Notice that our impulse is applied to the system's input at $t = 0$ and that the output actually anticipates, or starts, before the application of the input! This indicates that the filter can't be built in a practical analog circuit. Before we discuss the implications of this severe limitation (an ideal reconstruction filter can't actually be built because its impulse response is infinite in time), examine Fig. 2.10. Figure 2.10 shows the individual impulse response outputs of an ideal RCF with the impulse train of Fig. 2.7 as the input. The output of the RCF is the weighted sum of the individual responses. While this figure is "busy," the basic concept of reconstruction can be seen.

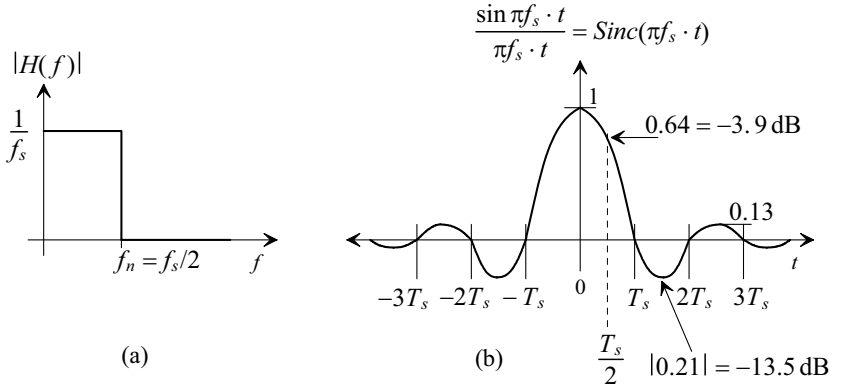

Figure 2.9 (a) Ideal RCF frequency response and (b) impulse response (time).

What can we do to ease the requirements on the RCF? One answer is to increase f_s so it's much larger than the maximum sampled frequency. This solution is the basis for *oversampled data converters* or noise-shaping data converters (studied in detail later in the book). This solution also eases the requirements placed on the AAF. Another idea for easing the design of the RCF is to increase the sample rate of the digital data coming out of the DSP block in Fig. 2.1. This technique is called *interpolation*.

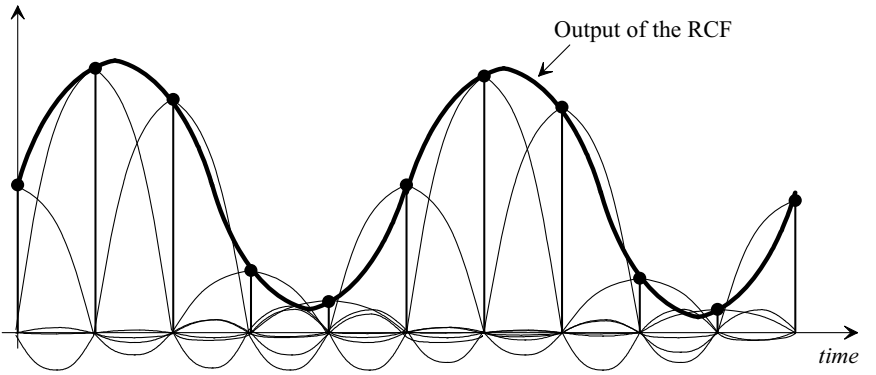

Figure 2.10 Reconstructing the 20 MHz sinewave of Fig. 2.7.

An Important Note

It is important to note that our impulse sampler quantizes[1] the input signal in *time* but not amplitude (unlike an analog-to-digital converter which quantizes the input in both time and amplitude). The amplitude out of the ideal impulse sampler is exactly the same as the amplitude input to the sampler at the sampling impulse times. The *z*-transform can be used to describe systems using both quantization in time as well as in amplitude. In other words, whether we are discussing digital words, in a binary format, or sampled-analog waveforms with amplitudes of volts, amps, or coulombs, we can use the *z*-transform to represent the discrete-time systems that process the signals. Laplace-transforms are used for continuous-time systems.

2.1.2 Decimation

In the last section we focused on sampling analog signals. We can apply the same concepts to digital signals. When a digital signal is "down sampled" its sample rate goes from f_s to a lower rate of f_s/K where K is generally, but not necessarily, a power of 2 (e.g., 2, 4, 8, 16, etc.). This reduction in the effective sampling frequency is termed *decimation* and is illustrated with the block diagram shown in Fig. 2.11. The term decimation (or

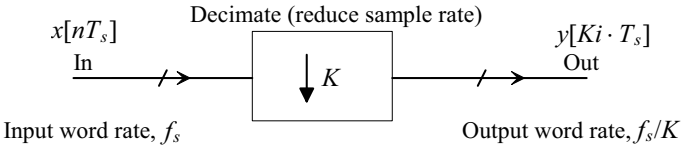

Figure 2.11 Block diagram of a decimation block.

[1] Quantize: to limit the possible values of a quantity to a discrete set of values. Quantizing in time, for example, means that the output amplitude is only defined at certain discrete times (such as the sampling impulse times for the ideal impulse sampler) or that the amplitude is unchanging during certain discrete time intervals (such as seen in the output of the ideal sample-and-hold discussed in the next section).

decimate) can be confusing since, among other uses, the dictionary definition is, "to select by lot and kill one in every ten." The origin of the word comes from a method of punishing military troops by selecting one in every ten for execution. Our much more kind-hearted definition will mean that we are passing the input word through a lowpass digital filter and then down-sampling the result (discarding samples). This procedure is effectively passing the digital data through an antialiasing filter and then resampling the result at a lower rate, Fig. 2.12. Note that the sampling gate is simply a register so it is trivial to implement decimation.

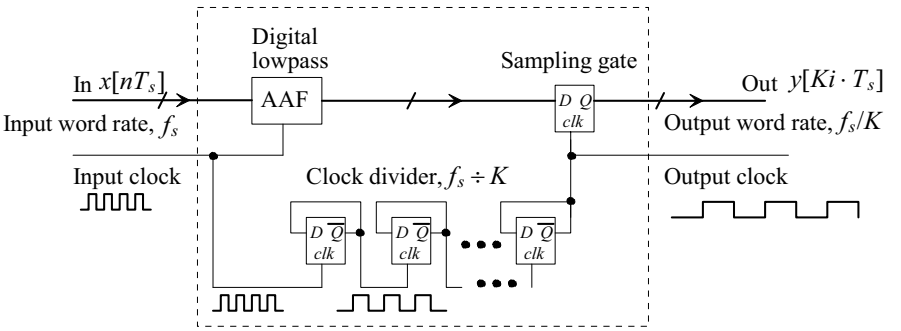

Figure 2.12 Components of a decimation block.

To illustrate the aliasing concerns when using decimation, and $K = 8$, examine Fig. 2.13. The input spectrum of the digital data, in (a), repeats every f_s. The digital input data in (a) is first passed through a digital lowpass filter that is used as an anti-aliasing filter, Fig. 2.13b. The input and output of the digital filter is clocked at f_s in both (a) and (b). In (c) we re-time the input signal at the slower rate. Decimation is used to lower power (because of the reduced clock frequency), simplify circuitry (e.g., serial multipliers can be used), and to lower the amount of data storage required (fewer words to store). Note that to use decimation the *wanted* input spectral content can't extend beyond $f_s/2K$.

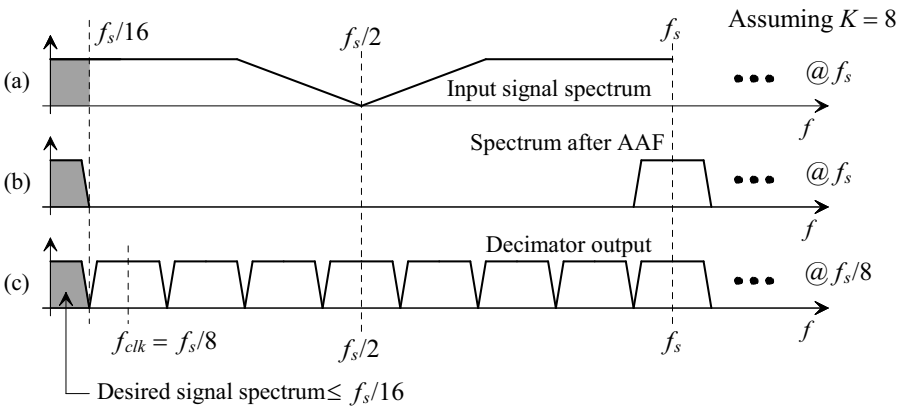

Figure 2.13 Example spectrums when decimation is employed.

2.1.3 The Sample-and-Hold (S/H)

Understanding the operation of the impulse sampler in Sec. 2.1.1 is important in understanding the concepts of aliasing and reconstruction. However, as seen in Fig. 2.1, most mixed-signal systems employ a sample-and-hold (S/H) rather than an impulse sampler so that the sampled waveform is available at times other than the sampling impulse times. Having the samples "held" in between the sampling impulse times is important for proper ADC operation. The disadvantage of using the S/H, as we shall shortly see, is that it will introduce distortion into our signal.

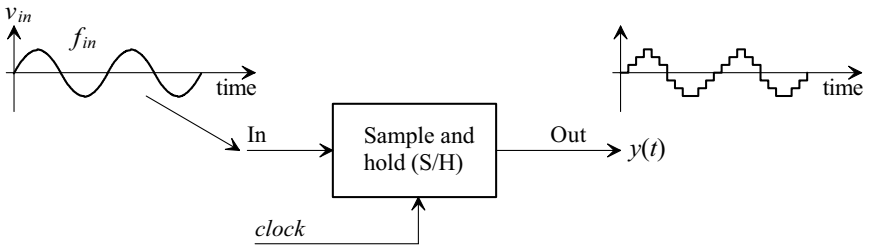

Figure 2.14 Sampling and holding an input sinewave.

S/H Spectral Response

Consider the application of a sinewave, at a frequency f_{in}, to the ideal S/H shown in Fig. 2.14. To make the discussion as general as possible, assume that the output of the S/H can return-to-zero (RZ) as shown in Fig. 2.15 (which shows coarse time quantization for a simpler figure and illustration of the concept of RZ). Note that as T approaches T_s we get the operation of the S/H in Fig. 2.14. The output of the ideal S/H is given by

$$y(t) = \sum_{n=-\infty}^{\infty} [V_p \sin(2\pi f_{in} \cdot nT_s) \cdot [u(t-nT_s) - u(t-nT_s-T)]] \qquad (2.8)$$

As depicted in this equation the input is sampled at the instants nT_s and then held at the sampled value $v_{in}(nT_s)$ for a pulse length of T. We can represent the resulting signal using convolution, see Fig. 2.16a, as

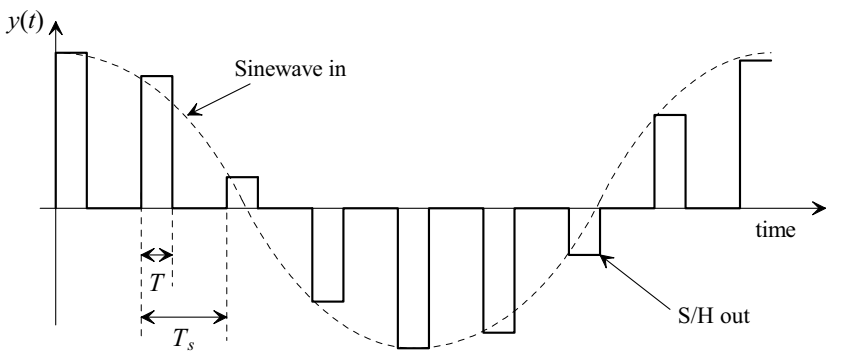

Figure 2.15 Sample-and-hold output with return to zero format.

$$y(t) = \sum_{n=-\infty}^{\infty} \overbrace{[V_p \sin(2\pi f_{in} \cdot t) \cdot \delta(t - nT_s)]}^{v_{in}(nT_s)} \otimes [u(t) - u(t-T)]$$
$$= \left[\overbrace{V_p \sin(2\pi f_{in} \cdot t)}^{v_{in}(t)} \cdot \overbrace{\sum_{n=-\infty}^{\infty} (\delta(t - nT_s))}^{p(t)} \right] \otimes \overbrace{[u(t) - u(t-T)]}^{h(t)} \qquad (2.9)$$

or

$$Y(f) = (v_{in}(f) \otimes P(f)) \cdot H(f) \qquad (2.10)$$

where, see Eq. (2.4),

$$v_{in}(f) \otimes P(f) = \frac{V_p}{2jT_s} \cdot \sum_{k=-\infty}^{\infty} [\delta(f - f_{in} - kf_s) - \delta(f + f_{in} - kf_s)] \qquad (2.11)$$

We can determine the spectrum of the sampling pulse $h(t)$ seen in Fig. 2.16a, $|H(f)|$, by taking its Fourier transform

$$H(f) = \int_0^{T_s} [u(t) - u(t-T)] e^{-j \cdot 2\pi \cdot f \cdot t} \cdot dt \qquad (2.12)$$

which is evaluated as

$$H(f) = \frac{e^{-j \cdot 2\pi \cdot f \cdot T} - 1}{-j \cdot 2\pi \cdot f} = e^{-j \cdot \pi \cdot f \cdot T} \cdot \frac{e^{j \cdot \pi \cdot f \cdot T} - e^{-j \cdot \pi \cdot f \cdot T}}{j \cdot 2\pi \cdot f} = \overbrace{e^{-j \cdot \pi \cdot f \cdot T}}^{\text{phase shift}} \cdot \overbrace{T \cdot Sinc(\pi \cdot f \cdot T)}^{\text{magnitude}} \qquad (2.13)$$

The magnitude of Eq. (2.13), $|H(f)|$, is plotted in Fig. 2.16b. The phase response corresponds to a shift in time of $T/2$. Since

$$Y(f) = (v_{in}(f) \otimes P(f)) \cdot H(f) \qquad (2.14)$$

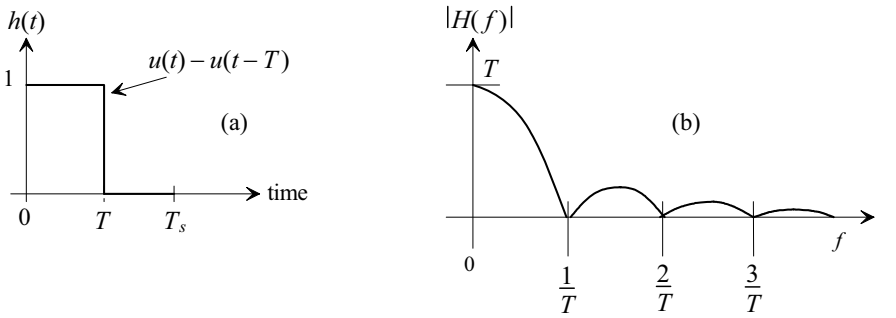

Figure 2.16 (a) Sampling pulse and (b) its spectrum.

$$Y(f) = \left(\frac{1}{T_s}\sum_{k=-\infty}^{\infty} v_{in}(f - kf_s)\right) \cdot T \cdot Sinc(\pi \cdot f \cdot T) \cdot e^{-j\cdot\pi\cdot f\cdot T}$$
$$= \frac{V_p}{2jT_s} \cdot \sum_{k=-\infty}^{\infty} [\delta(f - f_{in} - kf_s) - \delta(f + f_{in} - kf_s)] \cdot T \cdot Sinc(\pi \cdot f \cdot T) \cdot e^{-j\cdot 2\pi\cdot f\cdot \frac{T}{2}} \quad (2.15)$$

or

$$|Y(f)| = \overbrace{T \cdot |Sinc(\pi \cdot T \cdot f)|}^{\text{Weighting from S/H, } |H(f)|} \cdot \overbrace{\left[\frac{V_p}{2T_s} \cdot \sum_{k=-\infty}^{\infty} [\delta(f - f_{in} - kf_s) - \delta(f + f_{in} - kf_s)]\right]}^{\text{Ideal impulse sampler response}} \quad (2.16)$$

As $T \to 0$ the output spectrum of the sample-and-hold approaches the ideal impulse sampler's spectrum seen in Sec. 2.1.1. Note that using an RZ format (making $T < T_s$) can reduce the amount of attenuation (and thus distortion) introduced by the S/H. $|H(f)|$, as seen in Fig. 2.16, doesn't roll off as fast. However, the cost for this is a reduction in the sampled signal power (ultimately we get no signal power out of the S/H as $T \to 0$). Generally, reducing signal-to-noise ratio, SNR, by returning the S/H's output to ground (RZ), to improve distortion performance, is not a good idea. Reducing SNR to improve distortion can be useful in some situations, e.g., digital data transmission, where good SNR isn't as much of a problem as distortion.

For most circuit designs, $T = T_s$ so that, as Eq. (2.16) and Fig. 2.17 show, the sample-and-hold operation weights the amplitude of the ideal impulse sampler's frequency response by $Sinc\,\frac{\pi f}{f_s}$ or $Sinc\,\frac{\pi f}{2f_n}$. Note that at the sampling frequency (f_s=1/T_s) the output of the ideal S/H goes to zero. Also note that at the Nyquist frequency, f_n, the input signal is attenuated by 0.64 or − 3.9 dB. This "droop" in the S/H's response, as mentioned above, adds distortion to the input signal. Let's illustrate the effects of the S/H's frequency response using an example.

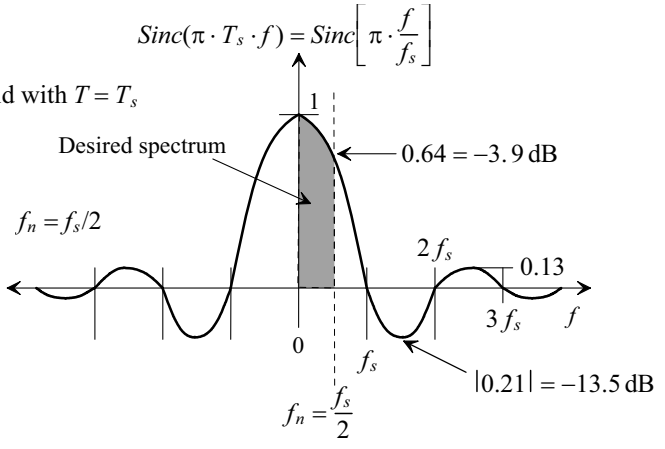

Figure 2.17 The frequency response of a S/H.

Example 2.2
Using an ideal SPICE model for the S/H show, and discuss, the spectrum resulting from sampling a 3 MHz sinewave at 100 Msamples/s.

The results of passing a 0.5 V (peak) sinewave centered at 0.5 V (–9 dB using RMS voltages) through the ideal S/H are shown in the SPICE simulation results seen in Fig. 2.18. Note that SPICE uses a one-sided spectrum so, for example, we must multiply Eq. (2.16) by two to ensure proper signal levels. The attenuation the 97 MHz image sees is

$$\text{Attenuation} = Sinc\left(\frac{\pi \cdot 97}{100}\right) = 0.031 = -30.2\ dB$$

The amplitude of the 97 MHz image is –9 dB below the attenuation resulting from using a S/H or –39.2 dB. At the Nyquist frequency of 50 MHz, an input signal is attenuated by –3.9 dB as seen in Fig. 2.17.

Note that the S/H cannot be used as an AAF since any aliasing that occurred using the impulse sampler still occurs using the S/H. For example, sampling a 60 MHz sinewave at 100 MHz still results in a 40 MHz alias signal in the base spectrum (the spectrum from DC to f_n), as shown in Fig. 2.3. Now, however, the signal is attenuated by the S/H (the attenuation is –2.4 dB at 40 MHz when sampling at 100 Msamples/s.) In other words, the S/H can be thought of as an ideal impulse sampler followed by a *Sinc* response filter.

An important thing to note is that repetitively sampling and holding a signal results in only one S/H attenuation hit (assuming the timing is such that a sampling operation is not occurring when the previous S/H stage's output is changing). This means that topologies that use several S/H operations on an input signal, such as a pipeline ADC, only attenuate the signal by $Sinc(\pi f/f_s)$ once. This is important to understand. ■

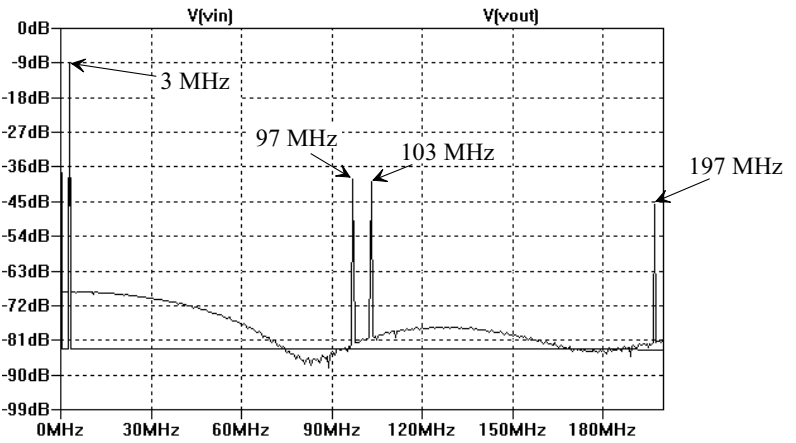

Figure 2.18 Output of a S/H after sampling a 3 MHz sinewave at 100 MHz.

The Reconstruction Filter (RCF)

Ultimately the (processed) output of the S/H (assuming $T = T_s$) should be passed through an RCF to recover the input signal. The spectral shape of the ideal RCF is seen in Fig. 2.19. The response peaks at the Nyquist frequency to compensate for the attenuation introduced by the S/H Sinc response, Fig. 2.17. Note how using the RZ format modifies the requirements placed on the reconstruction filter to the point, when using impulse sampling, of having the brick wall RCF seen in Fig. 2.6. Therefore there is no need for the peaking type response seen below (but using an RZ format reduces the S/H output signal power). Note that in many situations a digital filter may be used to compensate for the droop introduced by the S/H process.

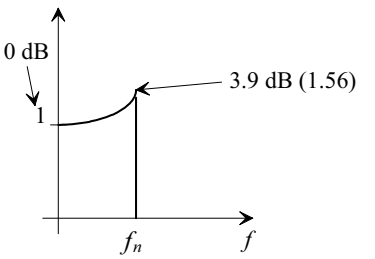

Figure 2.19 Ideal reconstruction filter frequency response for a S/H.

Circuit Concerns for Implementing the S/H

Figure 2.20 shows a single-ended S/H implementation. At the time t_0, the ϕ_1 and ϕ_2 switches are closed while the ϕ_3 switches are open. At this time the input signal charges the bottom plate (left side or, here, the plate closest to the substrate) of the hold capacitor, C_H, while the right side of the capacitor is held at ground by the feedback around the op-amp through the ϕ_1 switch. At t_1 the ϕ_1 switch opens and for a very short time (set by $t_3 - t_1$) the op-amp operates open loop (no feedback). It's assumed that this time is so short that the capacitor doesn't charge or discharge. As the top plate (right side of the capacitor) is always at ground at t_1, the charge injection and capacitive feedthrough

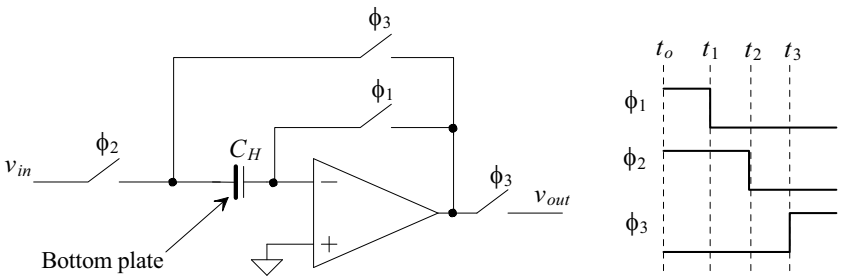

Figure 2.20 Single-ended S/H operation.

resulting from the ϕ_1 switch turning off is independent of the input signal. When the ϕ_2 switch turns off its charge will, ideally, be injected into the low-impedance input, v_{in} , since the impedance looking into the right of the ϕ_2 switch is large. This leaves the voltage across the hold capacitor unaffected. The sequence of turning off the switch to the right of C_H (the top plate) followed by turning off the switch connecting v_{in} to C_H (the bottom plate) is often called *bottom plate sampling*.

Bottom plate sampling is illustrated in its simplest form in Fig. 2.21. In this figure the switch connected to the bottom plate of the capacitor, the ϕ_1 switch, is turned off first. When this happens the charge is injected into the circuit independent of the input signal (each side of the switch is at ground). When the ϕ_2 switch turns off, its charge can be injected into the low-impedance node, the input v_{in} , or into the series combination of C_H and the off ϕ_1 switch. Again, the charge takes the lowest impedance path to ground and thus most of the charge injection resulting from the ϕ_2 switch turning off flows through v_{in}, leaving the voltage across the hold capacitor unaffected. The name "bottom plate sampling" can be confusing. Reviewing Fig. 2.20, we see that the (physical) top plate of the hold capacitor is connected to the ϕ_1 switch while, in Fig. 2.21, the (schematic representation) bottom plate of the hold capacitor is connected to the ϕ_1 switch.

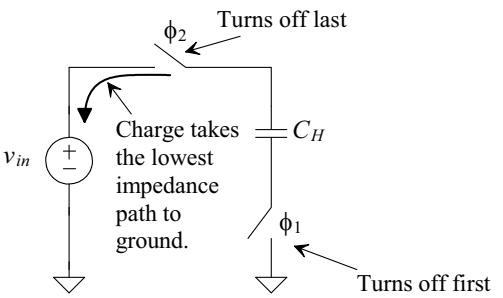

Figure 2.21 Bottom plate sampling.

An Example

Before leaving this section let's give an example of the spectrums associated with (ideal) sampling and reconstruction using a S/H, Figs. 2.1 and 2.22. In Fig. 2.22a we represent an input signal as a continuous spectrum that is not bandlimited (that is, the spectrum is completely occupied). In a real spectrum the spectral components don't have a constant amplitude (e.g. noise at high frequencies may be considerably smaller than desired content at low frequencies) but here, to simplify things, we assume a constant amplitude.

The first step in our example is to pass the input signal through an ideal AAF to limit the spectral content to the Nyquist frequency, $f_s/2$, Fig. 2.22b. At this point the spectrum hasn't been sampled so it doesn't repeat at multiples of f_s. The output of the AAF is then passed through the S/H. In Fig. 2.22c we show the Sinc weighting from the sample-and-hold process but we don't show the effects of sampling. Note the droop in the response at frequencies approaching $f_s/2$. In (d) the output of the S/H is seen. Note how the entire spectrum is occupied. Finally (e) shows the output after passing the S/H's output through an ideal RCF, Fig. 2.19. Note that the spectrum is no longer periodic.

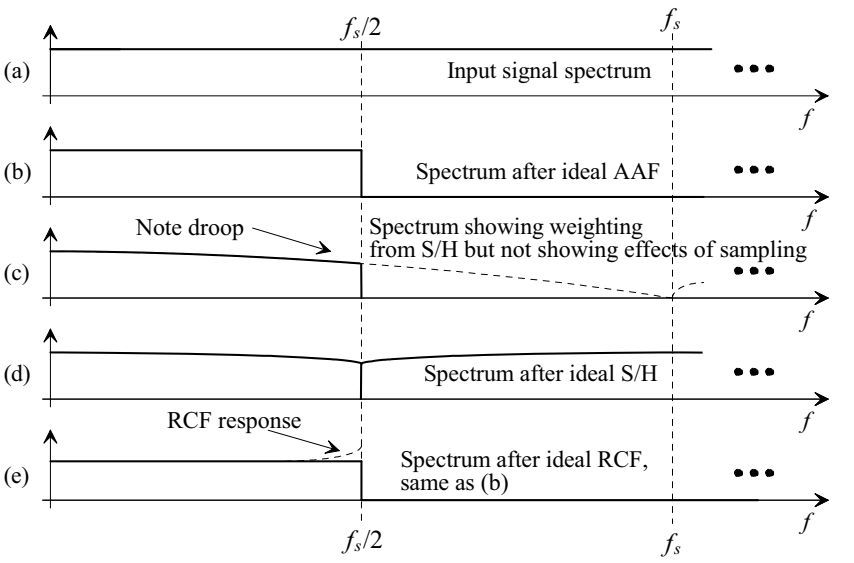

Figure 2.22 Example spectrums when ideal, AAF, S/H, and RCF are used.

2.1.4 The Track-and-Hold (T/H)

Another sampling circuit that is useful in mixed-signal circuits, especially those employing both analog- and digital-signal processing, is the track-and-hold, Fig. 2.23. The T/H is implemented using a sampling gate, here a MOSFET, and a storage capacitor. When the gate of the MOSFET is driven high it turns on and allows the input signal to directly drive the capacitor (the T/H's output). In the following discussion, we are assuming that the product of the MOSFET's on resistance and the hold capacitor, $R_{ch} \cdot C_H$, is much smaller than the period of the input signal.

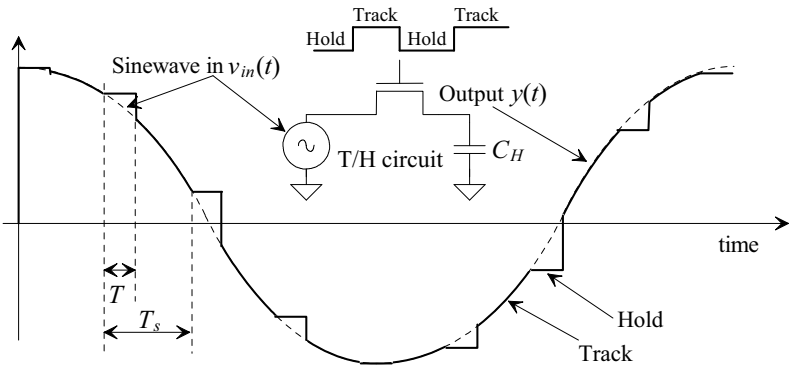

Figure 2.23 Track-and-hold output.

To determine how the T/H affects a sampled signal let's first notice that the *hold* portion of the output is exactly the same as the S/H with RZ format seen in Fig. 2.15, Eq. (2.15). Knowing this we can focus on the *track* portion of the output and then sum the responses to get the overall T/H response. For the track portion of the ideal T/H we can write, see Eq. (2.8),

$$y_t(t) = \sum_{n=-\infty}^{\infty} \{V_p \sin(2\pi f_{in} \cdot t) \cdot [u(t - nT_s - T) - u(t - nT_s - T_s)]\}$$

$$= V_p \sin(2\pi f_{in} \cdot t) \cdot \left\{ h_t(t) \otimes \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \right\} \tag{2.17}$$

Knowing

$$\sum_{n=-\infty}^{\infty} \delta(t - nT_s) \text{ has a Fourier transform of } f_s \sum_{k=-\infty}^{\infty} \delta(f - kf_s) \tag{2.18}$$

we can write

$$Y_t(f) = v_{in}(f) \otimes \left\{ H_t(f) \cdot f_s \sum_{k=-\infty}^{\infty} \delta(f - kf_s) \right\} \tag{2.19}$$

Reviewing Eqs. (2.12) and (2.13) we can write

$$H_t(f) = e^{-j2\pi f \cdot \frac{(T_s+T)}{2}} \cdot (T_s - T) \cdot Sinc(\pi \cdot f \cdot (T_s - T)) \tag{2.20}$$

and so, since $f_s = 1/T_s$,

$$H_t(f) \cdot f_s \sum_{k=-\infty}^{\infty} \delta(f - kf_s) = \frac{T_s - T}{T_s} \cdot \sum_{k=-\infty}^{\infty} e^{-j2\pi \cdot kf_s \cdot \frac{(T_s+T)}{2}} \cdot Sinc(\pi \cdot kf_s \cdot (T_s - T)) \cdot \delta(f - kf_s) \tag{2.21}$$

The track portion of the T/H's output spectrum for an input signal, $v_{in}(f)$, is

$$Y_t(f) = v_{in}(f) \otimes \left[\frac{T_s - T}{T_s} \cdot \sum_{k=-\infty}^{\infty} e^{-j2\pi \cdot kf_s \cdot \frac{(T_s+T)}{2}} \cdot Sinc(\pi \cdot kf_s \cdot (T_s - T)) \cdot \delta(f - kf_s) \right]$$

$$= \frac{T_s - T}{T_s} \cdot \sum_{k=-\infty}^{\infty} \left(e^{-j2\pi \cdot kf_s \cdot \frac{(T_s+T)}{2}} \cdot Sinc(\pi \cdot kf_s \cdot (T_s - T)) \cdot V_{in}(f - kf_s) \right) \tag{2.22}$$

For the single-tone input sinusoid used in Eq. (2.17)

$$Y_t(f) =$$

$$\frac{V_p(T_s - T)}{2jT_s} \cdot \sum_{k=-\infty}^{\infty} \left(Sinc(\pi \cdot kf_s \cdot (T_s - T)) \cdot [\delta(f - f_{in} - kf_s) - \delta(f + f_{in} - kf_s)] \cdot e^{-j2\pi \cdot kf_s \cdot \frac{(T_s+T)}{2}} \right)$$

or (2.23)

$$|Y_t(f)| = \sum_{k=-\infty}^{\infty} \left[\overbrace{(T_s - T) \cdot Sinc(\pi \cdot kf_s \cdot (T_s - T))}^{\text{Weighting from } h_t(t)} \cdot \overbrace{\frac{V_p}{2T_s} \cdot [\delta(f - f_{in} - kf_s) - \delta(f + f_{in} - kf_s)]}^{\text{Ideal impulse sampler response}} \right] \tag{2.24}$$

The total T/H output spectrum, $Y_{T/H}(f)$, for a general input signal $V_{in}(f)$, is the sum of Eqs. (2.15) and (2.22) or

$$Y_{T/H}(f) = \frac{T}{T_s} \cdot Sinc(\pi \cdot f \cdot T) \cdot e^{-j \cdot 2\pi \cdot f \cdot \frac{T}{2}} \cdot \sum_{k=-\infty}^{\infty} v_{in}(f - kf_s) + \frac{T_s - T}{T_s} \cdot \sum_{k=-\infty}^{\infty} \left(e^{-j2\pi \cdot kf_s \cdot \frac{(T_s+T)}{2}} \cdot Sinc(\pi \cdot kf_s \cdot (T_s - T)) \cdot v_{in}(f - kf_s) \right) \quad (2.25)$$

If $T = T_s/2 = 1/2f_s$ then we can write this equation as

$$Y_{T/H}(f) = \sum_{k=-\infty}^{\infty} \left(\left\{ \frac{1}{2} \cdot Sinc\left(\frac{\pi}{2} \cdot \frac{f}{f_s} \right) \cdot e^{-j \cdot \frac{\pi}{2} \cdot \frac{f}{f_s}} + \frac{1}{2} \cdot Sinc\left(\frac{\pi}{2} \cdot k \right) \cdot e^{-j\frac{3\pi}{2} \cdot k} \right\} \cdot v_{in}(f - kf_s) \right) \quad (2.26)$$

We know from Fig. 2.17 that a sinewave at nearly f_n will see an attenuation of 0.64 (–3.9 dB) when using a S/H with $T = T_s$. Using the T/H with $T = T_s/2$ the attenuation the sinewave sees at nearly f_n ($f \to f_s/2$) where $k = 0$ (the frequencies from DC to $f_s/2$) is

$$|Y_{T/H}(f)| = \frac{1}{2} \left| Sinc\left(\frac{\pi}{4} \right) \cdot e^{-j \cdot \frac{\pi}{4}} + 1 \cdot e^{0} \right| \quad (2.27)$$

or

$$|Y_{T/H}(f)| = \frac{1}{2} \left| 0.9 \angle \left(-\frac{\pi}{4} \right) + 1 \angle 0 \right| \quad (2.28)$$

We know we can't directly add the polar representation of these numbers so let's rewrite this equation, noting $0.9 \cos\left(-\frac{\pi}{4}\right) = 0.636$ and $0.9 \sin\left(-\frac{\pi}{4}\right) = -0.636$, using the Cartesian representation as

$$|Y_{T/H}(f)| = \frac{1}{2} |0.636 + j(-0.636) + 1 + j0| = 0.877 \to -1.1\text{dB} \quad (2.29)$$

Note that if we are sampling an analog waveform for Nyquist-rate, analog-to-digital conversion then we have to use a S/H (or the hold portion of the T/H). In this situation we don't want the input to our quantizer (ADC) to vary, as it does in the T/H during the track portion, since this will cause an error called aperture uncertainty (discussed in Sec. 5.2.1).

2.1.5 Interpolation

One of the main assumptions when reconstructing the output signals, in the preceding discussions, is that an RCF is available with a brickwall like shape (Figs. 2.9 and 2.19) and a cutoff frequency of $f_s/2$ (the Nyquist frequency). This, however, is a very challenging analog filter design problem. To make the design of the RCF less challenging we can increase f_s while keeping the desired spectrum limited in bandwidth. In other words, by increasing f_s the effective Nyquist frequency becomes larger than the maximum wanted frequency of interest. This is called *oversampling*.

Decreasing the clock frequency (decimation) was covered in Sec. 2.1.2. Here we cover increasing the clock frequency (call interpolation). Both decimation and interpolation can be used in discrete-time analog signal processing. Here, in this introductory section, we focus on digital signals. When a digital signal is "up sampled" its rate goes from f_s to a higher rate of $K \cdot f_s$. As with decimation, K is generally, but not necessarily, a power of 2. Interpolation is represented as seen in Fig. 2.24.

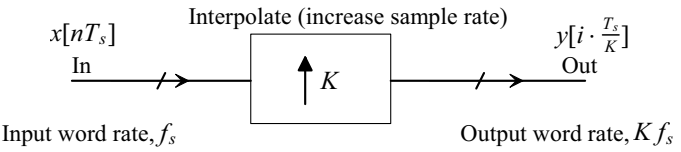

Figure 2.24 Block diagram of an interpolation block.

There are three basic interpolation schemes (ways of increasing the sampling, or clocking, frequency): zero padding, using a hold register, and linear interpolation, Fig. 2.25. Figure 2.25a shows an example input to an interpolator. In (b)-(d) we show interpolation with $K = 4$.

Zero Padding

The benefit of using zero padding, Figs. 2.25b and 2.26, is that the desired spectrum remains unchanged. We'll discuss this more in a moment. The drawback of zero padding is that the amplitude of the output signal drops by K. If our input is a constant value of 1 and we insert 3 zeroes ($K = 4$) then our output has an average value of 0.25 (average of 1, 0, 0, 0). This is normally not a problem for a digital signal since we can simply increase

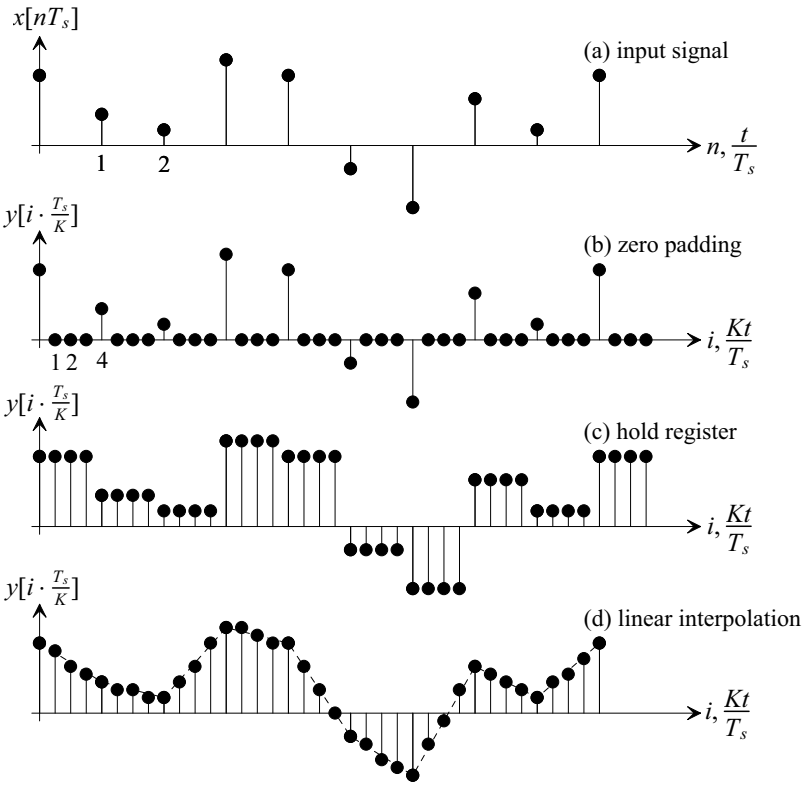

Figure 2.25 Types of interpolation.

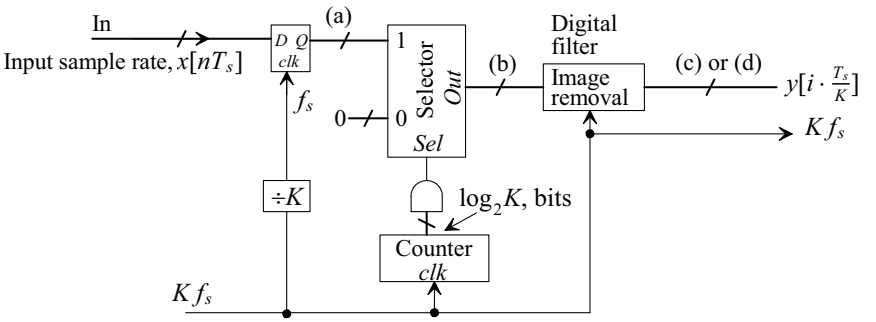

Figure 2.26 A zero-padding interpolation block, see spectrums in Fig. 2.27.

the word size and shift each nonzero sample towards the MSB by $\log_2 K$ (assuming K is a power of 2). For the present example we would shift the constant value of 1 to the left two places resulting in 4. When we average the 4 samples (4, 0, 0, 0) we get 1 (our original input). In the following, and in Fig. 2.26, we won't explicitly show the shifting in the input or output words to compensate for the signal reduction when using zero padding.

Returning to Fig. 2.26, we see that our input signal changes every T_s seconds and has the assumed spectrum seen in Fig. 2.27a (marked (a) in Fig. 2.26). A $\log_2 K$ size counter and AND gate are used to select the input signal one of K times so we get the zero padded waveform seen in Fig. 2.25b (spectrum shown in Fig. 2.27b). Note that the Nyquist frequency has moved from $f_s/2$ to $Kf_s/2$. The problem is that the images are still

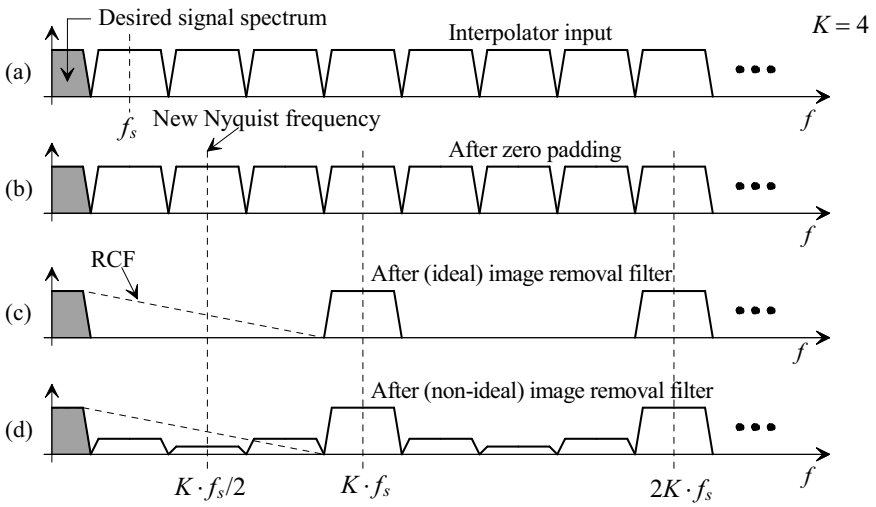

Figure 2.27 Example spectrums when zero padding interpolation is employed.

present in the waveform and thus need to be removed. This is the point of using the image removal filter seen in Fig. 2.26. Figure 2.27c shows the spectrum after increasing the sample rate and passing the signal through an ideal image removal filter. Also seen in this figure is the response of the RCF. It now starts rolling off at $f_s/2$ and can extend up to $Kf_s - f_s/2$. Note that the RCF's response seen in Fig. 2.27a must cut off abruptly at $f_s/2$. Finally, Fig. 2.27d shows the spectrums when a non-ideal digital image removal filter is used. The figure shows the nonzero spectral content remaining in the spectrum after filtering.

Hold Register

Figure 2.28 shows the block diagram of interpolation using an input hold register (which may simply be the input of a digital filter). The benefit of this topology is simplicity. We simply clock the input word K times faster into a register to increase the clocking frequency as seen in Fig. 2.25c. Note how the waveform seen in Fig. 2.25c looks similar to the output of the S/H discussed earlier in the chapter (so we should be expecting some sort of Sinc response effect on our input signal as seen in Eq. [2.16]).In order to quantify this last comment we can write the output of the hold register in terms of its input using

$$y_u\left[i \cdot \frac{T_s}{K}\right] = \sum_{i=K \cdot n}^{K \cdot (n+1)-1} \frac{1}{K} \cdot x\left[i \cdot \frac{T_s}{K}\right] = x[nT_s] \tag{2.30}$$

noting, $K \cdot n \le i \le K \cdot (n+1) - 1$, or

$$K \cdot y_u[nT_s] = x\left[Kn \cdot \frac{T_s}{K}\right] + x\left[(Kn+1)\frac{T_s}{K}\right] + x\left[(Kn+2)\frac{T_s}{K}\right] + \ldots + x\left[[K \cdot (n+1) - 1]\frac{T_s}{K}\right] \tag{2.31}$$

Writing the z-domain representation (using the input clock as the reference for the delays, or, $z = e^{j2\pi f \cdot T_s}$) of this equation gives

$$Y_u(z) \cdot z^n \cdot K = [1 + z^{1/K} + z^{2/K} + \ldots + z^{(K-1)/K}] \cdot z^n \cdot X(z) \tag{2.32}$$

or, where the z^n represents a shift in time of nT_s,

$$\frac{Y_u(z)}{X(z)} = \frac{1}{K} \cdot [1 + z^{1/K} + z^{2/K} + \ldots + z^{(K-1)/K}] \tag{2.33}$$

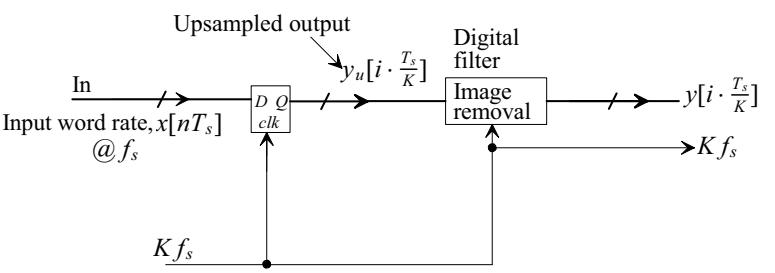

Figure 2.28 An interpolation block using a hold register, see spectrums in Fig. 2.32.

If we multiply the top and bottom of this equation by $1 - z^{1/K}$ we get

$$H_u(z) = \frac{Y_u(z)}{X(z)} = \frac{1}{K} \cdot \frac{1 - z}{1 - z^{1/K}} \tag{2.34}$$

or

$$H_u(f) = \frac{1}{K} \cdot \frac{1 - e^{j \cdot 2\pi \frac{f}{f_s}}}{1 - e^{j \cdot 2\pi \frac{f}{Kf_s}}} \tag{2.35}$$

Knowing $|1 - e^{jx}| = |(1 - \cos x) - j \sin x| = \sqrt{(1 - \cos x)^2 + (-\sin x)^2} = \sqrt{2(1 - \cos x)}$ and $1 - \cos x = 2 \sin^2 \frac{x}{2}$ we get

$$|H_u(f)| = \left| \frac{1}{K} \cdot \frac{1 - e^{j \cdot 2\pi \frac{f}{f_s}}}{1 - e^{j \cdot 2\pi \cdot \frac{f}{Kf_s}}} \right| = \frac{1}{K} \cdot \frac{\sqrt{2(1 - \cos 2\pi \cdot \frac{f}{f_s})}}{\sqrt{2(1 - \cos 2\pi \cdot \frac{f}{Kf_s})}} = \frac{1}{K} \cdot \left| \frac{\sin\left(\pi \cdot \frac{f}{f_s}\right)}{\sin\left(\pi \cdot \frac{f}{Kf_s}\right)} \right| \tag{2.36}$$

If we label the interpolator's output frequency $f_{s,new} = K \cdot f_s$ then

$$|H_u(f)| = \frac{1}{K} \cdot \left| \frac{\sin\left(\pi \cdot \frac{K \cdot f}{f_{s,new}}\right)}{\sin\left(\pi \cdot \frac{f}{f_{s,new}}\right)} \right| = \left| \frac{Sinc\left(\pi \frac{K \cdot f}{f_{s,new}}\right)}{Sinc\left(\pi \frac{f}{f_{s,new}}\right)} \right| \tag{2.37}$$

This equation is sketched in Fig. 2.29. This isn't exactly a Sinc response, Fig. 2.17, but a similar-shaped response. We'll find that this equation also comes up when discussing Sinc response digital filters so let's spend a moment characterizing it. The ratio of the main lobe to the first sidelobe can be determined by evaluating the response at $1.5f_{s,new}/K$ or

$$\left| \frac{\text{Main lobe}}{\text{First sidelobe}} \right| = K \cdot \sin\left(\frac{1.5\pi}{K}\right) \tag{2.38}$$

This equation is plotted in Fig. 2.30 for varying K. Note how the maximum amount of attenuation approaches 13.5 dB (the same as the Sinc response seen in Fig. 2.17).

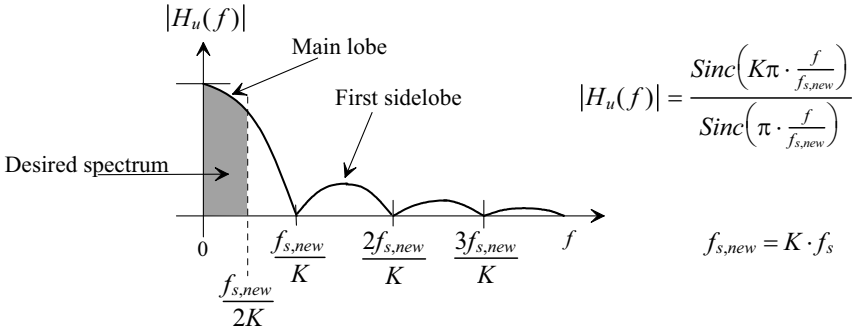

Figure 2.29 Frequency response interpolated data sees using a hold register.

It's also of interest to determine how much droop the filter will introduce into the signal frequencies of interest at the Nyquist frequency. Figure 2.31 shows the droop

(attenuation) at the maximum desirable input frequency of $f_s/2$ or $f_{s,new}/(2K)$. We can calculate the amount of droop, again using Eq. (2.37) when $f = f_{s,new}/(2K)$, as

$$\text{Droop} = \frac{1}{K \cdot \sin\left(\frac{\pi}{2K}\right)} \tag{2.39}$$

This equation is plotted in Fig. 2.31. Note that as K gets large the amount of droop approaches 3.9 dB (= 0.64) or the same as the Sinc response seen in Fig. 2.17.

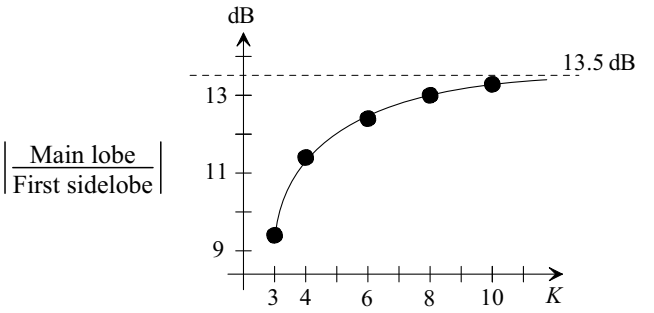

Figure 2.30 Attenuation versus K.

Figure 2.32 shows some example spectrums when $K = 4$ and using an input hold register for interpolation. In (a) we see a representative input spectrum that repeats every f_s. In (b) the input is upsampled to a clocking rate of $K \cdot f_s$. The effects of the input holding register's Sinc response are seen. At this point we have distorted our desired information with the drooping response seen in Fig. 2.31. In (c) the signal's spectrum, after passing through an ideal image removal filter to remove the undesired frequency components, is seen (see also Fig. 2.28). The RCF can have a slow roll-off ultimately passing negligible content at frequencies above $K \cdot f_s - f_s/2$ where the image around the new clocking frequency, $K \cdot f_s$, exists. Finally, in (d) we show what the spectrums may look like with a non-ideal image removal filter. The design of the RCF depends on the allowed amount of unwanted spectral content that can be tolerated in the final output spectrum.

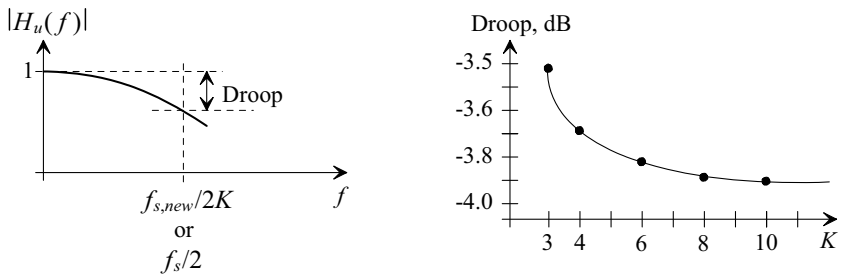

Figure 2.31 Droop at edge of signal bandwidth.

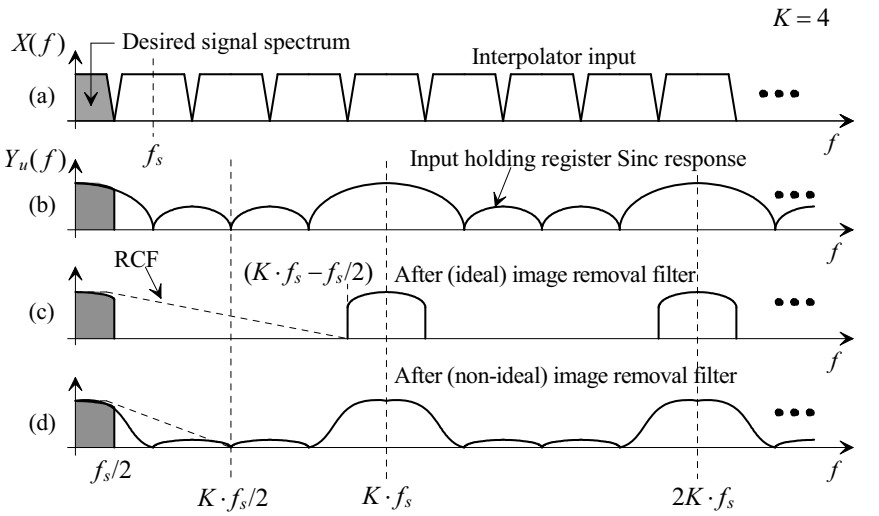

Figure 2.32 Example spectrums when interpolation using a hold register is employed.

Linear Interpolation

The final interpolation scheme we'll look at is linear interpolation, adding samples in between the interpolator's inputs that linearly change with time, Figs. 2.25 and 2.33. We can describe linear interpolation mathematically using

$$y_u\left[(i+1)\cdot\frac{T_s}{K}\right] = y_u\left[i\cdot\frac{T_s}{K}\right] + \frac{x[(n+1)T_s] - x[n\cdot T_s]}{K} \tag{2.40}$$

where $K\cdot n \le i < K\cdot(n+1)$. Note that when $i = K\cdot n$, $y_u\left[i\cdot\frac{T_s}{K}\right] = x[nT_s] = y_u[nT_s]$. Writing this equation in the z-domain we get

$$Y_u(z)\cdot z^{n+1/K} = z^n\cdot\left[Y_u(z) + \frac{X(z)\cdot z - X(z)}{K}\right] \tag{2.41}$$

$$\frac{Y_u(z)}{X(z)} = \frac{1}{K}\cdot\frac{1-z}{1-z^{1/K}} \tag{2.42}$$

which is the same as Eq. (2.34). After reviewing Fig. 2.25 we might have expected linear interpolation to introduce less distortion into the input signal than an interpolator made

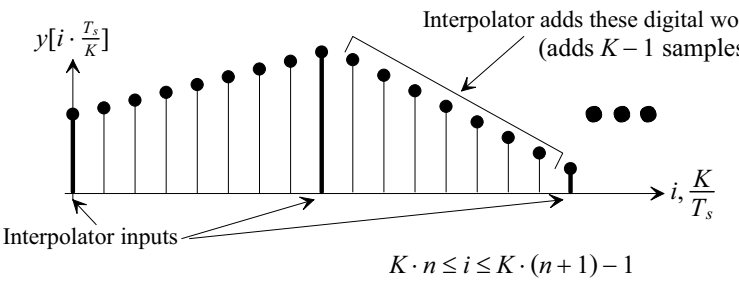

Figure 2.33 Using linear interpolation.

using a hold register. However, the fact that the output of an interpolator made using a hold register sees abrupt changes or steps over time (indicating higher spectral content) results in the equivalence in both interpolator's spectral responses. Note that this type of interpolator is more commonly found in analog signal processing using discrete-time analog circuits.

2.1.6 *K*-Path Sampling

In the last section discussing interpolation (upsampling our signal or increasing the clock rate) the input clock rate was f_s and the output clock rate was Kf_s. If we define z in terms of the *input clock*, $z \equiv e^{j2\pi \cdot \frac{f}{f_s}}$, then a delay on the output of the interpolator is written as $z^{-1/K} = e^{-j2\pi f \cdot \frac{T_s}{K}}$ and a delay on the input of the interpolator is written as z^{-1}. If, on the other hand, we define z in terms of the *output clock*, $z \equiv e^{j2\pi \cdot \frac{f}{Kfs}}$ then a delay on the output is written z^{-1} while a delay on the input of the interpolator is written as z^{-K}. In simpler terms, a delay on the input lasts T_s seconds while a delay on the output lasts T_s/K seconds. In analog signal processing we can get the same type of behavior, an increase in the output clock frequency (or upsampling the input signal) by using more than one path.

In order to understand this last statement, consider the parallel paths of S/Hs seen in Fig. 2.34. Each S/H is clocked on an opposite phase of an input clock. The resistors are used to sum the outputs of the S/Hs. If the input clock is f_s, then the output signal will change every $T_s/2$ seconds or at a rate of $2f_s$ Hz. By using two-paths we effectively realize an interpolation rate, K, of 2. In other words, we can think of the two-path S/H topology as a single path topology clocked at $2f_s$ Hz. For K paths we can write, again,

$$f_{s,new} = K \cdot f_s \tag{2.43}$$

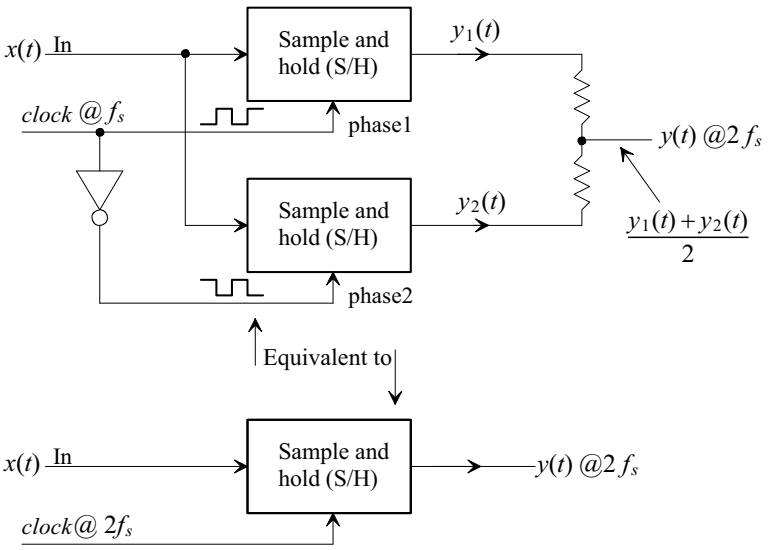

Figure 2.34 Using two S/H paths.

Switched-Capacitor Circuits

Let's show how to apply *K*-path design to switched-capacitor circuits (commonly used for analog signal processing). Examine the switched-capacitor circuit seen in Fig. 2.35. A switch is closed when a non-overlapping clock (meaning that the clock signals are never high at the same time) signal is high. When the ϕ_1 switch opens at $(n-1/2)T_s$ the charge on the capacitor is

$$Q_1 = v_{in}[(n-1/2)T_s] \cdot C_I \tag{2.44}$$

and when the ϕ_2 switch opens at nT_s the charge on the capacitor is

$$Q_2 = v_{out}[nT_s] \cdot (C_I + C_F) = v_{in}[(n-1/2)T_s] \cdot C_I + v_{out}[(n-1)T_s] \cdot C_F \tag{2.45}$$

Writing this equation in the *z*-domain we get

$$v_{out}(z) \cdot (C_I + C_F) = v_{in}(z) \cdot z^{-1/2} \cdot C_I + v_{out}(z) \cdot z^{-1} \cdot C_F \tag{2.46}$$

or

$$\frac{v_{out}(z)}{v_{in}(z)} = \frac{C_I \cdot z^{-1/2}}{C_I + C_F - C_F \cdot z^{-1}} \tag{2.47}$$

If we input a DC voltage, $f = 0$ or $z = 1$, then the output is equal to the input (the magnitude of Eq. (2.47) is one). This circuit behaves, for input frequencies $<< f_s$ like a simple RC circuit (as seen in Fig. 2.35). To prove this let's write

$$z = e^{j2\pi f/f_s} \approx 1 + j2\pi\frac{f}{f_s} = 1 + \frac{s}{f_s} \text{ for } f << f_s \tag{2.48}$$

and, knowing the $z^{-1/2}$ term in the numerator is simply a phase shift of one-half clock cycle (which is negligible for input frequencies $<< f_s$),

$$\left|\frac{v_{out}(f)}{v_{in}(f)}\right| = \left|\frac{\frac{C_I}{C_F}}{\frac{C_I}{C_F} + 1 - \left(1 - j2\pi\frac{f}{f_s}\right)}\right| \tag{2.49}$$

or

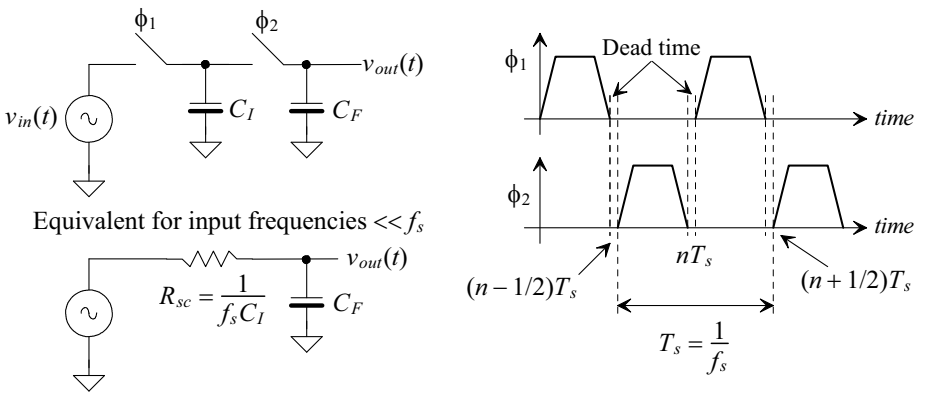

Figure 2.35 Switched-capacitor lowpass filter.

$$\left|\frac{v_{out}(f)}{v_{in}(f)}\right| = \left|\frac{1}{1+j2\pi C_F \frac{f}{C_I \cdot f_s}}\right| = \frac{1}{\sqrt{1+(2\pi f \cdot R_{sc} C_F)^2}} \tag{2.50}$$

where we've defined

$$R_{sc} = \frac{1}{f_s C_I} = \frac{T_s}{C_I} \tag{2.51}$$

We can also write the exact frequency response, Eq. (2.47), of this switched-capacitor circuit

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{\frac{C_I}{C_F} \cdot e^{-j2\pi f/2f_s}}{\frac{C_I}{C_F} + 1 - e^{-j2\pi f/f_s}} = \frac{\frac{C_I}{C_F} \cdot e^{-j2\pi f/2f_s}}{\left(\frac{C_I}{C_F} + 1 - \cos 2\pi f/f_s\right) + j(-\sin 2\pi f/f_s)} \tag{2.52}$$

or

$$\left|\frac{v_{out}(f)}{v_{in}(f)}\right| = \frac{\frac{C_I}{C_F}}{\sqrt{\left(\frac{C_I}{C_F} + 1 - \cos 2\pi f/f_s\right)^2 + \left(\sin^2 2\pi f/f_s\right)}} \tag{2.53}$$

Note that for $f << f_s$ the cosine terms is approximately one and the sine term is approximately $2\pi f/f_s$ so this equation simplifies to Eq. (2.50).

Next let's examine the two-path version of Fig. 2.35 shown in Fig. 2.36. The effect of using two paths is to double the output sampling rate, $f_{s,new} = 2f_s$. Using Eq. (2.47) we can write

$$H_{1-path}(z) = \frac{C_I \cdot z^{-1/2}}{C_I + C_F - C_F \cdot z^{-1}} \tag{2.54}$$

At the new sampling rate we can write

$$H_{2-path}(z) = \frac{C_I \cdot z^{-1}}{C_I + C_F - C_F \cdot z^{-2}} \tag{2.55}$$

or, in generic terms of *K*, replace *z* in the transfer function of the single-path topology with z^K to get the transfer function in the *K*-path topology,

$$z \rightarrow z^K \tag{2.56}$$

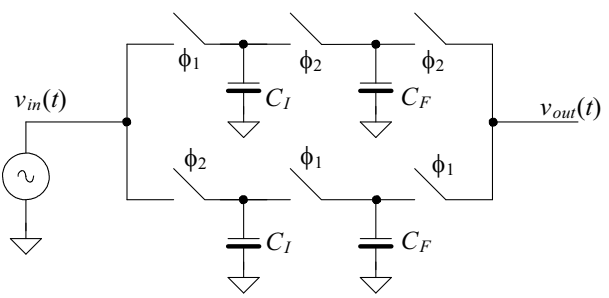

Figure 2.36 Switched-capacitor 2-path lowpass filter.

Figure 2.37 shows *K*-paths and the equivalent single path topology, a time interleaved topology. Note that at this point there are several important topics we can discuss including path matching and the effects of clock jitter (more later).

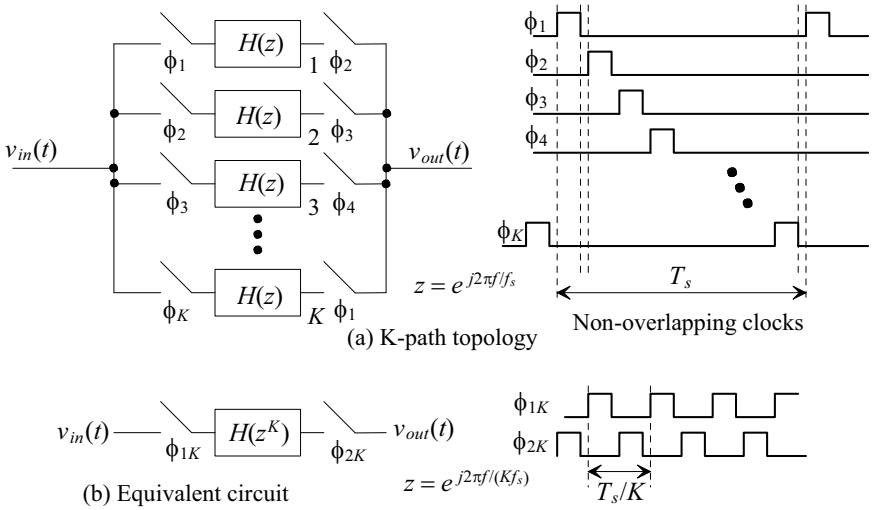

Figure 2.37 A K-path topology and its equivalent circuit.

Non-Overlapping Clock Generation

Figure 2.38 shows a circuit useful for generating four-phase, non-overlapping, clock signals. A shift register is preset so that only one bit is high. The logic block seen in the figure is used to detect if more than one output is high. Note the clear and set inputs of the flip-flops. The amount of non-overlap, or dead time, between pulses is set by the delay through the two inverters connected to the outputs of the NAND gates.

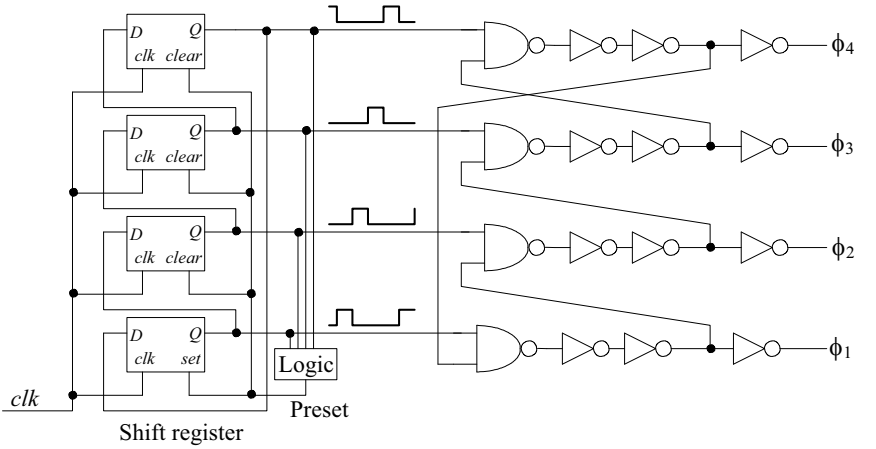

Figure 2.38 Generating a four-phase non-overlapping clock signal.

2.2 Circuits

In this section we discuss the implementation of the S/H and discrete analog integrators (DAIs). The focus is on developing equations and block diagrams for the circuits that will be useful as building blocks in the coming chapters. It's assumed, in this section, that the reader is familiar with the bottom-plate sampling technique seen in Fig. 2.20 and the associated discussion.

2.2.1 Implementing the S/H

A fully-differential mixed-signal S/H based on the topology seen in Fig. 2.20 is seen below in Fig. 2.39. The sample portion of the S/H occurs when the ϕ_1 and ϕ_2 switches are closed and the ϕ_3 switches are open. When the ϕ_3 switches are closed the ϕ_1 and ϕ_2 switches open and the value of the input signal at this instance is "held" until the next time the ϕ_3 switches are closed.

We can determine the relationship between the input of the S/H and its output by writing the charge stored on C_F when the ϕ_1 and ϕ_2 switches are closed (the ϕ_3 switches are open) as

$$Q_F^{\phi_1} = C_F \cdot (v_{in} - V_{CM} \pm V_{OS}) \tag{2.57}$$

where V_{OS} is the offset voltage of the op-amp. When the op-amp is in the follower configuration, the ϕ_1 switches are closed, and the input/output voltages of the op-amp go to $V_{CM} \pm V_{OS}$ (assuming infinite op-amp gain). When the ϕ_3 switches close we can write

$$Q_F^{\phi_3} = C_F \cdot (v_{out} - V_{CM} \pm V_{OS}) \tag{2.58}$$

Since charge must be conserved, $v_{out} = v_{in}$. The input is sampled on the falling edge of ϕ_1.

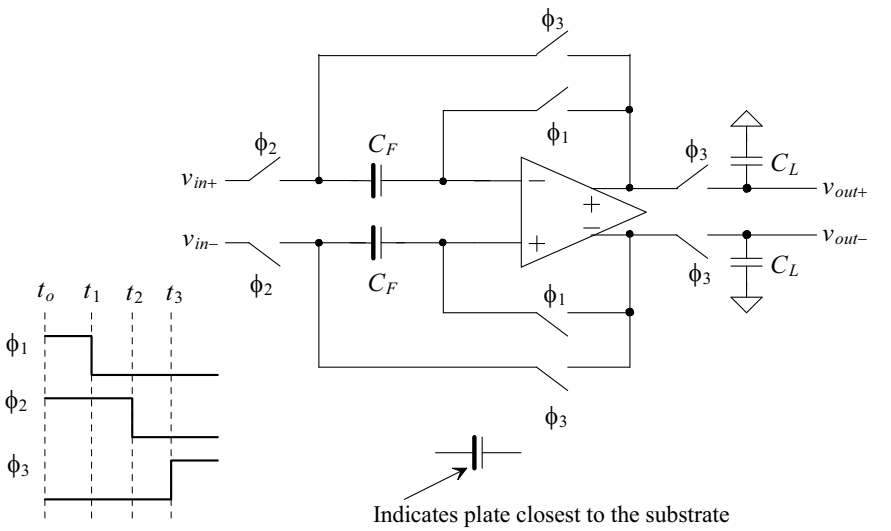

Figure 2.39 Fully-differential S/H differential topology.

Example 2.3
Simulate the operation of the S/H building block seen in Fig. 2.39 assuming C_F = 1 pF and f_s = 100 MHz. Show that the sampled signal isn't affected by the matching of the two capacitors in the S/H or by an op-amp offset.

The simulation results are shown in Fig. 2.40. In part (a) the clock signals are shown. Note the non-overlap time. Unlike the clock signals shown in Fig. 2.39 where the falling edge of ϕ_2 is delayed from ϕ_1, the simulation sets the signals so they go low at the same time. This was to avoid the outputs of the op-amp changing to very large values for the small amount of time the ideal op-amp operates open-loop with an input signal applied.

In part (b) we show the op-amp outputs. Note how, when ϕ_1 goes high, both outputs are set to the common-mode voltage by forcing the op-amp into a follower configuration (which may lead us to use switches to short the terminals of the op-amp to V_{CM} when ϕ_1 is high if offset isn't important, more on this in a moment). When ϕ_3 goes high, the circuit behaves as an S/H. Part (c) of the figure shows the outputs connected through ϕ_3 switches, as seen in Fig. 2.39, driving 10 pF load capacitances.

Introducing a 100% mismatch in the two capacitors by changing one of the values of C_F from 1 pF to 2 pF doesn't affect the simulation results seen in Fig. 2.40. Also, an unrealistically large op-amp offset of 100 mV doesn't affect the S/H's operation. ■

Finite Op-Amp Gain-Bandwidth Product

The previous derivations assumed the op-amp had infinite gain so the one op-amp input was driven to precisely $V_{CM} + V_{OS}$ while the other op-amp input was held at $V_{CM} - V_{OS}$. Op-amp open-loop gain is an important parameter when designing a S/H. Let's write the open-loop gain of an op-amp, assuming a dominant pole, as

$$A_{OL}(f) = \frac{A_{OLDC}}{1 + j \cdot \frac{f}{f_{3dB}}} = \frac{v_{out+} - v_{out-}}{v_{in+} - v_{in-}} \tag{2.59}$$

In nanometer CMOS the DC gain, A_{OLDC}, may be 500 while the f_{3dB} may be 100 kHz giving a gain-bandwidth product, or unity-gain frequency, of 50 MHz.

The S/H is an example of a feedback system that can be characterized using the classic feedback equation

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} \tag{2.60}$$

Since, during the hold operation, all of output signal is fed back to the input $\beta = 1$ and we can write, for DC,

$$A_{CL} = \frac{A_{OLDC}}{1 + A_{OLDC}} \tag{2.61}$$

As the op-amp's open-loop gain becomes very large the S/H's gain moves towards 1. Note that the closed-loop gain will always be less than the desired value. If, in a mixed-signal

circuit, *VDD* is 1-V and a S/H with a resolution better than 1 mV is required, then the open-loop gain of the op-amp can be estimated using

$$\frac{VDD - \text{Resolution}}{VDD} = \frac{1 - 0.001}{1} < \frac{A_{OLDC}}{1 + A_{OLDC}} \tag{2.62}$$

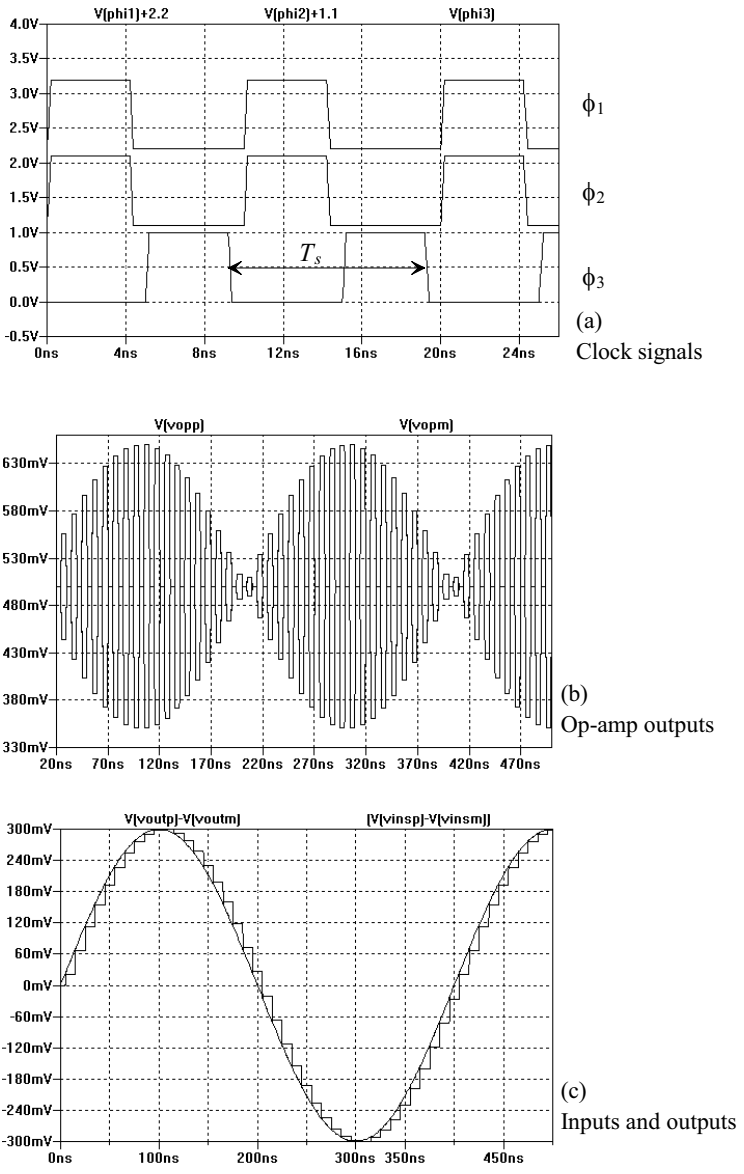

Figure 2.40 SPICE simulations of the operation of the S/H in Fig. 2.39

or $A_{OLDC} > 1,000$. We can write this equation in a more useful form as

$$A_{OLDC} > \frac{VDD}{\text{Resolution}} \tag{2.63}$$

We can estimate the required op-amp gain-bandwidth product (unity-gain frequency f_{un}) $A_{OLDC}f_{3dB}$, for a S/H by substituting Eq. (2.59) into Eq. (2.60) with $\beta = 1$ (noting that this assumes the op-amp doesn't experience slew-rate limitations and its response is first-order)

$$A_{CL} = \frac{A_{OLDC}}{1 + j \cdot \frac{f}{f_{3dB}} + A_{OLDC}} \tag{2.64}$$

or

$$A_{CL} \approx \frac{1}{1 + j \cdot \frac{f}{A_{OLDC} \cdot f_{3dB}}} = \frac{1}{1 + j \cdot \frac{f}{f_{un}}} \tag{2.65}$$

This first-order system has a time-domain response given by

$$v_{out} = v_{in}(1 - e^{-t \cdot 2\pi \cdot f_{un}}) \tag{2.66}$$

For a given resolution we can write

$$\text{Resolution} = 1 - \frac{v_{out}}{v_{in}} = e^{-t \cdot 2\pi \cdot f_{un}} \tag{2.67}$$

If the settling time must be faster than half of the sampling clock period T_s (=$1/f_s$), as seen in Fig. 2.40 during ϕ_3, then we can write

$$t_{settling} < \frac{1}{2f_s} = \frac{T_s}{2} \tag{2.68}$$

The minimum gain-bandwidth product of an op-amp used in a S/H is determined using

$$f_{un} = A_{OLDC} \cdot f_{3dB} > \frac{-f_s \cdot \ln(\text{Resolution})}{\pi} \tag{2.69}$$

If the *VDD* in a mixed-signal system is 1-V, the desired resolution of the S/H is 1 mV, and the sampling frequency is 100 MHz then the unity-gain frequency, f_{un}, must be greater than 210 MHz. If the required DC gain, from Eq. (2.63), is 1,000, then the f_{3dB} of the op-amp is 210 kHz. Of course, the actual DC gain and f_{un} should be much higher than these minimums.

Autozeroing

A single-ended version of the S/H in Fig. 2.39 is seen in Fig. 2.41 including the input referred noise, $V^2_{inoise}(f)$, power spectral density (PSD with units of V^2/Hz) and op-amp offset voltage. We'll represent the input-referred noise in the time-domain using $v_{inoise}(t)$. We've already shown in Ex. 2.3, Eqs. (2.57), and (2.58) that this topology "autozeroes" or removes the offset voltage. When the ϕ_1 switches are closed the op-amp is in the unity-follower configuration and its inputs move to $V_{CM} + V_{OS} + v_{inoise}(t)$. When the ϕ_3 switches close the voltage on the inputs of the op-amp is $V_{CM} + V_{OS} + v_{inoise}(t_3)$. Using Eq. (2.57) we can write, assuming $t_1 \approx t_3$,

$$Q_F^{\phi_1} = C_F \cdot (v_{in}(t_3) - V_{CM} - V_{OS} - v_{inoise}(t_3)) \tag{2.70}$$

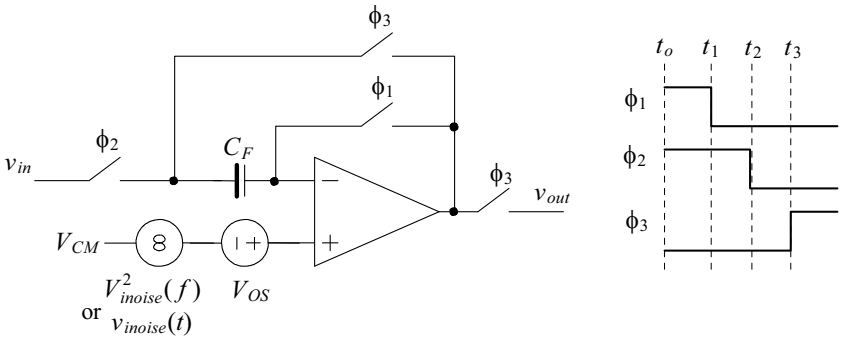

Figure 2.41 S/H with input-referred offset and noise shown.

At a time $T_s/2$ later, the ϕ_3 switches open and the ϕ_1 switches close again to sample the input signal and the noise. Writing the charge on C_F between t_3 and $t_3 + T_s/2$

$$Q_F^{\phi_3} = C_F \cdot (v_{out}(t) - V_{CM} - V_{OS} - v_{inoise}(t)) \tag{2.71}$$

Qualitatively, we can see that if the noise is moving slowly (e.g., Flicker noise) it is removed from the output signal. However, fast moving noise isn't subtracted out during the autozero process. Ultimately the bandwidth of the circuit (say switch resistances and capacitors) and op-amp finite bandwidth limit the frequency content of the noise.

To get a quantitative idea for how the autozero process affects noise in the S/H's output signal we can write

$$v_{out}(t) = v_{in}(t_3) + v_{inoise}(t) - v_{inoise}(t_3) \quad \text{for } t_3 \le t \le t_3 + T_s/2 \tag{2.72}$$

Focusing on the noise and taking the Fourier Transform of each side of this equation gives

$$V_{onoise}(f) = V_{inoise}(f) \cdot e^{-j2\pi f \cdot t_3}(e^{-j2\pi f \cdot (t - t_3)} - 1) \tag{2.73}$$

Note that when t is close to t_3 the output has little noise. The worst case situation is right before the ϕ_3 switches open at a time $t_3 + T_s/2$ (the ϕ_3 switches are on for $T_s/2$ seconds). If we look at this worst-case situation only, then

$$\left| \frac{V_{onoise}}{V_{inoise}} \right| = \left| e^{-j\pi f \cdot T_s} - 1 \right| \tag{2.74}$$

which is the transfer function of a differentiator, Sec. 1.2.2. Note how it would be straightforward to extend this derivation to any arbitrary time that the ϕ_3 switches are on. Borrowing the results seen in Eq. (1.46) we get a noise transfer function, *NTF*, of

$$NTF = \left| \frac{V_{onoise}}{V_{inoise}} \right| = 2 \cdot \left| \sin \frac{\pi}{2} \cdot f \cdot T_s \right| \tag{2.75}$$

This equation is plotted in Fig. 2.42 along with the response of the S/H. Note that at DC (where the op-amp's offset voltage is located) the output of the S/H is noise free. As alluded to earlier, autozeroing works well for reducing the effects of Flicker noise (a low frequency noise that is common in CMOS integrated circuits).

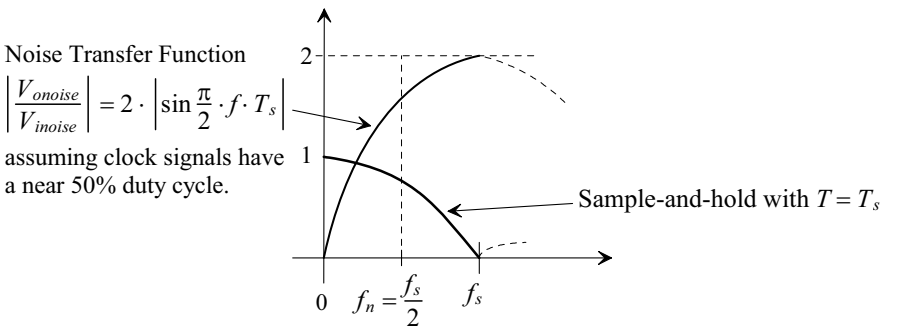

Figure 2.42 The noise transfer function of a S/H.

In the preceding discussion we didn't include the effects of sampling on the output noise spectrum. However, at this point, replicating the noise spectrum at multiples of f_s and weighting the output noise by the S/H response should be straightforward, Fig. 2.43. Having said this, however, note that if our op-amp's input-referred noise PSD isn't bandlimited to the Nyquist frequency, $f_s/2$, as it is in Fig. 2.43 then noise will alias into DC to $f_s/2$ range (the desired range).

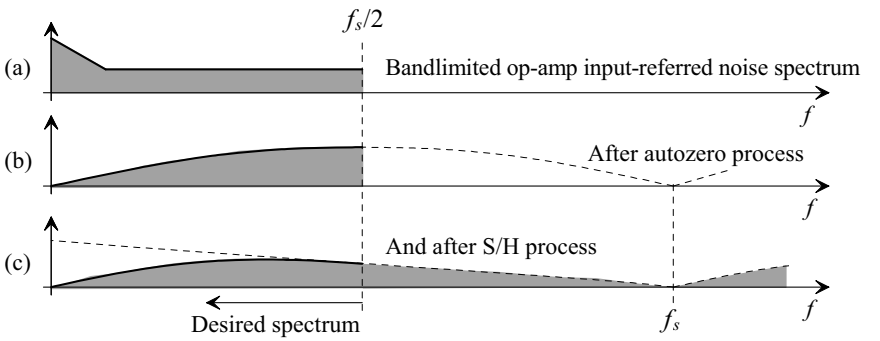

Figure 2.43 Example spectrums when S/H in Fig. 2.39 is used.

Correlated Double Sampling (CDS)

Correlated Double Sampling (CDS) is a name used for describing the autozero process followed by a S/H. The S/H in Fig. 2.39 thus employs CDS. Both the input signal and the noise/offset are sampled (double sample). Then the offset/noise is subtracted from the output signal (the correlation) to give an output signal with less noise and ideally no offset.

As an example of CDS, Fig. 2.44 shows an input-referred noise signal and offset along with a S/H input and output. The op-amp's input referred offset is about −220 mV and the input-referred noise has a peak-to-peak variation of about 80 mV. (Remember offset and noise are always measured on the output of a circuit and referred back to its input.) While we can see noise in the S/H's output it is clear that it has been reduced.

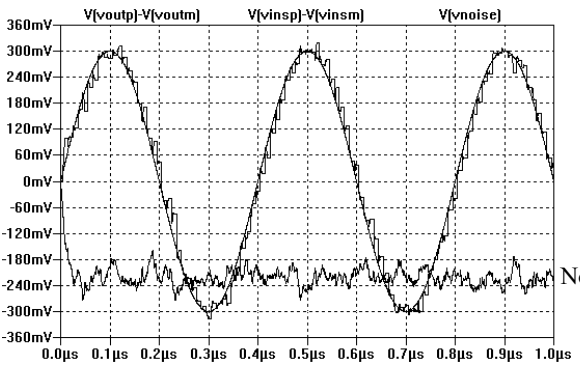

Figure 2.44 Showing how CDS reduces noise and offset in the S/H in Fig. 2.39.

Figure 2.45 shows a S/H that doesn't employ CDS. This topology is used to help ensure the CMFB circuits and biasing in the op-amp are more tolerant to offsets. When the ϕ_1 switches are on, the inputs of the op-amp are shorted to the common-mode voltage, V_{CM}, and the outputs are shorted together. Note that the op-amp settling time isn't a factor in the design during this hold portion of the S/H process. At this point in time we can write

$$Q_F^{\phi_1} = C_F \cdot (v_{in} - V_{CM}) \tag{2.76}$$

When the ϕ_3 switches turn on, the op-amp moves into the follower configuration and the op-amp inputs move to $V_{CM} \pm V_{OS}$. During this time we can write, see Eq. (2.58),

$$Q_F^{\phi_3} = C_F \cdot (v_{out} - V_{CM} \pm V_{OS}) \tag{2.77}$$

Since charge must be conserved

$$v_{out} = v_{in} \pm V_{OS} \tag{2.78}$$

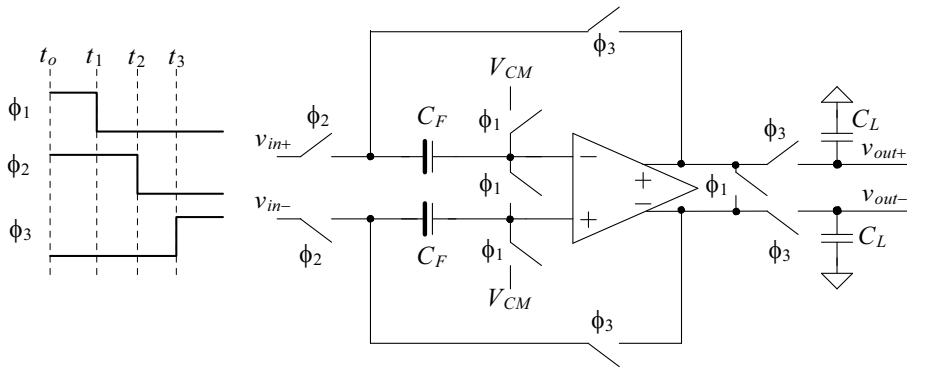

Figure 2.45 Fully-differential S/H differential topology without using CDS.

So why would we use this configuration? Neither the offset or noise would be reduced which is a significant disadvantage over the topology in Fig. 2.39. The answer is that since the inputs of the op-amp are driven to a known voltage (V_{CM}) and the outputs are driven to a known voltage via the op-amp's common-mode feedback circuit (again V_{CM}) ensuring good biasing and stable CMFB loops in the op-amp are easier to attain. Note that in a two-stage op-amp design we would also short the outputs of the first-stage diff-amp together so the inputs of output buffer are forced to a known value (the ideal output voltage of the diff-amp). Design of fully-differential op-amps is discussed in detail, as is our next topic, in the book *CMOS Circuit Design, Layout, and Simulation*.

Selecting Capacitor Sizes

The selection of the capacitor sizes in the S/H is based on thermal noise considerations, *kT*/*C* (kay tee over cee), and settling time. Small capacitors result in lower power circuits and faster settling times but, at the same time, increase the thermal noise floor. For a detailed discussion of *kT*/*C* noise, as well as other circuit noise topics, see *CMOS Circuit Design Layout, and Simulation*. Table 2.1 shows the relationship between various capacitor sizes and corresponding thermal noise for quick reference.

Table 2.1 Capacitor size and corresponding *kT*/*C* noise at 300 °K.

Capacitor size, pF	$\sqrt{kT/C}$, μV RMS	$\sqrt{kT/C}$, mV peak-to-peak
0.01	640	3.84
0.1	200	1.2
1	64	0.384
10	20	0.12
100	6.4	0.038

2.2.2 The S/H with Gain

Figure 2.46 shows a S/H with gain. Following the derivations from the last section we can write

$$Q_{I,F}^{\phi_1} = C_I \cdot (v_{in} - V_{CM} \pm V_{OS}) + C_F \cdot (v_{in} - V_{CM} \pm V_{OS}) \tag{2.79}$$

and when the ϕ_3 switches turn on

$$Q_I^{\phi_3} = C_I \cdot (V_{CM} - V_{CM} \pm V_{OS}) \tag{2.80}$$

and

$$Q_F^{\phi_3} = C_F \cdot (v_{out} - V_{CM} \pm V_{OS}) \tag{2.81}$$

Knowing charge must be conserved

$$Q_F^{\phi_3} = C_F \cdot (v_{out} - V_{CM} \pm V_{OS}) =$$

$$= \overbrace{C_F \cdot (v_{in} - V_{CM} \pm V_{OS})}^{Q_F^{\phi_1}} + \overbrace{C_I \cdot (v_{in} - V_{CM} \pm V_{OS})}^{Q_I^{\phi_1}} - \overbrace{C_I \cdot (V_{CM} - V_{CM} \pm V_{OS})}^{Q_I^{\phi_3}} \tag{2.82}$$

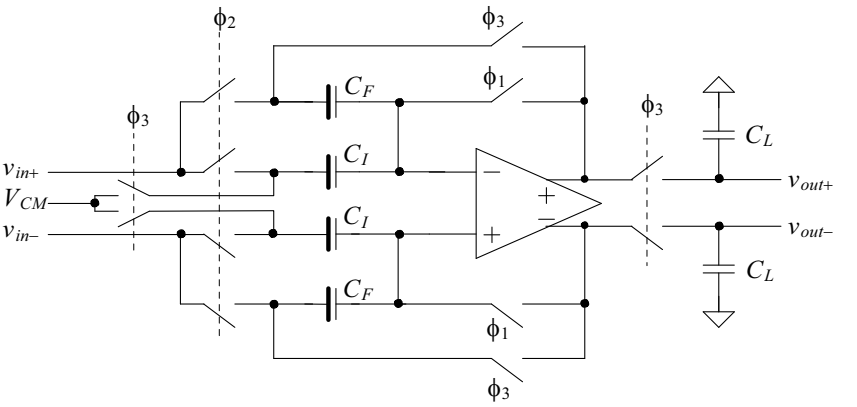

Figure 2.46 A S/H with gain.

or

$$v_{out} = \left(1 + \frac{C_I}{C_F}\right) \cdot v_{in} - \frac{C_I}{C_F} \cdot V_{CM} \tag{2.83}$$

For a fully-differential topology the last term is common to both the inverting and non-inverting inputs of the S/H so we can write

$$v_{out+} - v_{out-} = \left(1 + \frac{C_I}{C_F}\right) \cdot (v_{in+} - v_{in-}) \tag{2.84}$$

A block diagram for the S/H in Fig. 2.46 is shown in Fig. 2.47. Note that this op-amp topology employs CDS. Also note, though we didn't derive it in the last section (because it ends up being negligible in most circuits), the residual offset after autozeroing is V_{OS}/A_{OLDC}. An op-amp DC gain of 1,000 and an op-amp offset of 50 mV results in a 50 μV residual offset when employing CDS.

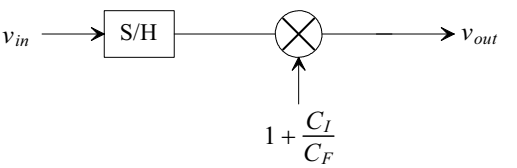

Figure 2.47 Block diagram for the S/H of Fig. 2.46.

Example 2.4
Simulate the operation of the data converter S/H building block shown in Fig. 2.46. Assume $C_I = C_F = 1$ pF and $f_s = 100$ MHz.

The simulation results are shown in Fig. 2.48. The gain, as we would expect, is 2. It may be useful at this point to simulate this circuit with an offset or noise like we did in Ex. 2.3. ■

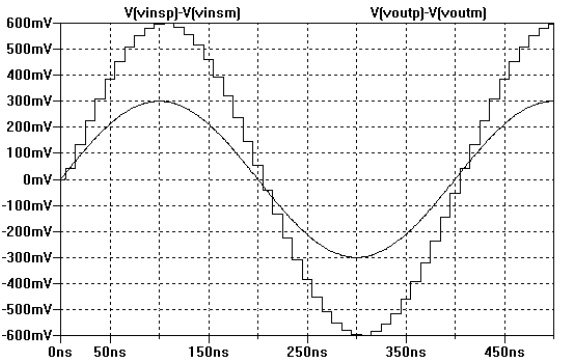

Figure 2.48 Simulating the S/H seen in Fig. 2.46 with a gain of 2.

Implementing Subtraction in the S/H

We'll see later, when covering Nyquist-rate data converters, that it is useful to implement subtraction in the S/H. Consider what would happen if instead of connecting the bottom plates of the C_I capacitors in Fig. 2.46 to V_{CM} we connect them to V_{CI+} and V_{CI-} (see Fig. 2.49). Doing this results in

$$Q_I^{\phi_3} = C_I \cdot (V_{CI+} - V_{CM} \pm V_{OS}) \tag{2.85}$$

or, after reviewing Eqs. (2.82) - (2.83)

$$v_{out+} = \left(1 + \frac{C_I}{C_F}\right) \cdot v_{in+} - \frac{C_I}{C_F} \cdot V_{CI+} \tag{2.86}$$

The differential output voltage is then given by

$$v_{out} = v_{out+} - v_{out-} = \left(1 + \frac{C_I}{C_F}\right) \cdot (v_{in+} - v_{in-}) - \frac{C_I}{C_F} \cdot (V_{CI+} - V_{CI-}) \tag{2.87}$$

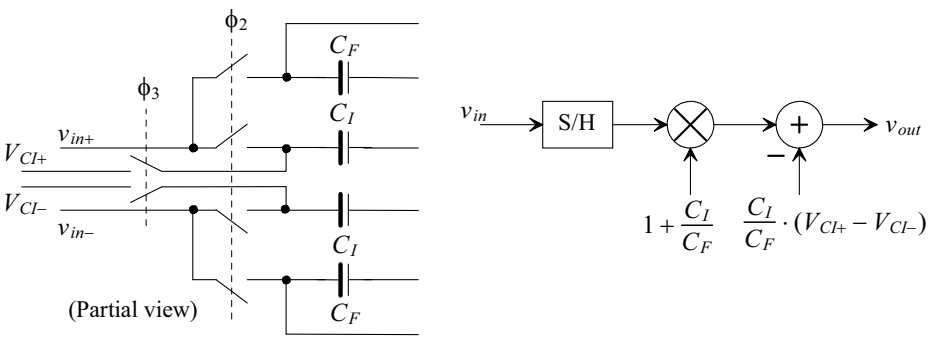

Figure 2.49 Implementing subtraction in the S/H.

Rearranging the block diagram seen in Fig. 2.49 results in the topology seen in Fig. 2.50.

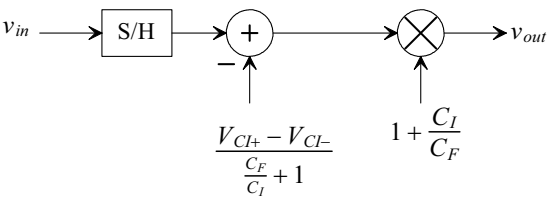

Figure 2.50 Block diagram of Fig. 2.49 with bottom plates of C_I tied to V_{CI}.

Example 2.5

Simulate the operation of the S/H shown in Fig. 2.51 if f_s = 100 MHz, $C_F = C_I$ = 1 pF, V_{CI+} = 1.5V_{CM}, and V_{CI-} is 0.5V_{CM} (V_{CM}= 500 mV). Comment on the resulting output.

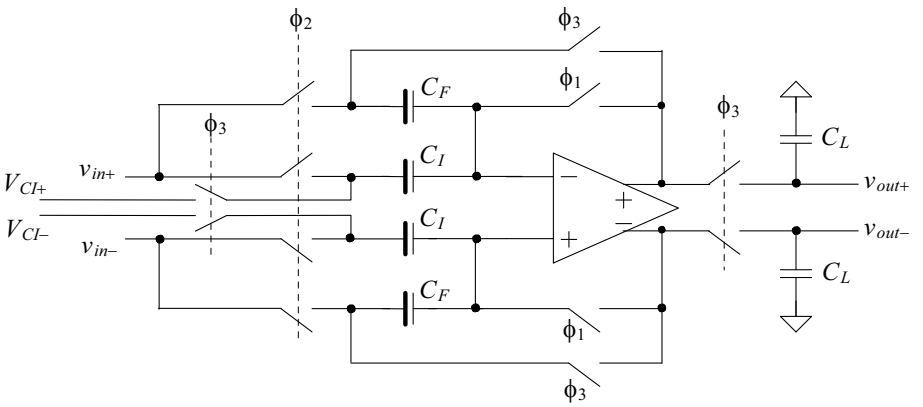

Figure 2.51 S/H used in Ex. 2.5.

The simulation results are shown in Fig. 2.52. We only show the situation when we would want to subtract V_{CM}/2 from the differential input signal. The inputs are fully-differential, swinging around the common-mode voltage of 500 mV with an amplitude of 100 mV (so they swing between 600 mV and 400 mV). The largest differential voltage is 600 mV – 400 mV or +200 mV while the smallest differential signal is 400 mV – 600 mV or –200 mV (so the differential signal swings around ground with an amplitude of 200 mV). Reviewing the block diagram in Fig. 2.50 with the values in this problem shows that the circuit takes this input signal, sample-and-holds it, subtract V_{CM}/2 (250 mV) then multiplies it by 2. We've scaled the output in Fig. 2.52 to show that this sequence of events is indeed what is happening. Note that if we were to switch V_{CI+} and V_{CI-} we would add V_{CM}/2 to the input signal. ■

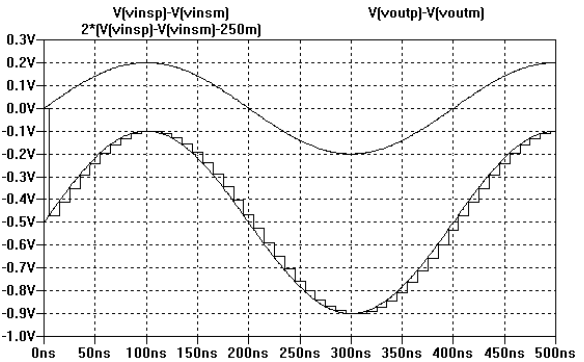

Figure 2.52 Simulation results for Ex. 2.5.

A Single-Ended to Differential Output S/H

Many input signals are single-ended, meaning the (one) input signal swings around V_{CM}. It is desirable in the first stage of the mixed-signal circuit to S/H the signal and then to change it into a fully-differential signal for further processing. A good single-to-differential converter will hold the op-amp's input common-mode voltage at V_{CM} for low distortion (important). In order to meet this goal consider the modified, from Fig. 2.46, S/H seen in Fig. 2.53. Again, we can write, (noting the C_F capacitors are discharged when the ϕ_1 switches are on)

$$Q_{I,F,total}^{\phi_1} = C_{I+} \cdot (v_{in} - V_{CM} \pm V_{OS}) + C_{I-} \cdot (V_{CM} - V_{CM} \pm V_{OS}) \tag{2.88}$$

When the ϕ_3 switches turn on the charge on these two input capacitors is

$$Q_I^{\phi_3} = 2C_I \cdot \left(\frac{v_{in}}{2} - V_{CM} \pm V_{OS} \right) \tag{2.89}$$

noting that the charge on the C_I capacitors (half of Eq. [2.89]) redistributes through the C_F capacitors. The charge on the feedback capacitors is then

$$Q_F^{\phi_3} = 2C_F \cdot (v_{out} - V_{CM} \pm V_{OS}) \tag{2.90}$$

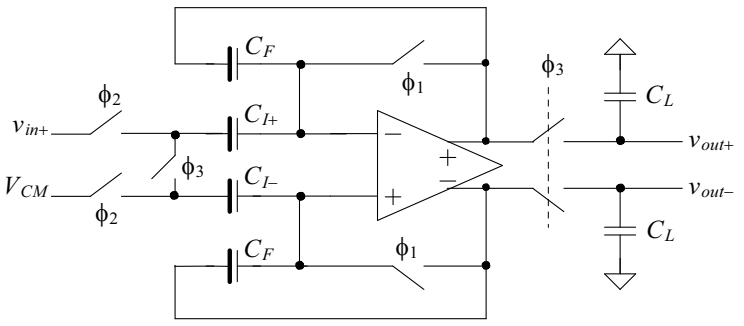

Figure 2.53 S/H for single-ended to differential conversion.

Equating the redistributed charge through C_F and C_I

$$C_{I+} \cdot (v_{in+} - V_{CM} \pm V_{OS}) = C_F \cdot (v_{out+} - V_{CM} \pm V_{OS}) + C_{I+} \cdot \left(\frac{v_{in+}}{2} - V_{CM} \pm V_{OS} \right) \tag{2.91}$$

or

$$C_F \cdot (v_{out+} - V_{CM} \pm V_{OS}) = C_{I+} \cdot \frac{v_{in+}}{2} \tag{2.92}$$

Assuming $C_{I+} = C_{I-}$ and taking the difference in the S/H outputs gives

$$\frac{v_{out+} - v_{out-}}{v_{in+}} = \frac{C_I}{C_F} \cdot [1 + 2V_{OS}] \tag{2.93}$$

Note that this topology doesn't employ correlated double sampling (CDS). Also note that if we model the op-amp's offset with a single voltage source in series with the non-inverting input of the op-amp then one of the inputs will go to $V_{CM} + V_{OS}/2$ while the other input will go to $V_{CM} - V_{OS}/2$ (we've just indicated the inputs of the op-amp are at a potential of $V_{CM} \pm V_{OS}$). Hence the factor of two in Eq. (2.93). In other words, if we re-write all of the equations in this chapter by replacing V_{OS} with $V_{OS}/2$ then the factor of two in Eq. (2.93) will go away. Simulations at CMOSedu.com are invaluable to understanding the operation of the circuits in this chapter. For example, see the simulation for Fig. 2.53.

2.2.3 The Discrete Analog Integrator (DAI)

The final sampling circuit we'll discuss in this chapter is an analog building block that we will find useful in implementing our data converters using feedback. The discrete analog integrator, DAI, is shown in Fig. 2.54. The two clocks signals, ϕ_1 and ϕ_2, form nonoverlapping clock signals. The common mode voltage, V_{CM}, falls halfway between the mixed-signal system's high- and low-reference voltages (generally *VDD* and ground). Note that the parasitic capacitance to ground associated with the bottom-plate of C_I is charged back and forth between v_1 and v_2 but doesn't affect the amount of charge transferred to the feedback capacitor, C_F. For this reason this DAI is often called a *parasitic-insensitive integrator*.

Table 2.2 shows the various relationships between the possible inputs and outputs for the DAI of Fig. 2.54. Let's derive the input/output relationships for the most general situations where both v_1 and v_2 are the inputs.

Table 2.2 Discrete analog integrator (DAI) input/output relationships.

Input	Output connected to ϕ_1	Output connected to ϕ_2
v_1 = input and $v_2 = V_{CM}$	$\frac{z^{-1}}{1-z^{-1}} \cdot \frac{C_I}{C_F}$	$\frac{z^{-1/2}}{1-z^{-1}} \cdot \frac{C_I}{C_F}$
v_2 = input and $v_1 = V_{CM}$	$\frac{-z^{-1/2}}{1-z^{-1}} \cdot \frac{C_I}{C_F}$	$\frac{-1}{1-z^{-1}} \cdot \frac{C_I}{C_F}$
v_1 and v_2 are both inputs	$\frac{V_1(z) \cdot z^{-1} - V_2(z) \cdot z^{-1/2}}{1-z^{-1}} \cdot \frac{C_I}{C_F}$	$\frac{V_1(z) \cdot z^{-1/2} - V_2(z)}{1-z^{-1}} \cdot \frac{C_I}{C_F}$

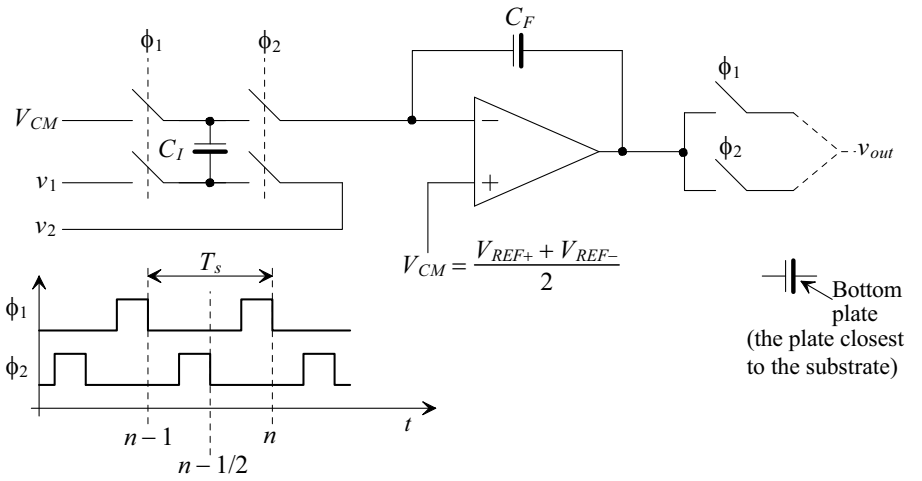

Figure 2.54 Schematic diagram of a discrete analog integrator (DAI).

To begin, let's assume the output of the DAI is connected to the op-amp through the ϕ_1 switch. When the ϕ_1 switches are closed (ϕ_1 is high) at $n-1$ (the instance when the switches shut off), the charge stored on C_I is

$$Q_1 = C_I(V_{CM} - v_1[(n-1)T_s]) \tag{2.94}$$

and the output of the integrator is $v_{out}[(n-1)T_s]$. When the ϕ_2 switches turn on the charge stored on C_I becomes

$$Q_2 = C_I(V_{CM} - v_2[(n-1/2)T_s]) \tag{2.95}$$

remembering that the op-amp holds its noninverting input terminal at V_{CM}. The difference in these charges, $Q_2 - Q_1$, is transferred to the op-amp's feedback capacitor resulting in an output voltage change. This change can be written as

$$(v_{out}[nT_s] - v_{out}[(n-1)T_s])C_F = C_I(v_1[(n-1)T_s] - v_2[(n-1/2)]T_s) \tag{2.96}$$

or writing this equation in the z-domain results in

$$v_{out}(z)(1-z^{-1}) = \frac{C_I}{C_F}(v_1(z)\cdot z^{-1} - v_2(z)\cdot z^{-1/2}) \tag{2.97}$$

The transfer function of the DAI with the output connected to the ϕ_1 switches is then

$$v_{out}(z) = \frac{C_I}{C_F}\cdot\frac{v_1(z)\cdot z^{-1} - v_2(z)\cdot z^{-1/2}}{1-z^{-1}} \tag{2.98}$$

Similarly, if we connect the output through the ϕ_2 switches (the edges we label n in Fig. 2.54 shift in time by $T_s/2$) we can write

$$Q_1 = C_I(V_{CM} - v_1[(n-1/2)T_s]) \tag{2.99}$$

$$Q_2 = C_I(V_{CM} - v_2[nT_s]) \tag{2.100}$$

and

$$(v_{out}[nT_s] - v_{out}[(n-1)T_s])C_F = C_I(v_1[(n-1/2)T_s] - v_2[nT_s]) \tag{2.101}$$

The transfer function of the DAI with the output connected to the ϕ_2 switches is then

$$v_{out}(z) = \frac{C_I}{C_F} \cdot \frac{v_1(z) \cdot z^{-1/2} - v_2(z)}{1 - z^{-1}} \tag{2.102}$$

Note that if $v_2(z) = V_{CM}$, this equation can be written as

$$H(z) = \frac{v_{out}(z)}{v_1(z)} = \frac{C_I}{C_F} \cdot \frac{z^{-1/2}}{1 - z^{-1}} \tag{2.103}$$

which has a frequency response, $|H(f)|$, shown in Fig. 1.27. Note that the factor C_I/C_F simply scales the amplitude response. If this factor is unity then the magnitude response, as shown in Fig. 1.27, is 0.5 at $f_s/2$. The $z^{-1/2}$ term in the numerator simply modifies the phase response of the DAI (delaying the output by $T_s/2$ or −180 degrees) and has no effect on the magnitude response. Note that at this point we could discuss the frequency responses of the transfer functions given in Table 2.2. However, we would see that the discussions and results given in Ch.1 for the digital integrator would apply to the DAI with little, or no, modifications.

Example 2.6

Determine the transfer function of the DAI of Fig. 2.54 *without* the switches on the output of the op-amp.

Reviewing Fig. 2.54 we see that charge is transferred to the feedback capacitor only when the ϕ_2 switches are closed. Therefore, the output only changes states during the time interval when the ϕ_2 switches are closed. The transfer function of the DAI, when no switches are used on the output of the op-amp, is given by Eq. (2.102). Using the ϕ_1 switches simply adds a half clock cycle delay, $z^{-1/2}$, to the integrator's transfer function (instead of the output changing with the rising edge of ϕ_2, the output changes one-half cycle later on the rising edge of ϕ_1). ■

A Note Concerning Block Diagrams

As we draw block diagrams describing our modulator topologies in this chapter and the next we often show a circuit like the one shown in Fig. 2.55. The summation, gain, and integrating blocks are implemented with a single switched-capacitor DAI having the transfer function given by Eq. (2.102). The gain, G, of the DAI is set by the ratio of

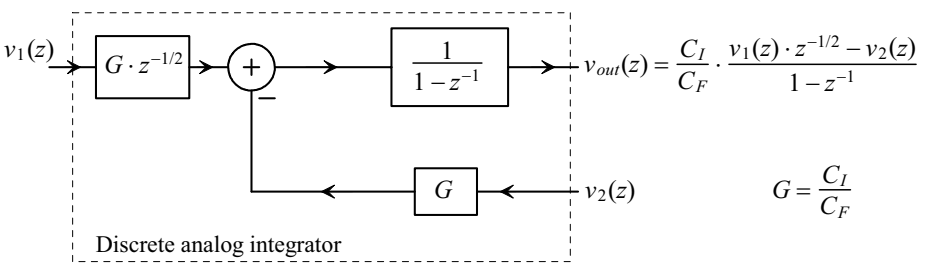

Figure 2.55 Block diagram of a DAI.

capacitors as indicated in the figure. It's important to realize that this circuit is entirely analog and is interfaced to, in general, both ADCs ($v_{out}[z]$ is connected to the input of an ADC) and DACs ($v_2[z]$ is connected to the output of a DAC).

It should be clear from both Fig. 2.54 and Table 2.2 that many different combinations of discrete analog building blocks are possible. Figure 2.56 shows two other possibilities. In part (a) the capacitors used have the same parasitic capacitance on each plate so there is no benefit to using a parasitic insensitive topology. The transfer function of this DAI is

$$v_{out}(z) = \frac{C_I}{C_F} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot (v_2(z) - v_1(z)) \tag{2.104}$$

noting each input signal sees the same delay, i.e., z^{-1} when the outputs are connected through ϕ_1 controlled switches and $z^{-1/2}$ delay when no switches or ϕ_2 controlled switches are used. If the integrator inputs must see the same delay and the capacitors available have asymmetric parasitic capacitance, the topology of Fig. 2.56b can be used. Its transfer function is

$$v_{out}(z) = \frac{z^{-1}}{1 - z^{-1}} \cdot \left(\frac{C_{I1}}{C_F} \cdot v_1(z) + \frac{C_{I2}}{C_F} \cdot v_2(z) \right) \tag{2.105}$$

noting the input signals can be scaled independently (a useful feature in filter design and discussed further in the next chapter).

Fully-Differential DAI

While we've derived the equations governing the operation of the DAI using a single-ended topology, in most practical circuits we'll use fully-differential implementations. The same equations apply to both configurations. Figure 2.57 shows the schematic for the fully-differential DAI. Note how we keep the bottom plates of the capacitors away from the op-amp's inputs.

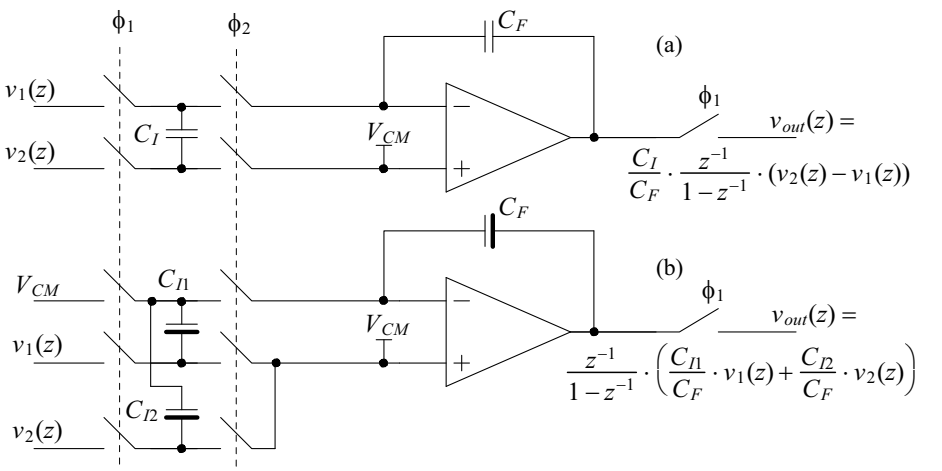

Figure 2.56 Other forms of DAIs.

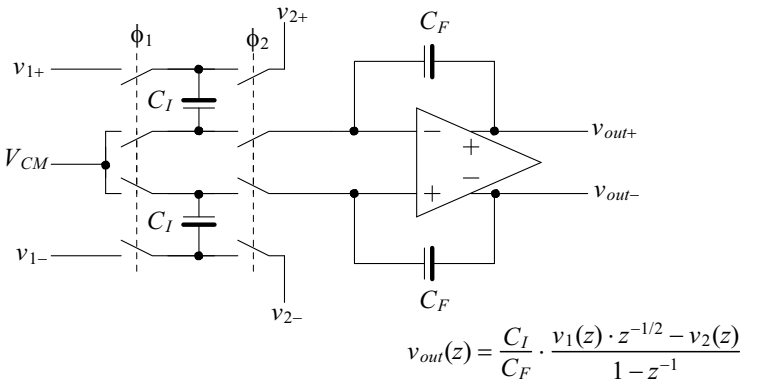

Figure 2.57 Fully-differential discrete-analog integrator (DAI) implementation.

DAI Noise Performance

Figure 2.58 shows the DAI with kT/C noise sources shown (see Table 2.1). The mean squared input- referred noise is given by

$$V_{in,RMS}^2 = \frac{kT}{C_I} \text{ (units of } V^2\text{)} \tag{2.106}$$

in series with both v_1 and v_2. A total of $2kT/C_I$ is sampled onto C_I during each clock cycle. If the input signal can swing from VDD to ground (peak value of the input is $VDD/2$ while the RMS value of this input is $VDD/\left(2\sqrt{2}\right)$), then we can estimate the SNR using

$$\text{SNR} = 20\log\frac{VDD/\left(2\sqrt{2}\right)}{\sqrt{2kT/C_I}} \tag{2.107}$$

This equation is useful for determining the capacitor values used in a DAI.

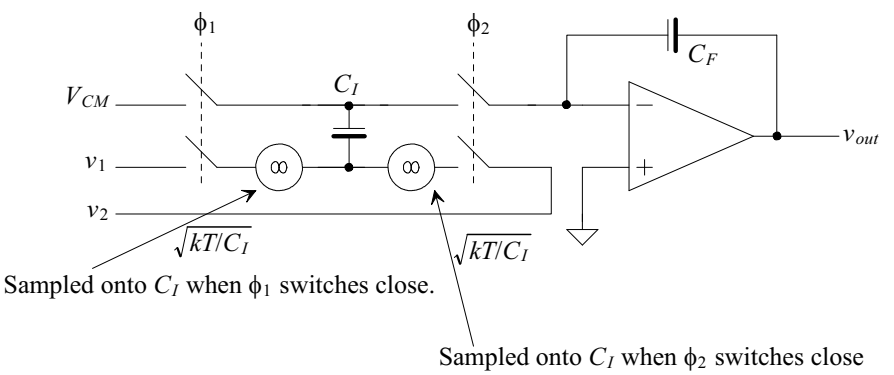

Figure 2.58 Noise performance of the DAI.

ADDITIONAL READING

[1] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation, Revised Second Edition*, Wiley-IEEE, 2008. ISBN 978-0470229415

[2] C. C. Enz and G. C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE*, Vol. 84, No. 11, pp. 1584-1614, November 1996.

[3] L. W. Couch, *Modern Communication Systems: Principles and Applications*, Prentice-Hall, 1995. ISBN 978-0023252860

QUESTIONS

2.1 Qualitatively, using figures, show how impulse sampling a sinewave can result in an alias of the sampled sinewave at a different frequency.

2.2 Re-sketch Figs. 2.12 and 2.13 when decimating by 5. hint: use a counter and some logic to implement the divide by 5 clock divider.

2.3 Explain why returning the output of the S/H to zero reduces the distortion introduced into a signal. What is the cost for the reduced distortion in a practical circuit?

2.4 Sketch the input and output spectrum for the following block diagram. Assume the DC component of the input is 0.5 V while the AC component is a sinewave at 4 MHz with a peak amplitude of 100 mV. Assume the clock frequency is 100 MHz.

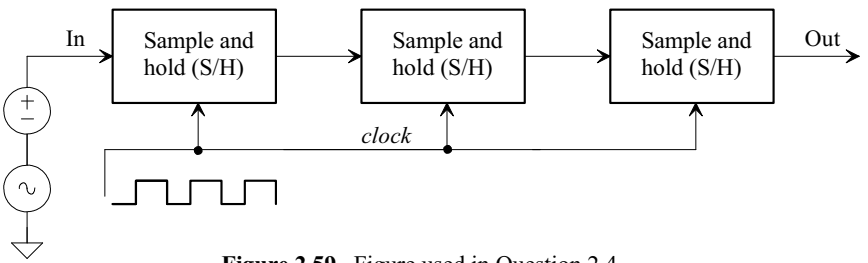

Figure 2.59 Figure used in Question 2.4.

2.5 Repeat Ex. 2.2 with an input sinewave at 30 MHz.

2.6 Re-sketch Fig. 2.22 if the input signal is a sinewave at 10 MHz (no other spectral content).

2.7 Suppose we are interpolating, with $K = 8$, digital data with $f_s = 100$ MHz. Prior to interpolation what is the frequency range of the desired spectrum? After interpolation what is the frequency range of the desired spectrum? What is the interpolator's output clock rate?

2.8 Verify, with simulations, that the topologies seen in Fig. 2.34 are equivalent.

2.9 Determine the transfer function, and verify with simulations, the behavior of 4 paths of the switched-capacitor topology seen in Fig. 2.36.

2.10 In your own words discuss why the ϕ_2 switches are shut off after the ϕ_1 switches in the S/H seen in Fig. 2.39.

2.11 Sketch the op-amp's open loop response, both magnitude and phase, specified by Eq. (2.59).

2.12 What is the voltage across C_F in Fig. 2.41 in terms of the input-referred offset and noise? Verify your answer with simulations commenting on the deviation of the frequency behavior of the input-referred noise to the frequency response of the voltage across the capacitor.

2.13 Provide a quantitative description of how capacitor mismatch will affect the operation of the S/H seen in Fig. 2.46. Verify your descriptions with simulations.

2.14 Is it possible to design a S/H with a gain of 0.5? How can this be done or why can't it be done? Use simulations to verify your answer.

2.15 For the first entry (v_1 = input, $v_2 = V_{CM}$) in Table 2.2 derive the frequency response, magnitude and phase, of the DAI. Use simulations at a few frequencies to verify your derivations.

2.16 Repeat Question 2.15 for the second entry.

2.17 Repeat Question 2.15 for the third entry.

2.18 Does the DAI use CDS? Why or why not? Use simulations to support your answers.