Chapter
3

Analog Filters

In the last chapter we discussed that analog anti-aliasing filters (AAFs) and reconstruction filters (RCFs) are an important component of a mixed-signal system. While we can perform signal processing and filtering in the digital domain, as seen in Fig. 2.1, AAFs and RCFs are still required in our system. Analog continuous-time filters can be faster (have wider bandwidths) and take up less area than their analog discrete-time (e.g., switched-capacitor) counterparts. However, unlike discrete-time filters, continuous- time filters cannot be fabricated with precise transfer functions and must be tuned. This is especially true if passive resistors and capacitors are used. Each one can have a variation of $\pm 20\%$. By using active CMOS integrators in the filter implementations instead of passive elements, we can electrically tune the filters. Also, we can more easily implement higher order filters while minimizing the effects of loading.

In this chapter we discuss analog filters made using continuous-time analog integrators (CAIs or active-RC integrators), MOSFET-C integrators, transconductor-capacitor (g_m-C) integrators, and discrete-time analog integrators (DAIs). Our focus is on practical analog filters for mixed-signal AAFs and RCFs. These filters may have fully-differential inputs and outputs so the common-mode voltage of the op-amp used in the active filter remains constant (important for noise and distortion). Further, inverting a signal using fully-differential topologies is trivial since we simply swap the filter's outputs. Single-ended topologies where the op-amp's common mode voltage can vary, such as Sallen-Key, and topologies that require separate amplifiers to generate an inversion such as Tow-Thomas biquad, are covered in the excellent books by Franco [1] and Schaumann [2].

3.1 Integrator Building Blocks

3.1.1 Lowpass Filters

In order to methodically develop our understanding of CMOS filters, consider the lowpass filter shown in Fig. 3.1. The transfer function of this filter is

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{1}{1 + j\omega RC} \tag{3.1}$$

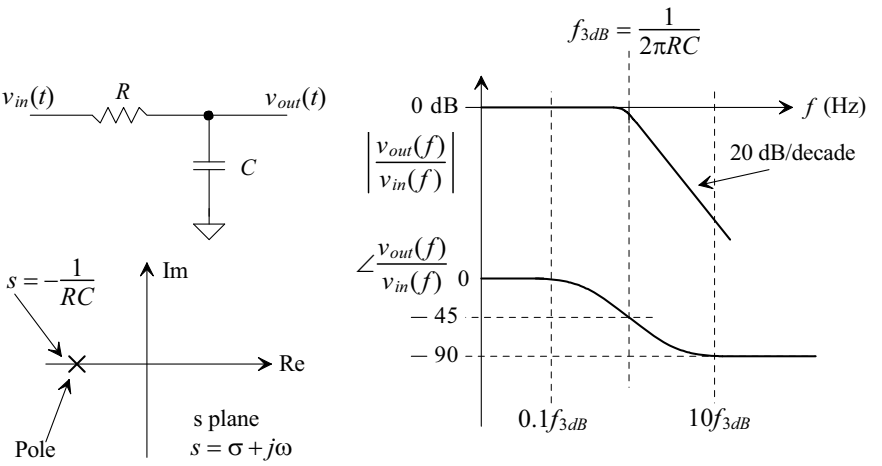


Figure 3.1 First-order lowpass filter.

where $\omega = 2\pi \cdot f$ and f is the frequency of the input (and thus the output). Next, consider the block diagram in Fig. 3.2. This figure shows an integrator and a summing block. The output of the block diagram can be determined by solving

$$v_{out}(f) = \frac{G}{s} \cdot (v_{in}(f) - v_{out}(f)) \tag{3.2}$$

or

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{1}{1 + s/G} \tag{3.3}$$

where for a sinewave input $s = j\omega$. Comparing this equation to Eq. (3.1), we see that if we set the integrator's gain, G, using

$$G = \frac{1}{RC} \text{ where } f_{3dB} = \frac{G}{2\pi} \tag{3.4}$$

we can use an integrator to implement a lowpass first-order filter (the filter has a single pole).

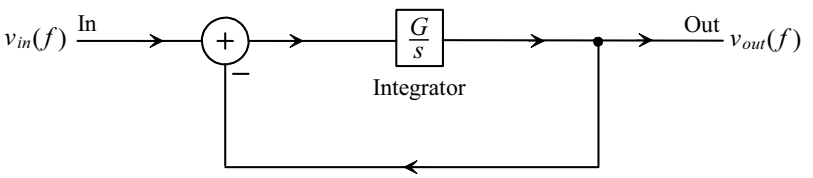


Figure 3.2 Block diagram of an integrator-based lowpass filter.

3.1.2 Active-RC Integrators

A continuous-time, fully-differential, analog integrator (CAI) is seen in Fig. 3.3. The CAI goes by other names, including the Miller integrator, the active-RC integrator, and when the resistors are replaced with MOSFETs operating in the triode region, the MOSFET-C integrators. The gain of the CAI can be written as

$$\frac{v_{out}}{v_{in}} = \frac{v_{out+} - v_{out-}}{v_{in+} - v_{in-}} = \frac{1}{s} \cdot \overbrace{\frac{1}{RC}}^{G} \tag{3.5}$$

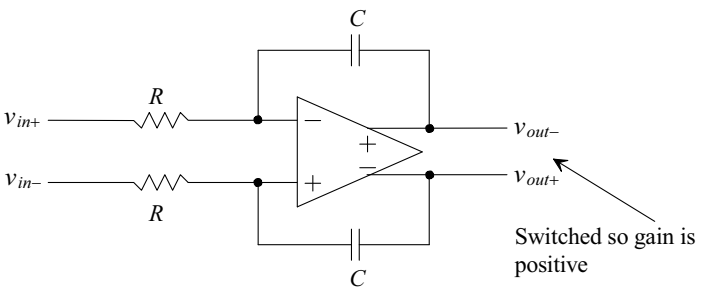


Figure 3.3 A continuous-time analog integrator (CAI).

Reviewing Fig. 3.2, we see that the CAI of Fig. 3.3 alone will implement the needed integration but not the summing (difference) block. By adding an additional feedback path, the entire block diagram of Fig. 3.2 can be implemented. Figure 3.4 shows the integrator-based implementation of the circuits in Figs. 3.1 and 3.2 (noting the op-amp must be able to drive a resistive load). This filter is called an *active-RC* filter because the RC is used with an active element (the op-amp). At this point there are several practical and useful modifications that we can make to this filter. However, let's work an example before moving on.

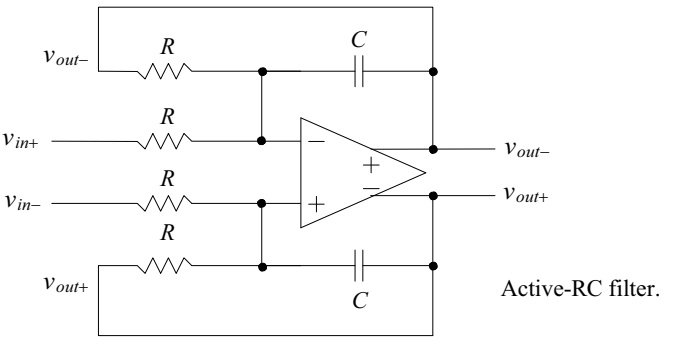


Figure 3.4 Implementation of a first-order lowpass filter using a CAI.

Example 3.1
Simulate the operation of the filter in Fig. 3.4 from DC to 100 MHz if R = 10k and C = 10 pF. Show both the magnitude and phase responses of the filter. Assume the op-amp is ideal.

From Fig. 3.1 we know the 3 dB frequency of the filter is 1.59 MHz. The simulation results are shown in Fig. 3.5. The magnitude and phase response follow, as expected, the responses for the simple RC filter shown in Fig. 3.1. ■

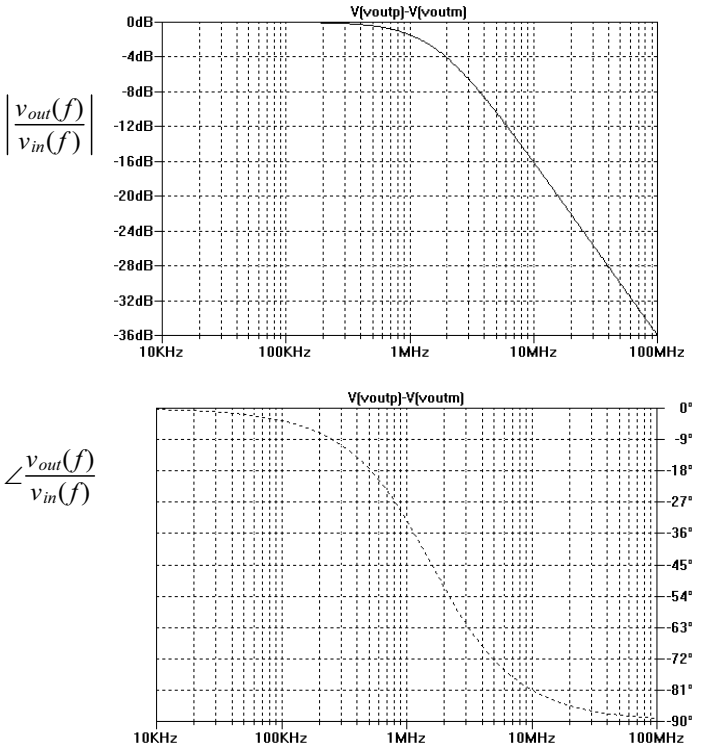


Figure 3.5 Magnitude and phase responses for the first-order filter in Fig. 3.4 if R = 10k and C = 10 pF.

What would happen if we switched what we define as v_{out+} and v_{out-} in the filter described in Ex. 3.1 without changing any other connections? Perhaps it is trivial, but the answer is that the output will be inverted. We can modify the block diagram of Fig. 3.2 by simply multiplying the output by −1, as seen in Fig. 3.6. The phase shift in Fig. 3.5 would shift up or down by 180 degrees. It would vary from 180 to 90 degrees, or from −180 to −270 (because +180 degrees is the same as −180 degrees) instead of from 0 to −90 degrees. If we allow the resistors used in the filter to have different values, as seen in Fig. 3.6, we can add a feedback gain to our block diagram. Assuming the outputs are labeled so that we don't have an inversion in the output of the filter (i.e., they are labeled as seen in Fig. 3.4), we can write

$$\frac{v_{in}}{R_I} - \frac{v_{out}}{R_F} = \frac{v_{out}}{1/sC} \tag{3.6}$$

It's important to notice (for later use) that in order to subtract the output from the input, the voltages are first changed to currents and then summed (or more correctly subtracted) on the inputs of the op-amp. This equation can be rewritten as

$$\frac{v_{out}}{v_{in}} = \frac{\frac{R_F}{R_I}}{1 + sR_FC} \tag{3.7}$$

Using the block diagram in Fig. 3.6, we can write

$$\frac{v_{out}}{v_{in}} = \frac{\frac{1}{G_2}}{1 + \frac{s}{G_1G_2}} \text{ and } f_{3dB} = \frac{G_1G_2}{2\pi} \tag{3.8}$$

Equating coefficients in these equations results in

$$G_2 = \frac{R_I}{R_F} \text{ and } G_1 = \frac{1}{R_IC} \tag{3.9}$$

Note that at DC where $s \to 0$, the block diagram in Fig. 3.6 becomes the classic feedback diagram with the forward gain approaching infinity and a feedback factor of G_2. Then from classic feedback theory, the closed-loop gain becomes $1/G_2$ or, for the filter in Fig. 3.6, R_F/R_I. Of course, analyzing this circuit (using loop equations) at DC when the capacitor is an open results in the same gain.

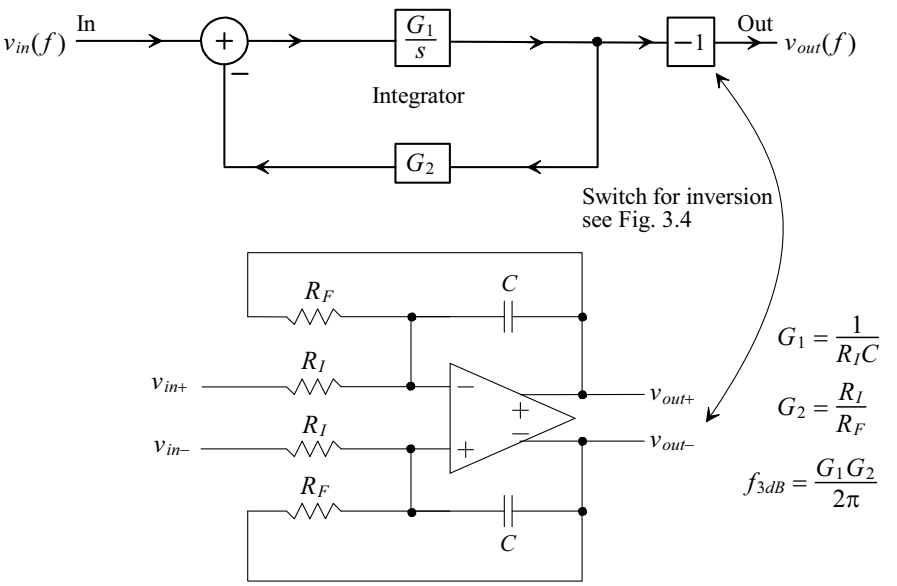


Figure 3.6 Integrator-based first-order filter.

Example 3.2
Modify the filter in Ex. 3.1 so that the low-frequency gain is 20 dB.

Using Eq. (3.7) or Eq. (3.8), we leave C = 10 pF and R_F = 10k. To get the gain of 10, we make R_I = 1k. The simulation results are shown in Fig. 3.7. ■

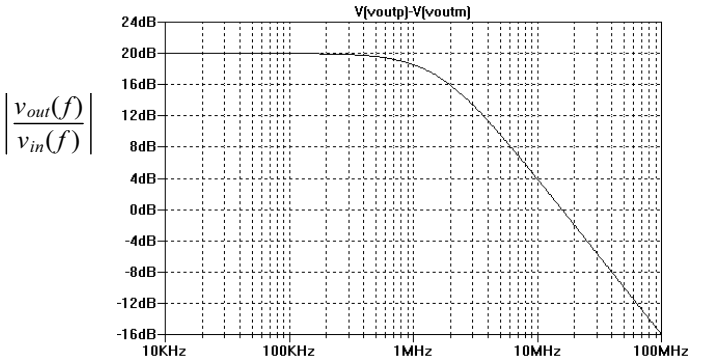


Figure 3.7 A first-order filter with gain, see Ex. 3.2.

Effects of Finite Op-Amp Gain Bandwidth Product, f_{un}

In the previous two examples we assumed a near-ideal op-amp. The open-loop gain of the op-amp can be written, assuming a dominant-pole compensated op-amp, by

$$A_{OL}(f) = \frac{v_{out}}{v_+ - v_-} = \frac{A_{OLDC}}{1 + j \cdot \frac{f}{f_{3dB}}} \tag{3.10}$$

where v_+ and v_- are the voltages on the noninverting and inverting op-amp input terminals, respectively. Note that we are using f_{3dB} in both Figs. 3.6 and Eq. (3.10) to indicate the 3 dB frequency of a frequency response. While the symbol is the same the actual values vary from circuit to circuit. When a practical op-amp is operating at frequencies above a few kHz, we can approximate the open-loop response (knowing the imaginary part of the denominator is much larger than the real part) as

$$A_{OL}(f) \approx \frac{A_{OLDC} \cdot f_{3dB}}{j \cdot f} = \frac{f_{un}}{j \cdot f} = \frac{2\pi f_{un}}{s} = \frac{\omega_{un}}{s} \tag{3.11}$$

where f_{un} is the frequency where the op-amp's open loop gain is unity (0 dB). Rewriting Eq. (3.6) to include the op-amp's finite gain bandwidth product (that is, f_{un}) and assuming, without the loss of generality, that the op-amp is operating with a single-ended output (v_+ tied to V_{CM} [AC ground]), results in

$$\frac{v_{in} - v_-}{R_I} + \frac{v_{out} - v_-}{R_F} + sC \cdot (v_{out} - v_-) = 0 \tag{3.12}$$

After some algebraic manipulation with $v_- = -v_{out}/A_{OL}(f)$, we get

$$\frac{v_{out}}{v_{in}} = \frac{-\frac{R_F}{R_I}}{\underbrace{1 + sCR_F}_{\text{Desired response}} + \frac{sCR_F}{A_{OL}(f)} + \frac{1}{A_{OL}(f)}\left(1 + \frac{R_F}{R_I}\right)} \tag{3.13}$$

or, with $A_{OL}(f) = \omega_{un}/s$

$$\frac{v_{out}}{v_{in}} = \frac{-\frac{R_F}{R_I}}{s^2\frac{CR_F}{\omega_{un}} + s\cdot\left[CR_F + \frac{1}{\omega_{un}}\left(1+\frac{R_F}{R_I}\right)\right] + 1} \tag{3.14}$$

This equation is very revealing and shows just how significant a limitation the op-amp can be in a filter. For the moment, to simplify things, let's assume $\omega^2 << \omega_{un}/CR_F$ so that the s^2 term in Eq. (3.14) is negligible. We can then write the magnitude and phase responses as

$$\left|\frac{v_{out}}{v_{in}}\right| = \frac{\frac{R_F}{R_I}}{\sqrt{1+\left[\omega CR_F + \frac{\omega}{\omega_{un}}\left(1+\frac{R_F}{R_I}\right)\right]^2}} \text{ and } \angle\frac{v_{out}}{v_{in}} = -\tan^{-1}\left[\omega CR_F + \frac{\omega}{\omega_{un}}\left(1+\frac{R_F}{R_I}\right)\right] \tag{3.15}$$

Example 3.3

Suppose a first-order filter is designed based on the topology seen in Fig. 3.6, where $\omega_{un} = 10/R_FC$ and $R_F/R_I = 10$. Assuming $\omega^2 << \omega_{un}/CR_F$, comment on how the magnitude and phase responses of the filter will be affected by the finite op-amp, f_{un}.

The op-amp's unity gain frequency is only 10 times larger than the bandwidth of the filter. This means the op-amp's closed-loop bandwidth (with a gain of 10) is equal to the desired bandwidth of the filter. The bandwidth of a gain of 10 op-amp circuit is $f_{un}/10$, which here is equal to the ideal filter 3 dB frequency of $1/2\pi R_FC$. The magnitude of the filter's response can be approximated as

$$\left|\frac{v_{out}}{v_{in}}\right| = \frac{\frac{R_F}{R_I}}{\sqrt{1+[\omega\cdot 2CR_F]^2}} \text{ and } \angle\frac{v_{out}}{v_{in}} = -\tan^{-1}[\omega\cdot 2CR_F]$$

which shows the filter's 3 dB frequency is off by a factor of 2. ■

The point of the preceding example is, in general lowpass filter design, to minimize the effects of the op-amp's finite f_{un} a low value of closed-loop DC gain should be used. In the remaining discussion let's assume $R_F/R_I = 1$, so Eq. (3.14) can be approximated as

$$\left|\frac{v_{out}}{v_{in}}\right| \approx \frac{1}{\frac{CR_F}{\omega_{un}}\cdot s^2 + s\cdot CR_F + 1} \tag{3.16}$$

The poles of this transfer function are located at

$$s_{p1,p2} = \frac{-CR_F \pm \sqrt{(CR_F)^2 - 4\frac{CR_F}{\omega_{un}}}}{2\cdot\frac{CR_F}{\omega_{un}}} \tag{3.17}$$

noting that if $\omega_{un} \to \infty$, then $s_{p1} = \infty$, and $s_{p2} = -1/CR_F$ (the ideal position of the pole, see Fig. 3.1).

To get some idea of the required op-amp f_{un} ($\omega_{un} = 2\pi f_{un}$), let's assume that we want the pole to vary no more than 1% from the ideal location due to finite op-amp bandwidth

$$\frac{-1}{CR_F} = \frac{99}{100} \cdot \frac{-CR_F - \sqrt{(CR_F)^2 - 4\frac{CR_F}{\omega_{un}}}}{2 \cdot \frac{CR_F}{\omega_{un}}} \tag{3.18}$$

This can be rewritten as

$$1.01 = \frac{\omega_{un} \cdot CR_F}{2} - \frac{1}{2}\sqrt{(\omega_{un} \cdot CR_F)^2 - 4(\omega_{un} \cdot CR_F)} \tag{3.19}$$

If we let $x = \omega_{un} \cdot CR_F$, then we need to solve

$$x - \sqrt{x^2 - 4x} = 2.02 \tag{3.20}$$

knowing x is positive and much larger than one ($\omega_{un} >> 1/CR_F$). Solving Eq. (3.20) for x, results in $x = 100$. This means the op-amp's unity gain frequency must be 100 times larger than the filter's f_{3dB} in order for the variation of this frequency (the pole) to deviate less than 1% from the ideal. If we can withstand a 10% decrease in the filter's cutoff frequency, then f_{un} need only be 10 times larger than the filter's f_{3dB}. Clearly, from Eq. (3.14), the first-order filter's frequency response is actually second-order when the op-amp's gain bandwidth product f_{un} is a factor. Therefore, the shapes of the magnitude and phase responses will deviate from the ideal first-order shapes seen in Fig. 3.1. *We can draw two very practical conclusions*. First, even if it were possible to fabricate precise resistor and capacitor values, the limitations of the op-amp's finite bandwidth may still require the use of tuning when filtering with active-RC integrator-based filters. Tuning would consist of adding or removing resistors and capacitors to adjust the precise filter cutoff frequency (adding/removing the elements using either fuses or, if possible, MOSFET switches). Second, the op-amp's f_{un} should be at least 10 times larger than the cutoff frequency (f_{3dB}) of the filter (again assuming a closed-loop DC gain of unity, i.e., $R_F/R_I = 1$). This is a general "rule-of-thumb." Precision filters (well-defined magnitude and phase responses) would require wider bandwidth op-amps. Consider the following example.

Example 3.4

Repeat Ex. 3.1 if an op-amp is used with a DC gain of 10,000 and an f_{un} of 10 MHz.

Because the op-amp's A_{OLDC} is 10,000 and f_{un} = 10 MHz, the op-amp's open loop f_{3dB} is 1 kHz (see Eq. [3.11]). We can use the circuit shown in Fig. 3.8 in our SPICE simulation to model an op-amp with finite f_{un}. The RC in Fig. 3.8 is selected to give an op-amp open loop f_{3dB} of 1 kHz.

The 3-dB frequency of the filter described in Ex. 3.1 is, under ideal conditions, 1.59 MHz. Because our op-amp's unity gain frequency is only 10 MHz, we would expect, from Eq. (3.16), the op-amp to affect the frequency response of the filter. Figure 3.9 shows the simulation results using the op-amp model of Fig. 3.8. Comparing Fig. 3.9 to Fig. 3.5, we see differences in both the magnitude and phase responses of the filters. The magnitude response of Fig. 3.9 initially rolls off at 20 dB/decade below the ideal 1.59 MHz. Around 10 MHz the response

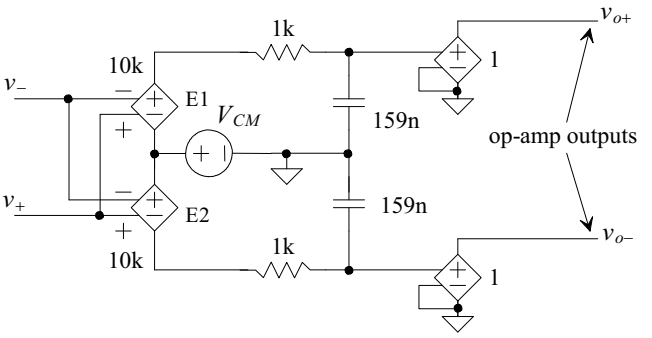


Figure 3.8 SPICE modeling of a differential input/output op-amp with finite bandwidth.

transitions to 40 dB/decade. Clearly this faster roll-off is the result of the op-amp's closed-loop pole coming into play. The limiting behavior of the op-amp, when looking only at the magnitude response, may be welcome (the filter's response rolls off faster) in a lowpass filter. However, it is not welcome in other filters (a highpass filter, for example). Figure 3.10 shows what happens if we decrease the filter's 3 dB frequency to 159 kHz by increasing the resistors used to 100k. What we are doing here is showing how making the op-amp's bandwidth much larger than the filter's affects the frequency response of the circuit. The magnitude response starts to fall off at –40 dB/decade at the op-amp's unity gain frequency, f_{un}, of 10 MHz. Also seen in Fig. 3.10 is the phase response of the filter. The op-amp's (closed-loop) phase response, which starts rolling off one decade below f_{un}, results in the final phase shift of the filter approaching –180 degrees. ■

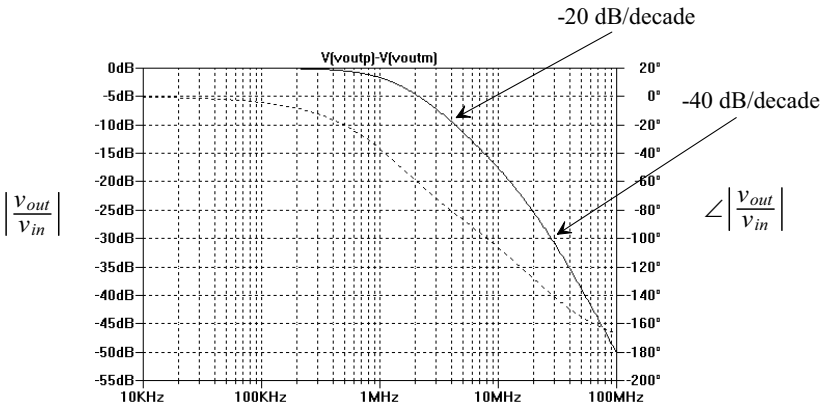


Figure 3.9 Magnitude and phase responses for the first-order filter in Fig. 3.4 if R=10k and C=10 pF using an op-amp with a 10 MHz unity-gain frequency.

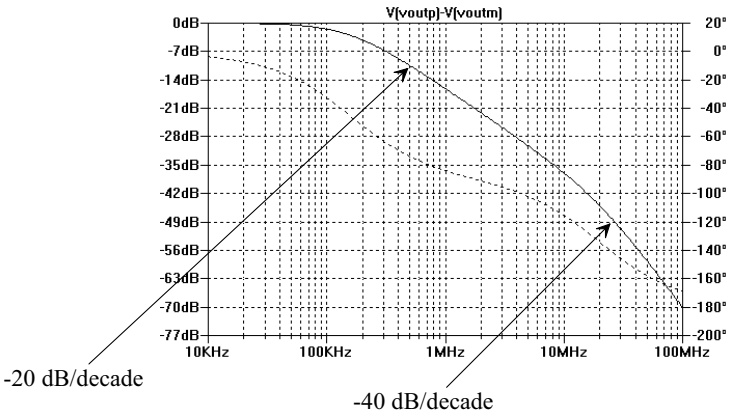


Figure 3.10 Increasing the resistance to 100k and replotting Fig. 35.9.

In order to model the effects of op-amp finite bandwidth on an active-RC filter's frequency response, we can add a pole to the ideal transfer function. Assuming unity gain in the passband (see Eq. [3.3]) results in

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{1}{1+s/G} \cdot \overbrace{\frac{1}{1+j\frac{f}{f_{un}}}}^{\text{Undesired}} \tag{3.21}$$

This result could have been used in the previous example to predict how the op-amp affects the filter's behavior. If the filter has gain (> 1) in the passband, see Eq. (3.8), we can modify this equation to read

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{\frac{1}{G_2}}{1+\frac{s}{G_1 G_2}} \cdot \overbrace{\frac{1}{1+j\frac{f}{G_2 \cdot f_{un}}}}^{\text{Undesired}} \tag{3.22}$$

For a higher order filter we would multiply the desired frequency response by the undesired term's (the op-amp's) response for each op-amp used in the circuit. Clearly, this limits the order of the filter (limits the number of op-amps used in a circuit; a first-order filter uses one op-amp, a second-order filter uses two op-amps, etc.). This is especially true if the filter has a passband approaching the f_{un} of the op-amps used.

Active-RC SNR

Consider the single-ended active-RC filter shown in Fig. 3.11. Let's assume an ideal op-amp with a maximum RMS output voltage of $VDD/(2\sqrt{2})$. The RMS input-referred noise of the filter, assuming thermal noise dominates over the bandwidth of interest, is simply $\sqrt{kT/C}$. The filter's *SNR* can then be written as

$$SNR = 20 \cdot \log \frac{VDD/\left(2\sqrt{2}\right)}{\sqrt{kT/C}} = 10 \cdot \log \frac{VDD^2/8}{kT/C} \tag{3.23}$$

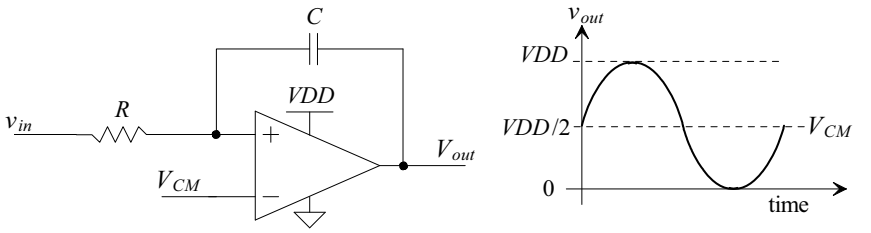


Figure 3.11 Estimating maximum possible SNR of an active-RC filter.

The size of the integrating capacitor fundamentally sets the *SNR* in integrator-based data converters or modulators. But consider the following: the maximum electrical energy stored in the capacitor used in an integrator is

$$\text{Maximum electrical energy} = \frac{1}{2}C \cdot \left(\frac{VDD}{2}\right)^2 \tag{3.24}$$

Equation (3.23) can then be rewritten as

$$SNR = 10 \cdot \log \frac{VDD^2/8}{kT/C} = 10 \cdot \log \frac{\frac{1}{2}C\left(\frac{VDD}{2}\right)^2}{kT} = 10 \cdot \log \frac{\text{Electrical energy}}{\text{Thermal energy}} \tag{3.25}$$

This equation can also be used to estimate the fundamental dynamic range, *DR*, of a filter. *Practically, DRs approaching 90 dB (*15 *bits)* can be attained using active-RC filters with good polysilicon resistors (to avoid the large nonlinear voltage coefficient associated with diffused or implanted resistors) and linear capacitors. Bandwidths approaching 50 MHz, assuming 500 MHz f_{un} op-amps are used, can be attained (at, of course, lower DRs).

3.1.3 MOSFET-C Integrators

Let's now look at a variation of the active-RC filter where the resistors are replaced with MOSFETs. Figure 3.12 shows a MOSFET-C filter. In order for the MOSFETs to behave as resistors they must remain in the triode region. Using long length devices helps ensure triode operation. Because the MOSFETs are operating as resistors, their speed is not governed directly by their gate-source voltage (overdrive voltage) or channel length. However, the linearity of the MOSFET resistors is still very important, as is the possibility that the MOSFETs will introduce a parasitic pole into the filter's frequency response because of the distributed resistance/capacitance of the channel (Fig. 3.12). For large input signals, the active MOSFET resistors become nonlinear, resulting in filters with *DRs of around only 40 dB*. The bandwidth of the MOSFET-C filters parallels that of the active-RC filters.

We might be questioning the usefulness of the MOSFET-C filter with a *DR* of only 40 dB. Clearly this filter will only find use in data conversion systems using six bits of resolution or less (36 dB *DR*) or in systems that process continuous-time signals. The big benefit of this filter over the active-RC filter is its ability to be tuned. Tuning the active-RC filter required adding or removing, via switches or fuses, resistors or capacitors in parallel or series with the existing resistors and capacitors. Tuning the MOSFET-C

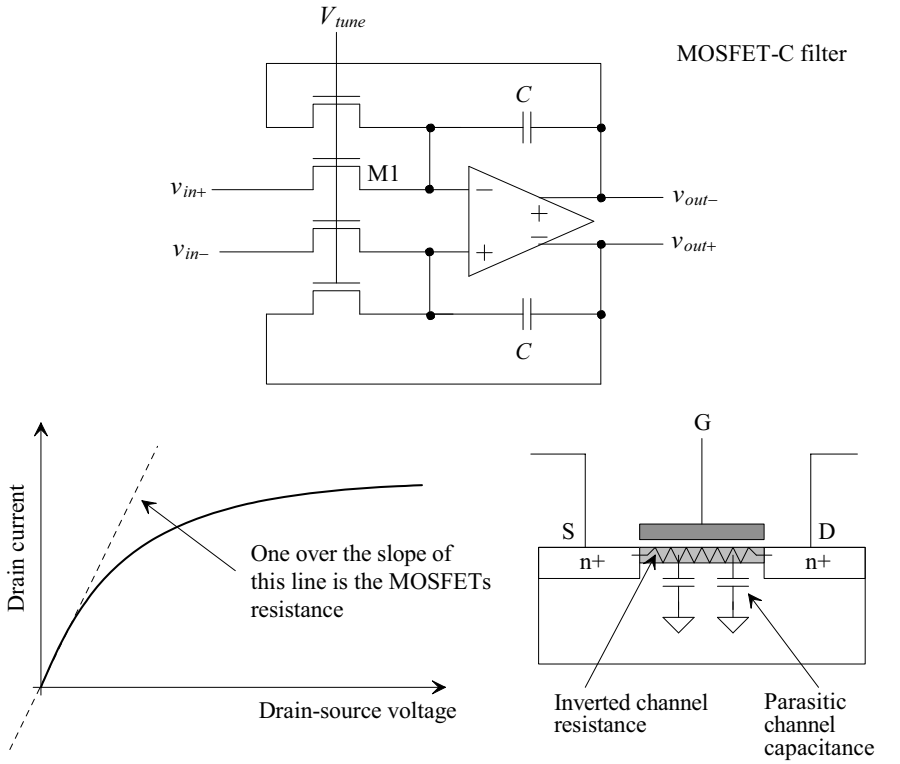


Figure 3.12 A first-order MOSFET-C filter.

filter shown in Fig. 3.12 can be accomplished by adjusting V_{tune}. If we assume long-channel behavior, we can write the resistance of the MOSFETs in terms of V_{tune} (assuming the input common-mode voltage of the op-amp is 0) as

$$R_n = \frac{1}{KP \cdot \frac{W}{L} \cdot \left(V_{tune} - V_{THN} - \underbrace{V_{DS}}_{= vin} \right)} \tag{3.26}$$

The current through M1 in Fig. 3.12 is

$$\frac{v_{in+}}{R_{n1}} = v_{in+} \cdot KP \cdot \frac{W}{L}(V_{tune} - V_{THN} - v_{in+}) \tag{3.27}$$

Some improvement in the linearity of the MOSFET resistors, say 10 dB (resulting in a *DR* of 50 dB), can be achieved by utilizing the fully-balanced signals available in the circuit. Consider replacing M1 in Fig. 3.12 with the pair of MOSFETs, M1A and M1B, shown in Fig. 3.13. The resulting current is now

$$\frac{v_{in+}}{R_{n1A}} + \frac{v_{in-}}{R_{n1B}} = KP \cdot \frac{W}{L}[v_{in+} \cdot (V_{tune+} - V_{THN} - v_{in+}) + v_{in-} \cdot (V_{tune-} - V_{THN} - v_{in-})] \tag{3.28}$$

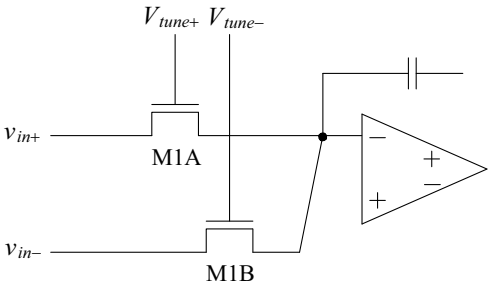


Figure 3.13 Linearizing MOSFET resistors.

Knowing $v_{in+} = -v_{in-}$ and letting $V_{tune} = V_{tune+} - V_{tune-}$, we can write the equivalent current through M1 as

$$\frac{v_{in+}}{R_{n1}} = v_{in+} \cdot KP \cdot \frac{W}{L} \cdot V_{tune} \tag{3.29}$$

The result is that the nonlinear behavior of the MOSFET's channel resistance due to the changing drain-source voltage cancels to a first order. Figure 3.14 shows the implementation of a first-order MOSFET-C filter using linearized MOSFETs.

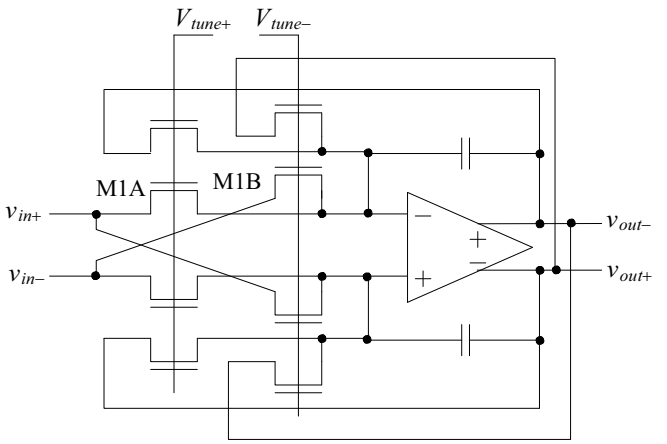


Figure 3.14 First-order MOSFET-C filter using linearized MOSFET resistors.

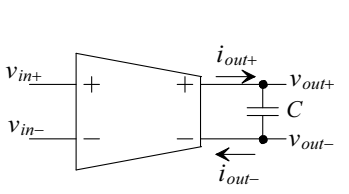
Why Use an Active Circuit (an Op-Amp)?

Before going any further, let's realize that we can get the exact same frequency performance using a simple resistor/capacitor or MOSFET/capacitor as we get when we use these elements with an op-amp. So, "Why use the op-amp?" The answer to this question comes when we realize that when a capacitive or resistive load is connected to the output of the filter (without an active element), the frequency behavior changes. Using

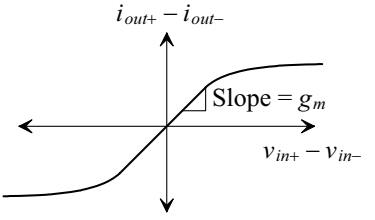
the op-amp allows us to drive an arbitrary (within reason) capacitive or resistive load. Using an active element will also allow us to cascade first-order sections to implement higher order filters.

3.1.4 g_m-C (Transconductor-C) Integrators

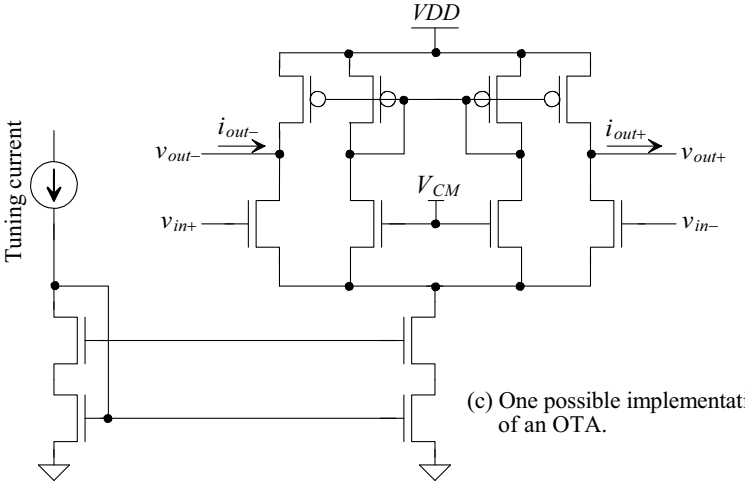
The operational-transconductance amplifiers, OTA, is an amplifier that has only two high-impedance nodes: the amplifier's input and its output. Figure 3.15 shows a schematic symbol, transfer curves, and a possible implementation for an OTA (based on a fully-differential diff-amp). Transconductor-C, or g_m-C, filters use a circuit, a transconductor, that provides a linear voltage-current transfer curve. Our OTA in Fig. 3.15 does behave like a transconductor over a portion of the input voltage range but becomes nonlinear for large input voltage differences, $v_{in+} - v_{in-}$. By increasing the lengths of the NMOS diff-pairs used in the OTA, we can increase the linear common-mode range of the OTA, making it appear as though it were a transconductor. The fundamental problems with increasing the lengths of the diff-pair MOSFETs are the increase in the OTA's input capacitance (affecting the location of the filter's poles and zeroes) and, perhaps more fundamentally, the inherent reduction in the MOSFET's f_T.



(a) Schematic symbol of an OTA or transconductor.



(b) Transfer curves for an OTA.



(c) One possible implementation of an OTA.

Figure 3.15 Showing an implementation of an OTA and transfer curves.

Before discussing these issues in more detail, let's look at an important limitation of g_m-C filters; namely, the fact that the transconductor's input voltage must vary. In any precision application, the input voltage must remain constant because of the roll-off associated with the amplifier's CMRR (unless, of course, the common-mode voltage can be held at a precise value). This *limits the DR of g_m-C filters to around 50 dB*. Again, this is not too useful if used as an antialiasing or reconstruction filter unless the system's resolution is less than eight bits (48 dB SNR). The g_m-C filter finds extensive use in continuous-time signal processing.

We can relate the input voltage difference to the output voltage difference for the circuit in Fig. 3.15a using

$$v_{out+} - v_{out-} = \frac{i_{out+}}{j\omega C} = \frac{i_{out-}}{j\omega C} = \frac{g_m(v_{in+} - v_{in-})}{j\omega C} \tag{3.30}$$

Comparing this result to Eq. (3.5), we can use the same design techniques if we require

$$G = \frac{1}{RC} = \frac{g_m}{C} \text{ or } f_{3dB} = \frac{G}{2\pi} \tag{3.31}$$

The big benefit of the g_m-C filter over the active-RC filter is the ability to tune the filter by adjusting the transconductor's g_m.

The circuit of Fig. 3.15a implements an integrator, as does the active-RC circuit of Fig. 3.3. However, as seen in Fig. 3.2, we also need to implement a summing block in a first-order filter. In order to move toward the goal of implementing the summing block, consider the transconductor circuit shown in Fig. 3.16a. The output current of a single transconductor is $g_m(v_{in+} - v_{in-})$. We can sum this current with the output current from the second transconductor to implement the summing block in Fig. 3.2. As seen in Fig. 3.16b, the outputs of the two OTAs are combined, so the output currents from each transconductor subtract. Assuming each transconductor has the same transconductance, we can write

$$g_m(v_{in+} - v_{in-}) - g_m(v_{out+} - v_{out-}) - j\omega C(v_{out+} - v_{out-}) = 0 \tag{3.32}$$

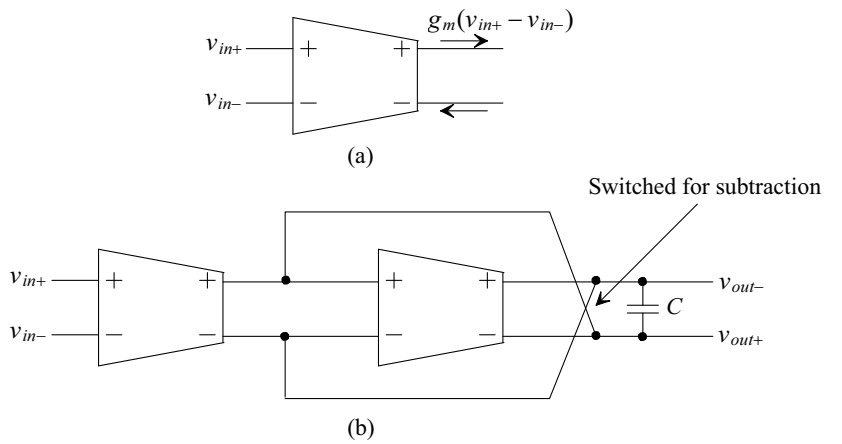


Figure 3.16 Implementing a first-order filter using transconductors.

or

$$\frac{v_{out+} - v_{out-}}{v_{in+} - v_{in-}} = \frac{1}{1 + j\omega C \cdot \frac{1}{g_m}} \tag{3.33}$$

If the transconductors have different g_ms, we can design a filter with a DC gain (see Problem 3.10), which can be characterized using Eq. (3.8).

Example 3.5

Repeat Ex. 3.1 using a g_m-C filter with a g_m of 100 μA/V.

To simulate a transconductor using SPICE, a voltage-controlled current source can be used as seen in Fig. 3.17. In order to set the output common-mode voltage to V_{CM} in the simulation, we add the large resistors (whose values can be changed to simulate the finite, nonideal, output resistance of the OTA) connected to V_{CM}. If we didn't use these resistors, after reviewing Fig. 3.16, it would result in an unknown common-mode voltage on the second transconductor input.

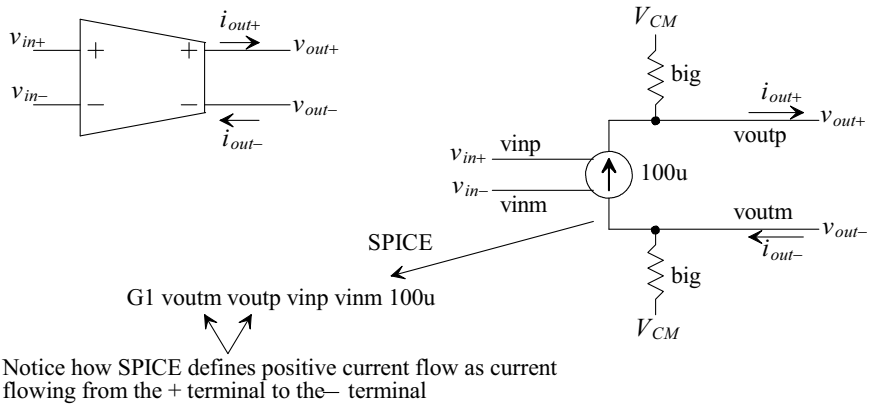


Figure 3.17 Modeling an ideal transconductor in SPICE using a voltage-controlled current source.

In order to have the same time constant, and thus pole location, as in Ex. 3.1, let's set the capacitor value, in the schematic of Fig. 3.16 to 10 pF. The value of the transconuctance, $1/g_m$, is 10k. The simulation results are shown in Fig. 3.18. As we would expect, the shape follows, exactly, that of the active-RC filter in Fig. 3.5. Also, although not shown, the phase response matches as well. ■

Common-Mode Feedback Considerations

In most OTAs the load capacitance is used for compensation. These capacitances compensate both the normal, forward, differential signal path as well as the CMFB path. Reviewing Fig. 3.15, we see that the capacitance in part (a) indeed does provide a load for differential signals. However, any signal that is common to both outputs (a common-mode signal) doesn't cause a displacement current to flow through the capacitor. Because both sides of the capacitor change at the same rate for common-mode signals, the change in voltage across the capacitor is zero. This can result in unstable CMFB

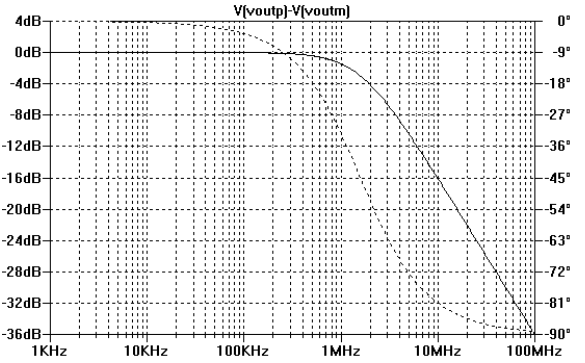


Figure 3.18 Simulation results for Ex. 35.5.

loops. Figure 3.19 shows how we would break the capacitor in Fig. 3.15 up into two components to provide the same loading for differential and common-mode signals. We can write

$$\frac{v_{out+}}{1/j\omega 2C} = i_{out+} = i_{out-} = \frac{-v_{out-}}{1/j\omega 2C} \tag{3.34}$$

$$i_{out+} = g_m(v_{in+} - v_{in-}) = i_{out-} \tag{3.35}$$

$$\frac{v_{out+} - v_{out-}}{v_{in+} - v_{in-}} = \frac{g_m}{j\omega C} \tag{3.36}$$

which is the same result as Eq. (3.30).

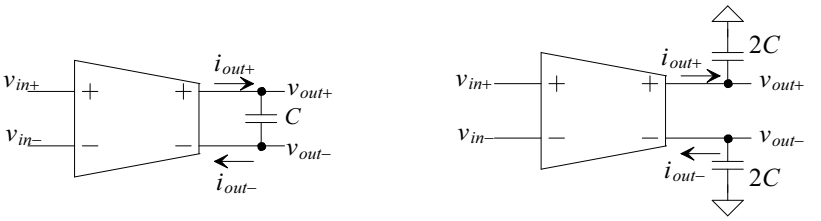


Figure 3.19 Showing how we break the capacitor up to provide a load for the CMFB circuit.

A High-Frequency Transconductor

A transconductor, Fig. 3.20, can be implemented using inverters. To increase the input common-mode range of the transconductor, the lengths of INV1 and INV2 can be increased as we discussed for the diff-amp seen in Fig. 3.15. This, again, lowers the location of the parasitic poles introduced into the transconductor's response. Note, in this circuit, that other than the power supplies and the tuning voltage, there are only two sets of nodes: the input and the output nodes. This allows the transconductor's capacitances to sum with the load capacitances and be tuned out.

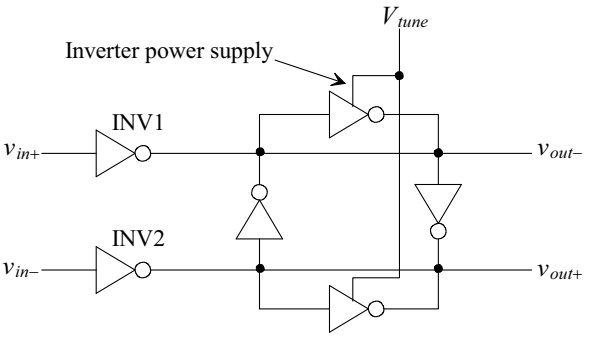


Figure 3.20 High-frequency transconductor.

3.1.5 Discrete-Time Integrators

Let's consider using a discrete-analog integrator, DAI, discussed in the last chapter to implement a first-order filter. The output of a DAI with two delaying inputs is

$$\frac{v_{out}(z)}{v_1(z)-v_2(z)} = \frac{C_I}{C_F}\cdot\frac{z^{-1}}{1-z^{-1}} \tag{3.37}$$

If we apply the filter's input to the noninverting input of the DAI and feed the output back to the subtracting input, see Fig. 3.21, we get

$$\frac{v_{out}(z)}{v_{in}(z)-v_{out}(z)} = \frac{C_I}{C_F}\cdot\frac{z^{-1}}{1-z^{-1}} \tag{3.38}$$

we can write, see Eqs. (1.62) and (1.66)

$$\left|\frac{v_{out}}{v_{in}-v_{out}}\right| = \frac{C_I}{C_F}\cdot\frac{1}{2\left|\sin\pi\frac{f}{f_s}\right|} \text{ and } \angle\frac{v_{out}}{v_{in}-v_{out}} = -\pi\frac{f}{f_s}-\frac{\pi}{2} \text{ for } 0<f<f_s \tag{3.39}$$

The sampling frequency (the frequency the discrete-time filter is clocked at) is f_s, while the filter's input frequency is labeled f. If we require $f<<f_s$ (say at least sixteen times less so $\sin\pi\frac{f}{f_s}\approx\pi\frac{f}{f_s}$), then we can rewrite Eq. (3.39) as

$$\frac{v_{out}(z)}{v_{in}(z)-v_{out}(z)} = \frac{C_I}{C_F}\cdot\frac{z^{-1}}{1-z^{-1}} \approx \frac{C_I}{C_F}\cdot\frac{f_s}{j2\pi f} = G\cdot\frac{1}{s} \tag{3.40}$$

where

$$G = \frac{C_I}{C_F}\cdot f_s = \frac{1}{C_F R_{sc}} \text{ and } f_{3dB} = \frac{G}{2\pi} \tag{3.41}$$

placing the gain of the integrator in the same form as Eqs. (3.4). The variable R_{sc} is a switched capacitor resistor

$$R_{sc} = \frac{1}{C_I\cdot f_s} = \frac{T_s}{C_I} \tag{3.42}$$

The equivalent block diagrams for first-order filters using CAIs and using the DAIs (again assuming $f<<f_s$) are compared in Fig. 3.21.

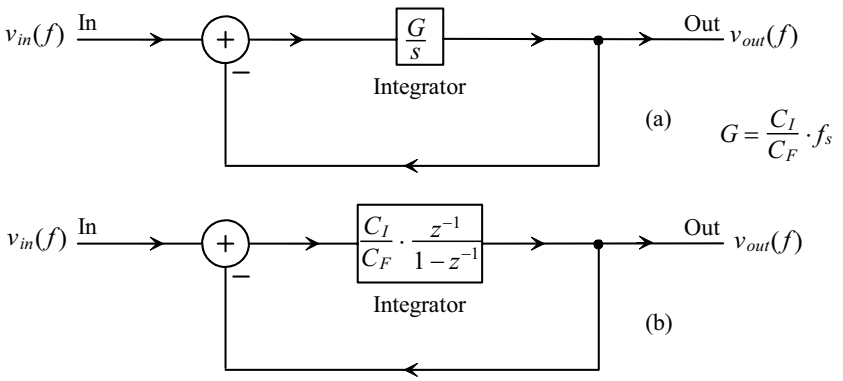


Figure 3.21 Block diagram of an integrator-based lowpass filter. (a) Continuous-time and (b) the discrete-time equivalent.

Example 3.6

Sketch the implementation of a DAI-based (switched-capacitor), first-order filter with characteristics like the one in Ex. 3.1. Use SPICE to simulate the design.

The schematic of the filter is shown in Fig. 3.22. Here we are assuming the clocking frequency of the filter is 100 MHz. If the feedback capacitance, C_F, is 10 pF, the size of the input capacitor, C_I, is then, from Eq. (3.42) and knowing R_{sc} is 10k, 1 pF. The 3 dB frequency of the filter is, once again, $1/2\pi R_{sc} C_F = 1.59$ MHz. Because of the time-domain (clock) component of the filter, we can't use an AC analysis for the SPICE simulation. Let's apply a 1 V peak-to-peak sinewave to the filter at 1.59 MHz and verify the output of the filter is 3 dB down (0.707 V peak-to-peak). The results are seen in Fig. 3.23.

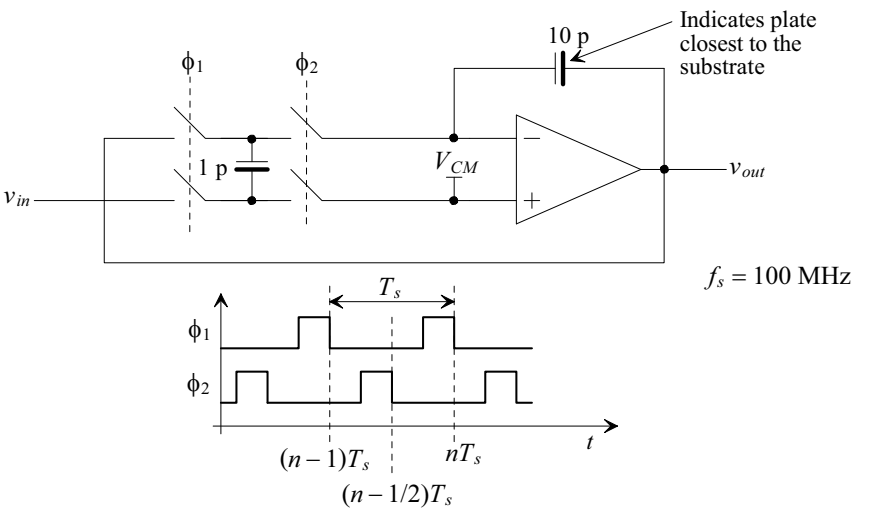


Figure 3.22 A switched capacitor, first-order filter similar to the one described in Ex. 3.1.

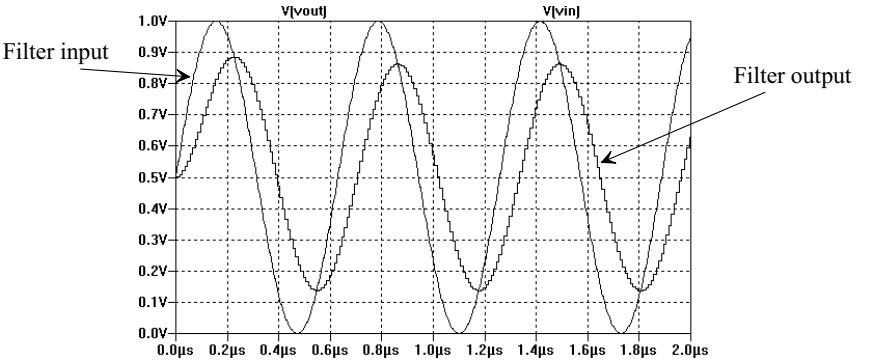


Figure 3.23 Output of the switched-capacitor circuit in Fig. 3.22.

Let's comment on the exact transfer function of the DAI in Fig. 3.22. We see in Fig. 3.22 that the output is indeed fed back to the input through a ϕ_1 controlled switch. The result is that the output, through the feedback loop, sees one clock cycle delay, z^{-1}. The output is assumed settled on the falling edge of ϕ_2 during each clock cycle. Because of this, the input, which is settled on the falling edge of ϕ_1, sees only a half clock cycle delay, $z^{-1/2}$. This means that the DAI in Fig. 3.22 really has a transfer function of

$$v_{out}(z) = \frac{C_I}{C_F} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot [v_{in}(z) \cdot z^{1/2} - v_{out}(z)] \qquad (3.43)$$

If we think of the input signal arriving a half-clock cycle earlier, then the only difference in the transfer function here, when compared to the continuous-time equivalent and assuming $f << f_s$, is a small phase difference. We can delay the input signal a full clock cycle by adding a ϕ_1 controlled switch on the output of the filter. However, because this switch may be part of the next filter section, we don't discuss this option further. ■

Example 3.7

Sketch the switched-capacitor implementation of the discrete-time lowpass (first-order) filter shown in Fig. 3.24.

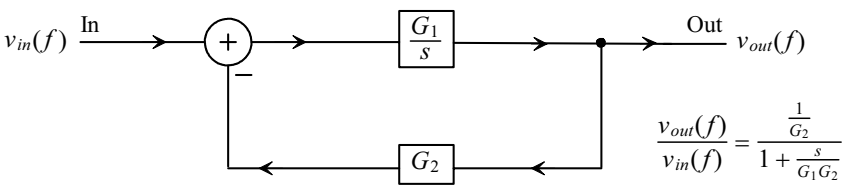


Figure 3.24 General implementation of a lowpass first-order filter.

The implementation is seen in Fig. 3.25. The coefficients are

$$G_1 = \frac{C_{I1}}{C_F} \cdot f_s \text{ and } G_2 = \frac{C_{I2}}{C_F} \cdot f_s \cdot \frac{1}{G_1} = \frac{C_{I2}}{C_{I1}} \tag{3.44}$$

The DC gain, as seen in Eq. (3.8) is set by the ratio of C_{I2} to C_{I1} $(1/G_2)$, and the filter's 3 dB frequency is

$$f_{3dB} = \frac{G_1 G_2}{2\pi} \tag{3.45}$$

Note that the DAI used in this filter has a transfer function of

$$v_{out}(z) = \frac{z^{-1}}{1 - z^{-1}} \cdot [\frac{C_{I1}}{C_F} \cdot v_{in}(z) \cdot z^{1/2} - \frac{C_{I2}}{C_F} \cdot v_{out}(z)] \tag{3.46}$$

■

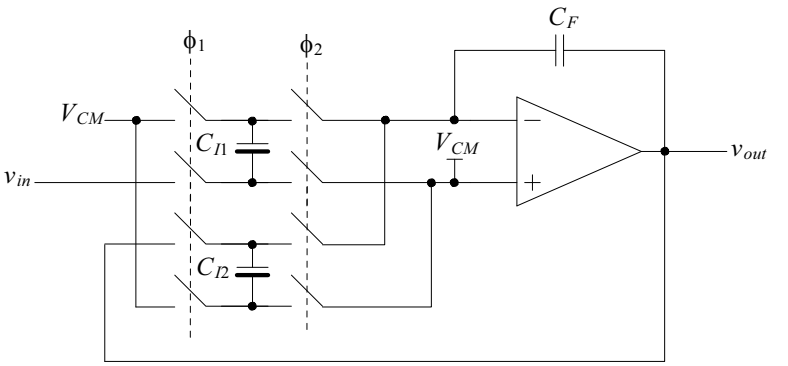


Figure 3.25 Implementation of the block diagram shown in Fig. 3.24.

The big benefit of switched-capacitor-based filters is the fact that the filters' poles and zeroes are determined by a ratio of capacitors and an external clock frequency (which is often a precise frequency set by a crystal oscillator). No tuning is needed. Varying the clocking frequency can precisely set the filter's characteristics for adaptive filtering (changing the filter's characteristics on the fly). Switched-capacitor filters with SNDRs in the 90 dB range have been attained at audio frequencies.

In the previous two examples we used ideal op-amps and didn't concern ourselves with the potential aliasing resulting from the analog sample-and-hold operation on the input of the filter. An analog antialiasing filter, AAF, (that is, not a discrete-time filter) must be used to remove the potential aliased signal prior to sampling. As with the noise-shaping modulator-based data converters we'll study later in the book, the fact that the sampling frequency, f_s, is much larger than the input frequencies of interest allows a relaxed AAF design. Indeed, the resistance of the MOSFET switches used combined with the switched input capacitance (C_I) form a lowpass filter. This filtering may serve as the switched-capacitor filter's AAF in many designs.

An Important Note

If we pause for a moment and think about the filters we have covered in this chapter we come to the realization that all require precise analog components. High-speed, wide-bandwidth op-amps and/or components with precise matching or absolute values are needed. We might argue that this would be a reason to focus our discussion on digital filtering (filters using only multipliers, delays, and adders) instead of filters using analog components. However, digital filters can't alone filter an analog waveform without first running the signal through an ADC. Further, traditional digital filters that use general-purpose multipliers at reasonable speeds can be very large (take up a significant layout area). They can be so large in fact as to not be practical in a general purpose filtering application. Special-purpose chips have been fabricated specifically for digital filtering (called digital signal processors, DSPs).

The noise-shaping topologies that use oversampling, discussed later in the book, can reduce the requirements placed on the analog components in the circuit. *Isn't it logical then to attempt to combine noise-shaping with purely digital filtering for the design of analog interfaces?* The answer is obviously, "yes"; however, as mentioned above, we have some caveats. While the resulting interface will place lower demands on the precision of the analog circuitry, we'll need to develop digital filters that don't rely on complex multipliers. The multiplications we do use should be simple, perhaps requiring an additional adder, or trivial (shift) multiplication. Also we'll need to use the digital filters to not only filter the input signal but to filter out the modulation noise present in the output of the NS modulator. Again these topics are discussed in much greater detail later in the book.

Exact Frequency Response of an Ideal Discrete-Time Filter

Figure 3.26 shows an equivalent diagram for Figs. 3.21a and 3.21b. We have replaced the ratio of capacitors, C_I/C_F, with the variable A in the figure. To determine the transfer function we can write

$$v_{out}(f) = A \cdot [v_{in}(f) - v_{out}(f)] \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{3.47}$$

or

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{Az^{-1}}{Az^{-1} + 1 - z^{-1}} = \frac{A}{z - (1 - A)} \tag{3.48}$$

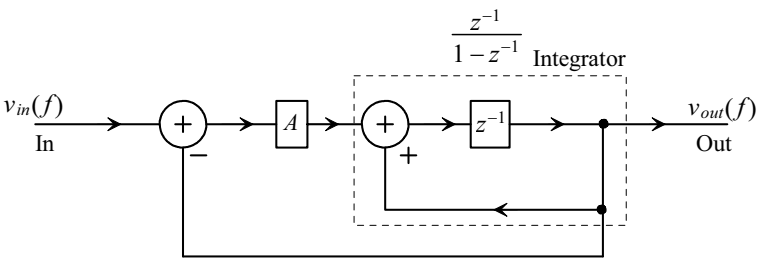


Figure 3.26 Digital block diagram of an integrator-based discrete-time lowpass filter.

Figure 3.27 shows the *z*-plane plot and magnitude response for this first-order filter. Remembering that all discrete-time filters have a periodic frequency response (a period of f_s or one complete revolution around the unit circle), we can compare this filter's response to the filters in the previous examples. To do so, let's assume $f_s = 100$ MHz and write, from Eq. (3.41),

$$f_{3dB} = \frac{Af_s}{2\pi} = 1.59 \text{ MHz} = \frac{0.1 \cdot 100 \text{ MHz}}{2\pi} \text{ that is, } A = 0.1 \qquad (3.49)$$

We can write the magnitude response of Eq. (3.48), with $z = \cos 2\pi f/f_s + j \sin 2\pi f/f_s$, as

$$\left| \frac{v_{out}}{v_{in}} \right| = \frac{A}{\sqrt{(\cos 2\pi f/f_s - 1 + A)^2 + \sin^2 2\pi f/f_s}} \qquad (3.50)$$

Figure 3.28 shows the responses of the first-order discrete-time filter. The maximum attenuation of the filter occurs at $f_s/2$ or 50 MHz here and is, from Fig. 3.27 with $A = 0.1$, 0.0526 or – 25.6 dB.

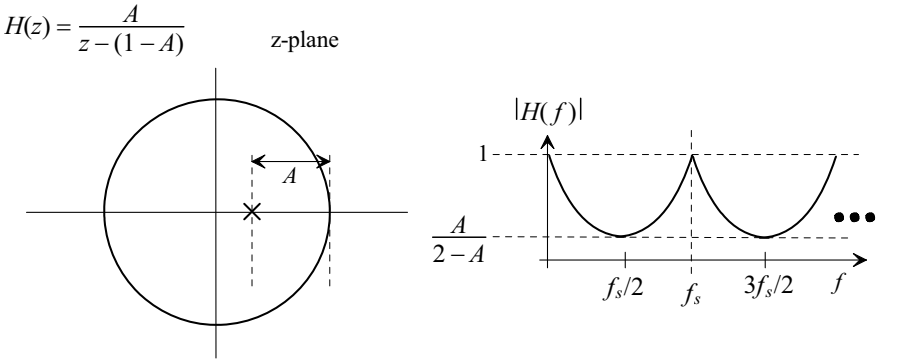


Figure 3.27 The z-plane representation and magnitude response of a first-order discrete-time filter.

3.2 Filtering Topologies

In this section we present some basic filter building blocks using integrators. Our focus is on continuous-time analog implementations of these filters.

3.2.1 The Bilinear Transfer Function

Consider the block diagram of the general first-order filter shown in Fig. 3.29. We can relate the filter's output to its input using

$$[v_{in}(f) \cdot [1 + sG_3] - G_2 \cdot v_{out}(f)] \cdot \frac{G_1}{s} = v_{out}(f) \qquad (3.51)$$

or

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{1}{G_2} \cdot \frac{1 + \frac{s}{1/G_3}}{1 + \frac{s}{G_1 G_2}} \qquad (3.52)$$

This filter's transfer function is termed "bilinear" because it is the ratio of two linear functions. Using this topology we can implement lowpass, allpass (used for phase

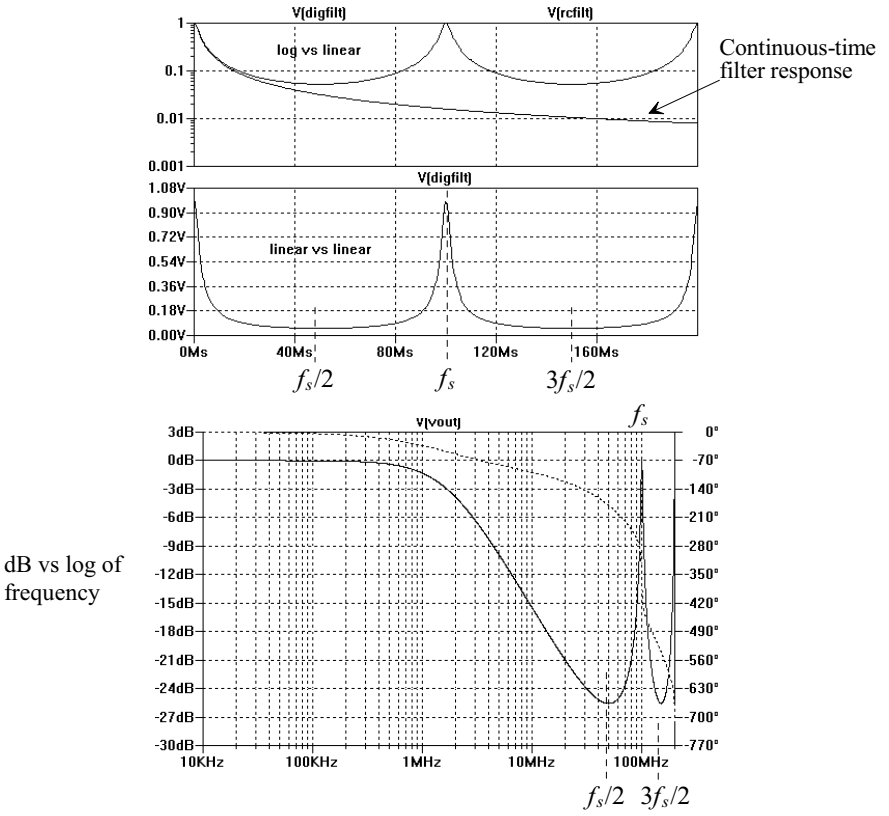


Figure 3.28 The magnitude response of the discrete-time first-order filter of Fig. 3.26 with an A of 0.1.

shifting), and highpass filters (keeping in mind that the highpass filter will ultimately change into a bandpass filter response because of the op-amp's or transconductor's high frequency rolloff). The location of the filter's pole is given by

$$f_{3dB,pole} = \frac{G_1 G_2}{2\pi} \tag{3.53}$$

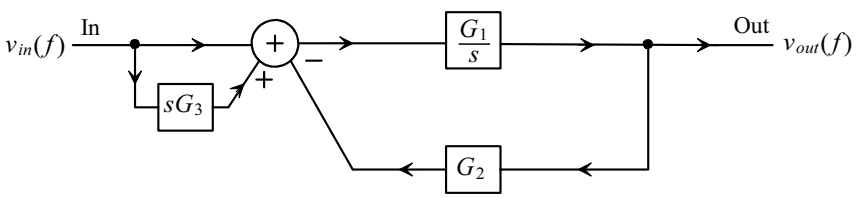


Figure 3.29 Implementation of a bilinear transfer function using an integrator.

while the filter's zero is located at

$$f_{3dB,zero} = \frac{1}{2\pi G_3} \tag{3.54}$$

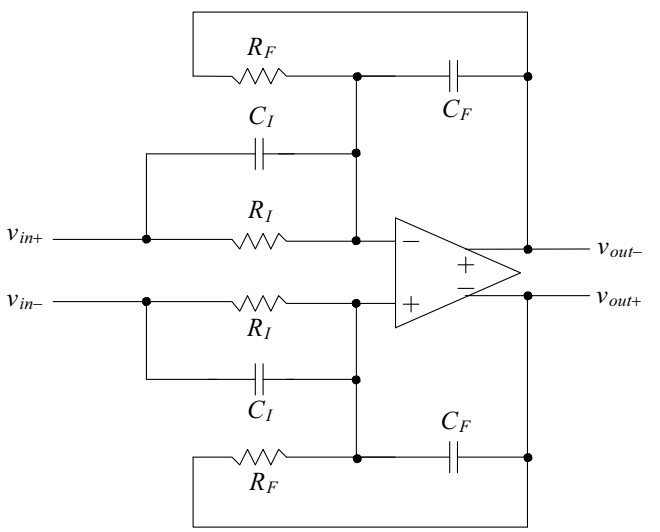
The filter's gain at DC, in all cases, is

$$A_{DC} = \frac{1}{G_2} \tag{3.55}$$

Active-RC Implementation

The active-RC implementation of the bilinear transfer function is seen in Fig. 3.30. Again, as mentioned earlier, the resulting active-RC transfer function suffers from poor repeatability from one process run to the next. The RC time constants must be tuned, on-chip, with fuses (or switches) and adding/removing resistors or capacitors. Note how the summation is implemented by changing the input/output voltages to currents. The currents are summed at the inputs of the op-amp (which remain, ideally, at the common-mode voltage, V_{CM}). This is important to note in both the active-RC and switched-capacitor implementations.

We won't discuss the implementation of the MOSFET-C-based bilinear transfer function. It should be obvious that replacing the resistors in Fig. 3.30 with MOSFETs or linearized MOSFETs (see Figs. 3.12-3.14) provides a MOSFET-C implementation.



$$G_1 = \frac{1}{R_I C_F}$$

$$G_2 = \frac{R_I}{R_F}$$

$$G_3 = R_I C_I$$

Figure 3.30 Implementation of an active-RC bilinear transfer function filter.

Transconductor-C Implementation

Figure 3.31 shows the implementation of the bilinear transfer function using transconductor stages. Again, as with the active-RC filter, signals are summed using currents. Summing the currents at the output nodes results in

$$g_{m1}(v_{in+}-v_{in-})-g_{m2}(v_{out+}-v_{out-})+\frac{v_{in+}-v_{out+}}{1/s2C_1}-\frac{v_{out+}}{1/s2C_2}=0 \tag{3.56}$$

where we know $v_{out+}=-v_{out-}$ and $v_{in+}=-v_{in-}$. It will be helpful to write

$$\frac{v_{in+}}{1/s2C_1}=\frac{2v_{in+}}{1/sC_1}=\frac{v_{in+}-v_{in-}}{1/sC_1} \tag{3.57}$$

Using this expression, we can write Eq. (3.56) as

$$(v_{out+}-v_{out-})\cdot(s(C_1+C_2)+g_{m2})=(v_{in+}-v_{in-})\cdot(g_{m1}+sC_1) \tag{3.58}$$

or finally

$$\frac{v_{out+}-v_{out-}}{v_{in+}-v_{in-}}=\frac{g_{m1}}{g_{m2}}\cdot\frac{1+\frac{s}{g_{m1}/C_1}}{1+\frac{s}{g_{m2}/(C_1+C_2)}} \tag{3.59}$$

It's important to note that when looking at this equation, the location of the pole and zero can be adjusted by changing each transconductor's g_m independently. The ability to adjust one variable in a filter's transfer function and only change the position of a single pole or zero is called *orthogonal tuning*.

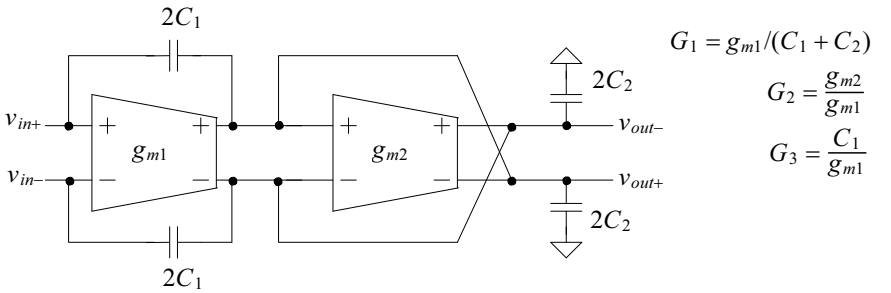


Figure 3.31 Implemention of a bilinear filter using transconductors.

Switched-Capacitor Implementation

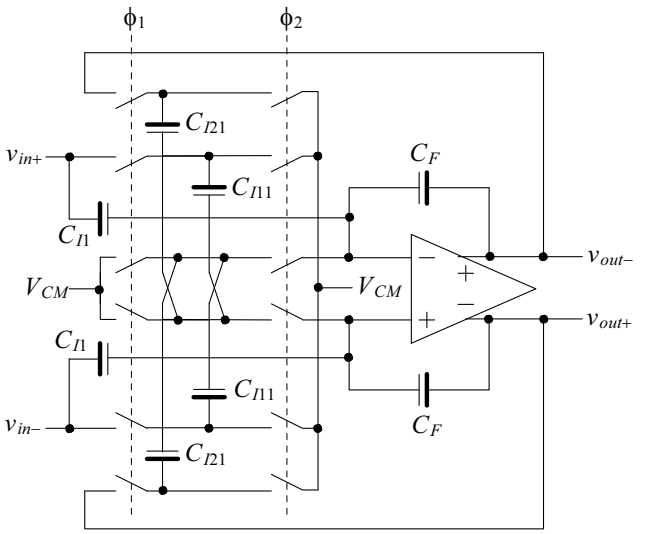
The switched-capacitor, SC, implementation of the bilinear filter is seen in Fig. 3.32. This filter is directly derived from the active-RC filter of Fig. 3.30. From Eq. (3.42) we can write

$$R_I=\frac{1}{C_{I1}\cdot f_s}\text{ and }R_F=\frac{1}{C_{I2}\cdot f_s} \tag{3.60}$$

and so

$$G_1=\frac{C_{I1}}{C_F}\cdot f_s,\ G_2=\frac{C_{I2}}{C_{I1}},\text{ and }G_3=\frac{C_{I3}}{C_{I1}\cdot f_s} \tag{3.61}$$

Note how, in this discrete-time filter, the passband gain is C_{I3}/C_F when the filter is designed for a highpass response (and the filter no longer behaves like a discrete-time filter). The gain at DC in all situations is C_{I1}/C_{I2}.



$$G_1 = \frac{C_{I11}}{C_F} \cdot f_s$$

$$G_2 = \frac{C_{I21}}{C_{I11}}$$

$$G_3 = \frac{C_{I1}}{C_{I11} \cdot f_s}$$

$$\frac{v_{out}(f)}{v_{in}(f)} = \frac{1}{G_2} \cdot \frac{1 + \frac{s}{1/G_3}}{1 + \frac{s}{G_1 G_2}}$$

Figure 3.32 Implemention of a bilinear filter using switched capacitors.

3.2.2 The Biquadratic Transfer Function

As we briefly indicated in the last section, higher order filters can be implemented by cascading first-order sections. However, because the pole and zero locations in these first-order filters are restricted to real values, the performance of these cascades is poorer than filters with complex pole and zero locations. For example, cascading two identical lowpass filters having f_{3dB} frequencies of 1.59 MHz would result in a filter that has an attenuation of 6 dB at 1.59 MHz and a – 40 dB/decade roll off at higher frequencies. Using a second-order filter, we can design a filter to have a sharper transition at 1.59 MHz so that the attenuation is less than 6 dB at 1.59 MHz (however, the roll off remains –40 dB/decade). Further, we can use these sections to implement higher order filters using Butterworth, Chebyshev, Elliptic (Cauer), or Bessel responses.

The biquadratic, or "biquad" for short, filter transfer function (a ratio of two quadratic equations) is given by

$$\frac{v_{out}}{v_{in}} = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + \left(\frac{2\pi f_0}{Q}\right) s + (2\pi f_0)^2} \tag{3.62}$$

where $2\pi f_0 = \omega_0$. The complex-conjugate poles are located at

$$p_1, p_2 = -\frac{\pi f_0}{Q} \pm \frac{1}{2}\sqrt{\left(\frac{2\pi f_0}{Q}\right)^2 - 4(2\pi f_0)^2} \tag{3.63}$$

or

$$p_1, p_2 = -\frac{\pi f_0}{Q} \pm j \cdot 2\pi f_0 \sqrt{1 - \left(\frac{1}{2Q}\right)^2} \tag{3.64}$$

In order to move toward the goal of implementing a biquad, consider the block diagram in Fig. 3.33. This block diagram is essentially the cascade of two first-order blocks (as seen in Fig. 3.29) except that instead of feeding the output of the second stage back to its input, we feed it back to the input of the first stage. We can determine the transfer function of this filter by writing

$$v_{out1} = (v_{in} + sG_3v_{in} - G_5v_{out} - G_2v_{out1}) \cdot \frac{G_1}{s} \tag{3.65}$$

or

$$v_{out1}\left(\frac{s + G_1G_2}{s}\right) = v_{in}\frac{(1 + sG_3)G_1}{s} - v_{out}\frac{G_1G_5}{s} \tag{3.66}$$

Further, we can relate v_{out1} to the output using

$$v_{out} = v_{out1}(1 + sG_6) \cdot \frac{G_4}{s} \tag{3.67}$$

Using Eq. (3.66) with Eq. (3.67) gives

$$v_{out} = \left(v_{in} \cdot \frac{(1 + sG_3)G_1}{s + G_1G_2} - v_{out}\frac{G_1G_5}{s + G_1G_2}\right) \cdot (1 + sG_6)\frac{G_4}{s} \tag{3.68}$$

or

$$v_{out}\left(1 + \frac{G_1G_4G_5(1 + sG_6)}{s^2 + sG_1G_2}\right) = v_{in}\left(\frac{(1 + sG_3)G_1(1 + sG_6)G_4}{s^2 + sG_1G_2}\right) \tag{3.69}$$

Finally, the transfer function of the biquad is given by

$$\frac{v_{out}}{v_{in}} = \frac{s^2G_1G_3G_4G_6 + s(G_1G_3G_4 + G_1G_4G_6) + G_1G_4}{s^2 + s(G_1G_2 + G_1G_4G_5G_6) + G_1G_4G_5} \tag{3.70}$$

Equating terms in Eqs. (3.62) and (3.70) gives

$$a_2 = G_1G_3G_4G_6 \tag{3.71}$$

$$a_1 = G_1G_3G_4 + G_1G_4G_6 \tag{3.72}$$

$$a_0 = G_1G_4 \tag{3.73}$$

$$\frac{2\pi f_0}{Q} = G_1G_2 + G_1G_4G_5G_6 \tag{3.74}$$

$$(2\pi f_0)^2 = G_1G_4G_5 \tag{3.75}$$

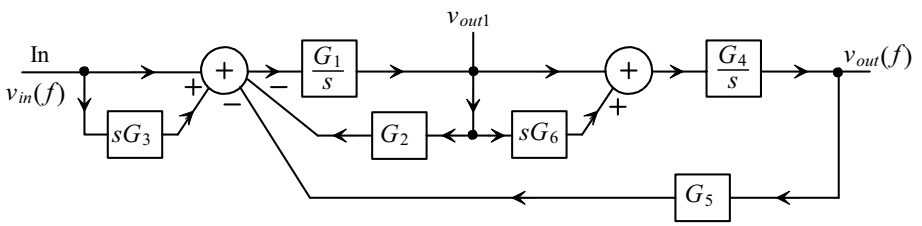
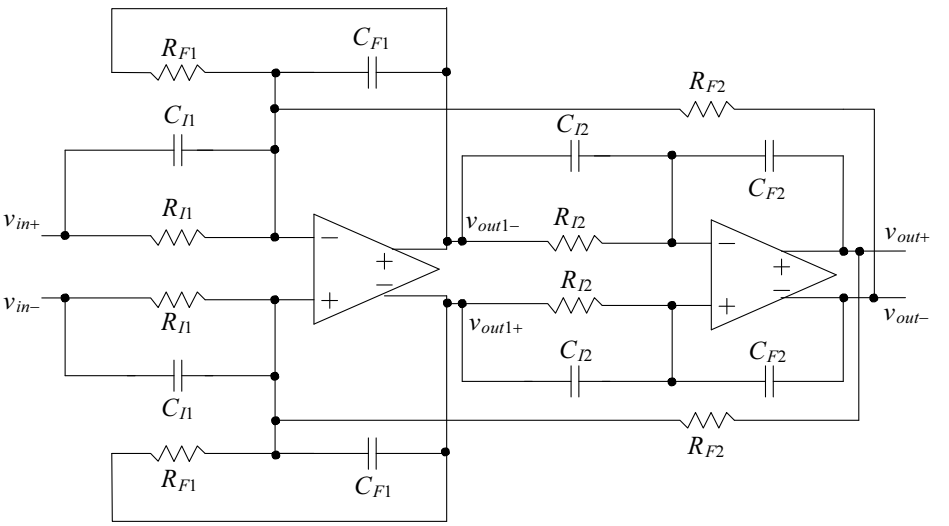


Figure 3.33 Implementation of a biquadratic transfer function using two integrators.

Active-RC Implementation

Figure 3.34 shows the active-*RC* implementation of the biquad filter along with the associated design equations. It should be noted that this is the general design schematic. If, for example, a lowpass filter needs to be implemented, the filter can be greatly simplified.



$$G_1 = \frac{1}{R_{I1}C_{F1}} \quad G_2 = \frac{R_{I1}}{R_{F1}} \quad G_3 = R_{I1}C_{I1} \quad G_4 = \frac{1}{R_{I2}C_{F2}} \quad G_5 = \frac{R_{I1}}{R_{F2}} \quad G_6 = R_{I2}C_{I2}$$

$$a_2 = \frac{C_{I1}C_{I2}}{C_{F1}C_{F2}} \qquad a_1 = \frac{C_{I1}}{R_{I2}C_{F1}C_{F2}} + \frac{C_{I2}}{R_{I1}C_{F1}C_{F2}} \qquad a_0 = \frac{1}{R_{I1}C_{F1}R_{I2}C_{F2}}$$

$$\frac{\omega_0}{Q} = \frac{2\pi f_0}{Q} = \frac{1}{R_{F1}C_{F1}} + \frac{C_{I2}}{C_{F1}R_{F2}C_{F2}} \qquad f_0 = \frac{1}{2\pi} \cdot \sqrt{\frac{1}{C_{F1}R_{I2}C_{F2}R_{F2}}}$$

Figure 3.34 Implementation of the active-RC biquadratic transfer function filter.

Figure 3.35 shows the frequency response, pole-zero locations in the s-plane, and transfer function for a second-order lowpass circuit made using an inductor (*L*), capacitor (*C*), and resistor (*R*). This LRC circuit has the same frequency response shape as a lowpass biquad filter. However, the DC gain of the LRC circuit must be unity while the DC gain of the biquad filter can be set to $a_0/(2\pi f_0)^2$. Note that if the pole quality factor, *Q*, is greater than $1/\sqrt{2}$ the response will show peaking. Setting *Q* to 0.707 results in the Butterworth or maximally flat response.

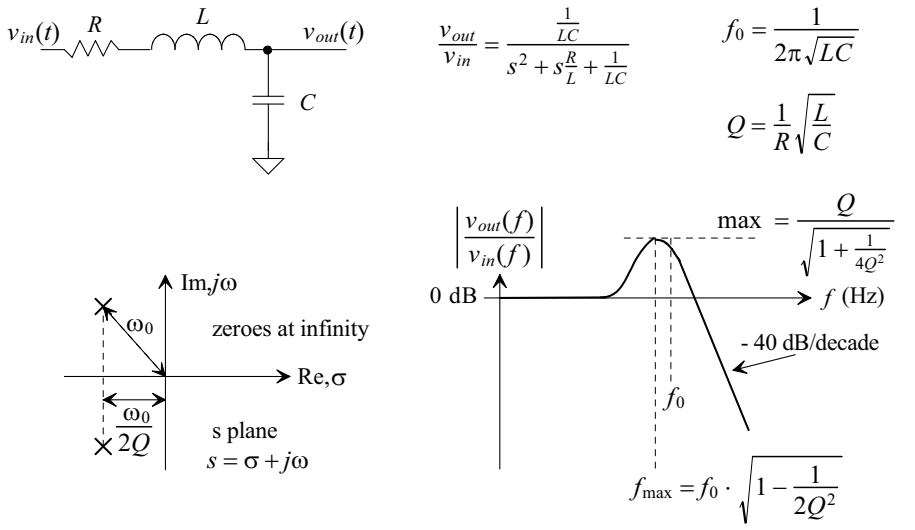


Figure 3.35 Second-order lowpass filter.

Example 3.8
Design an LRC circuit with a Q of 0.707 and a cutoff frequency (f_0) of 1.59 MHz.

From Fig. 3.35 we have two equations we need to solve

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = 1.59\ MHz \rightarrow LC = 10 \times 10^{-15} \text{ and } Q = \frac{1}{\sqrt{2}} = \frac{1}{R}\sqrt{\frac{L}{C}}$$

We can set C = 100 pF, then L = 100 μH, and R = 1.414k (definitely not practical values if the circuit is going to be purely integrated). The response of the resulting LRC circuit is shown in Fig. 3.36. Note how the cutoff frequency is set by the

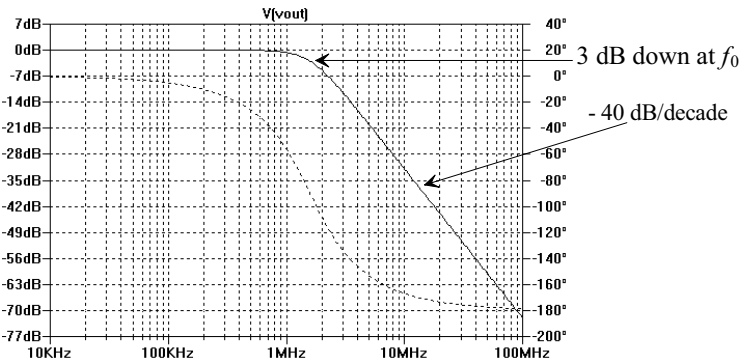


Figure 3.36 Second-order magnitude response for the circuit described in Ex. 3.8.

inductor and capacitor, while the Q of the circuit is set by all three elements (variations in the resistance having the largest effect on the circuit's Q). Higher Q indicates the poles are moving toward the imaginary axis (keeping in mind that a system with right-half plane poles is unstable [oscillates]) and more peaking, Fig. 3.37. ■

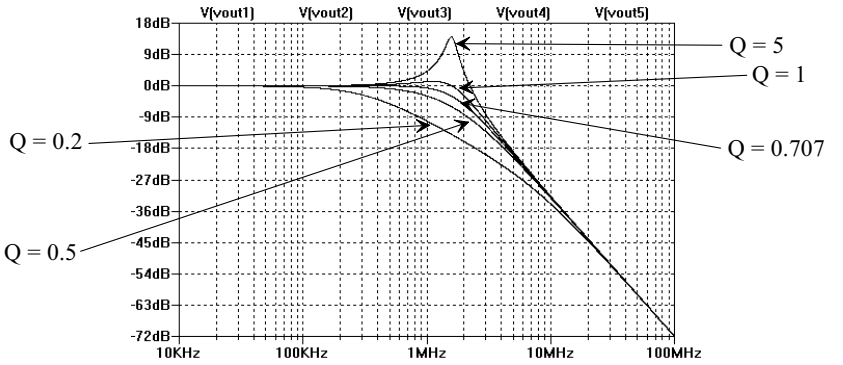


Figure 3.37 The effect of Q on the frequency response of a second-order lowpass filter.

Example 3.9
Simulate the design of an active-RC filter that has frequency characteristics similar to Fig. 3.36.

Using the basic topology of Fig. 3.34, we see that for a lowpass filter, $C_{I1} = C_{I2} = 0$ and therefore $G_3 = G_6 = 0$. Further

$$f_0 = 1.59\ MHz = \frac{1}{2\pi}\sqrt{\frac{1}{C_{F1}R_{I2}C_{F2}R_{F2}}}$$

which we shall use to set $R_{I2} = R_{F2} = 10k$ and $C_{F1} = C_{F2} = 10\,pF$. The Q of the filter is given by

$$Q = \frac{1}{\sqrt{2}} = 2\pi f_0 \cdot R_{F1}C_{F1} \rightarrow R_{F1} = 7.07\,k\Omega$$

Knowing $a_2 = a_1 = 0$, the gain at DC is $a_0/(2\pi f_0)^2$ or R_{F2}/R_{I1} $(1/G_5)$, which is 1 here. The simulation results are shown in Fig. 3.38. ■

Notice that at DC, when used in the lowpass configuration, the outputs of the first integrator, v_{out1+} and v_{out1-}, must be equal. If not, the difference is integrated by the second section. As the frequency increases, so does the difference in these voltages.

Figure 3.39 shows the second-order bandpass response. Again, as with the second-order lowpass response, the center frequency (resonant frequency) is set by the values of the inductor and capacitor. The Q of the filter indicates how narrow the bandpass response is; higher Q indicates a narrower response. Note how the response eventually rolls off at –20 dB/decade. At low frequencies the capacitor can be thought of as an open (resulting in a first-order RL circuit response), while at high frequencies the inductor can be thought of as an open (resulting in a first-order RC circuit response).

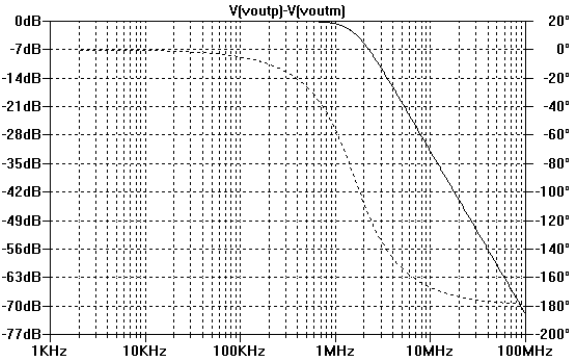


Figure 3.38 Magnitude and phase responses for the active-RC filter of Ex. 3.9.

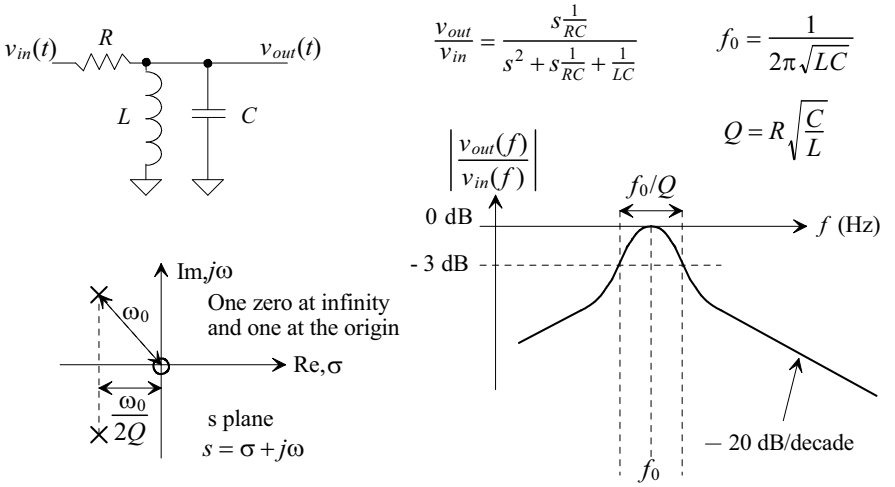


Figure 3.39 Second-order bandpass filter.

Example 3.10
Repeat Ex. 3.8 for the bandpass *LRC* circuit.

Again, we can set $C = 100$ pF and $L = 100$ μF. Solving for Q using the equation in Fig. 3.39 results in

$$Q = R\sqrt{\frac{C}{L}} = 0.707 = R\sqrt{\frac{100p}{100\mu}} \rightarrow R = 707$$

The simulation results are seen in Fig. 3.40. ■

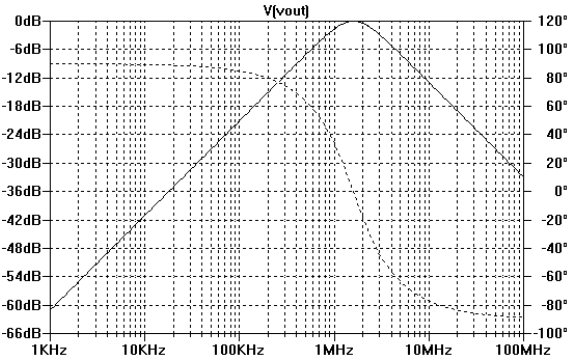


Figure 3.40 Bandpass response of a second-order circuit with a Q of 0.707.

Example 3.11
Repeat Ex. 3.10 if the Q is increased to 20.

Figure 3.41 shows the simulation results. To attain a Q of 20, we use a resistor of 20k with the inductor and capacitor values remaining unchanged. ■

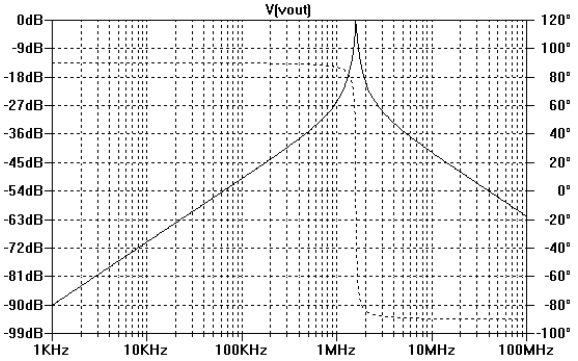


Figure 3.41 Bandpass response of a second-order circuit with a Q of 20.

Example 3.12
Use an active-RC filter to implement a filter with the response shown in Fig. 3.41.

Let's begin by writing the filter's transfer function

$$\frac{v_{out}}{v_{in}} = \frac{a_1 s}{s^2 + \left(\frac{2\pi f_0}{Q}\right)s + (2\pi f_0)^2} = \frac{a_1 s}{s^2 + \left(\frac{10\times 10^6}{20}\right)s + (10\times 10^6)^2}$$

Looking at this equation, Eq. (3.62), and Fig. 3.34 we see that $a_2 = a_0 = 0$ and so $C_{I2} = 0$ and $R_{I1} = \infty$. Further then

$$a_1 = \frac{C_{I1}}{R_{I2}C_{F1}C_{F2}} \qquad f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{C_{F1}R_{I2}C_{F2}R_{F2}}} = 1.59\text{ MHz}$$

$$\frac{2\pi f_0}{Q} = \frac{2\pi \cdot 1.59\text{ MHz}}{20} = \frac{1}{R_{F1}C_{F1}}$$

The passband gain (the maximum gain) occurs at f_0 and is calculated by replacing s in the transfer function above with $j2\pi f_0$. It is given by

$$A_{passband} = \frac{a_1 Q}{2\pi f_0}$$

If, again, we set $C_{F1} = C_{F2} = 10$ pF and $R_{I2} = R_{F2} = 10$k, we get an f_0 of 1.59 MHz. Further then, with a Q of 20, we can set R_{F1} to 200k. Finally, setting the passband gain to unity results in

$$a_1 = \frac{2\pi f_0}{Q} = \frac{C_{I1}}{R_{I2}C_{F1}C_{F2}} \rightarrow C_{I1} = 0.5\,\text{pF}$$

While these values do result in a biquad with the shape seen in Fig. 3.41, the values are not practical. Redoing the calculations while trying to minimize the component spread gives another possible solution: R_{I2} = 100k, C_{F1} = 20p, R_{F1} = 100k, C_{F2} = 5p, C_{I1} = 5p, and R_{F2} = 1k. The simulation results are seen in Fig. 3.42. ■

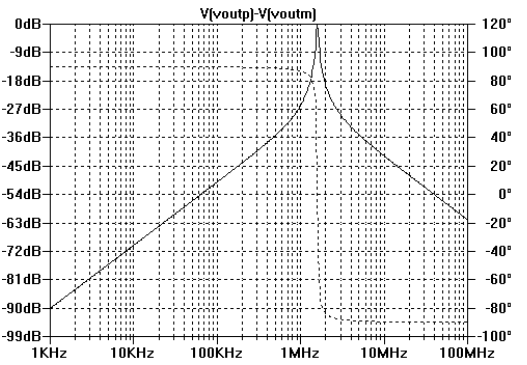


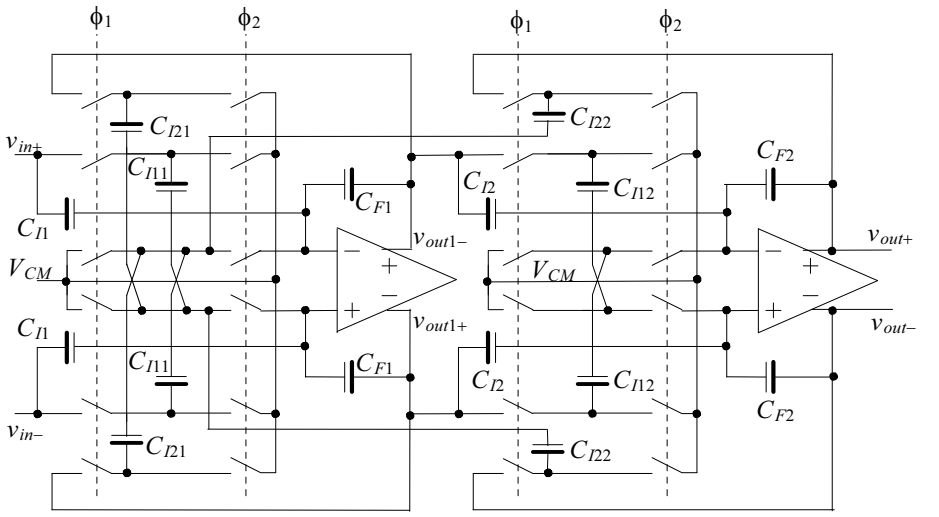
Figure 3.42 Outputs of the biquad of Ex. 35.12 using active-RC elements.

Switched-Capacitor Implementation

The switched-capacitor implementation of the biquad circuit is shown in Fig. 3.43. Note how this circuit is a simple translation of the active-RC circuit of Fig. 3.34. Again, if the filter designed using this section has a lowpass or bandpass response, it can be simplified. For example, from Figs. 3.35 and 3.39 (the implementation of lowpass and bandpass filters), we see that a_2 is zero. This indicates that G_6 *can be set to zero* (removing C_{I2} in Figs. 3.34 or 3.43). The resulting second-order filter response can be written as

$$\frac{v_{out}}{v_{in}} = \frac{a_1 s + a_0}{s^2 + \left(\frac{2\pi f_0}{Q}\right)s + (2\pi f_0)} = \frac{sG_1G_3G_4 + G_1G_4}{s^2 + sG_1G_2 + G_1G_4G_5} \qquad (3.76)$$

Technically, the filter is no longer biquadratic, so we will refer to it as a second-order filter.



$$G_1 = \frac{C_{I11}}{C_{F1}} \cdot f_s \quad G_2 = \frac{C_{I21}}{C_{I11}} \quad G_3 = \frac{C_{I1}}{C_{I11} \cdot f_s} \quad G_4 = \frac{C_{I12}}{C_{F2}} \cdot f_s \quad G_5 = \frac{C_{I22}}{C_{I11}} \quad G_6 = \frac{C_{I2}}{C_{I12} \cdot f_s}$$

Figure 3.43 Implementing a biquad filter using switched capacitors.

The biquad in Fig. 3.43 can look confusing until we start to dissect it. If we understand the topology of Fig. 3.32, we see that the switched-capacitor biquad is nothing more than two bilinear filters connected in cascade. The only difference is that the switched capacitance, C_{I22}, is fed back to the input of the first op-amp to simulate the feedback resistance, R_{F2}, in Fig. 3.34. This circuit, for the general lowpass or bandpass filter implementation, gets much simpler when the unused components are removed.

High Q

We have a major concern alluded to in Ex. 3.12 when using either of the topologies of Fig. 3.34 or 3.43 with a large Q. As we saw in this example the capacitor values were within a factor of 4 of each other (20p and 5p) but the resistors used were two orders of magnitude different (100k and 1k). This large difference can be traced to, again assuming $G_6 = 0$,

$$\frac{2\pi f_0}{Q} = G_1 G_2 \text{ and } 2\pi f_0 = \sqrt{G_1 G_4 G_5} \text{ or } Q = \frac{\sqrt{G_4 G_5}}{\sqrt{G_1}\, G_2} = \sqrt{\frac{C_{F1}}{R_{I2} C_{F2} R_{F2}}} \cdot R_{F1} \tag{3.77}$$

This equation shows that R_{F1} has the largest direct dependence on Q. Using a large value of R_{F1} results in a smaller feedback signal (a smaller amount of current is fed back to the input of the first op-amp). In other words G_2 in Fig. 3.33 is small.

In order to minimize the amount of signal, v_{out1}, fed back and summed with the input signal, while at the same time forcing the components to have similar values, consider the modified, from Fig. 3.33, biquad block diagram shown in Fig. 3.44. All we have done here is added a separate signal path in parallel with the G_2 path. Instead of subtracting, though, we are now adding the signal to the input summing block. Equation (3.70) can be rewritten, assuming G_6 is zero (a bandpass or lowpass response), as

$$\frac{v_{out}}{v_{in}} = \frac{s(G_1G_3G_4) + G_1G_4}{s^2 + sG_1(G_2 - G_{2Q}) + G_1G_4G_5} \tag{3.78}$$

or, equating the coefficient of s in the denominator of this equation with the coefficient of s in the denominator of Eq. (3.62), results in

$$\frac{2\pi f_0}{Q} = G_1(G_2 - G_{2Q}) \tag{3.79}$$

The implementation of the "high-Q" biquad is seen in Fig. 3.45 (with G_6 included). The additional gain from the figure is

$$G_{2Q} = \frac{R_{I1}}{R_{F1}\frac{Q}{Q-1}} = G_2 \cdot \frac{Q-1}{Q} \tag{3.80}$$

Rewriting Eq. (3.79) results in

$$\frac{2\pi f_0}{Q} = G_1G_2\left(1 - \frac{Q-1}{Q}\right) = \frac{G_1G_2}{Q} \tag{3.81}$$

Let's use this result in the following example.

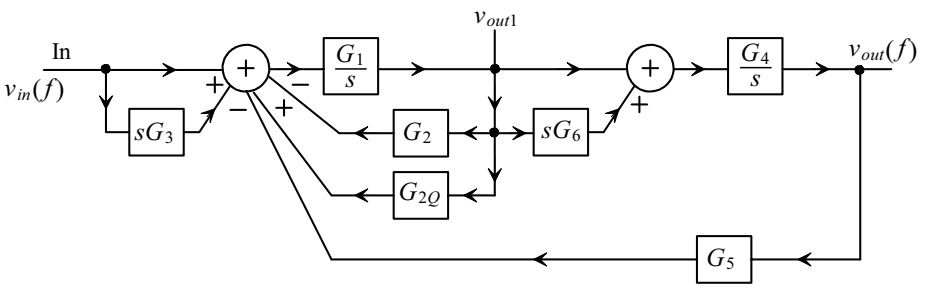


Figure 3.44 Implementation of a "high-Q" biquadratic transfer function.

Example 3.13
Repeat Ex. 3.12 using the high-Q circuit of Fig. 3.45.

The passband gain is 1 so we know that

$$a_1 = \frac{2\pi f_0}{Q} = \overbrace{G_1G_3G_4}^{a_1} = G_1(G_2 - G_{2Q}) = \frac{G_1G_2}{Q}$$

or $2\pi f_0 = 10 \times 10^6 = G_1G_2 = 1/R_{F1}C_{F1}$. We also know that

$$G_1 G_3 G_4 = \frac{C_{I1}}{C_{F1} R_{I2} C_{F2}} = G_1 (G_2 - G_{2Q}) = \frac{1}{C_{F1} R_{F1}} \cdot \frac{1}{Q}$$

and

$$2\pi f_0 = 10 \times 10^6 = \sqrt{\frac{1}{C_{F1} R_{I2} C_{F2} R_{F2}}}$$

In an attempt to minimize component spread let's set R_{F1} to 5k, R_{I2} to 20k, C_{I1} to 4p, C_{F2} to 20p, C_{F1} = 20p, R_{F2} = 1.25k, and finally R_{F1Q} = 5.25k (roughly). The simulation results and schematic are shown in Fig. 3.46. ■

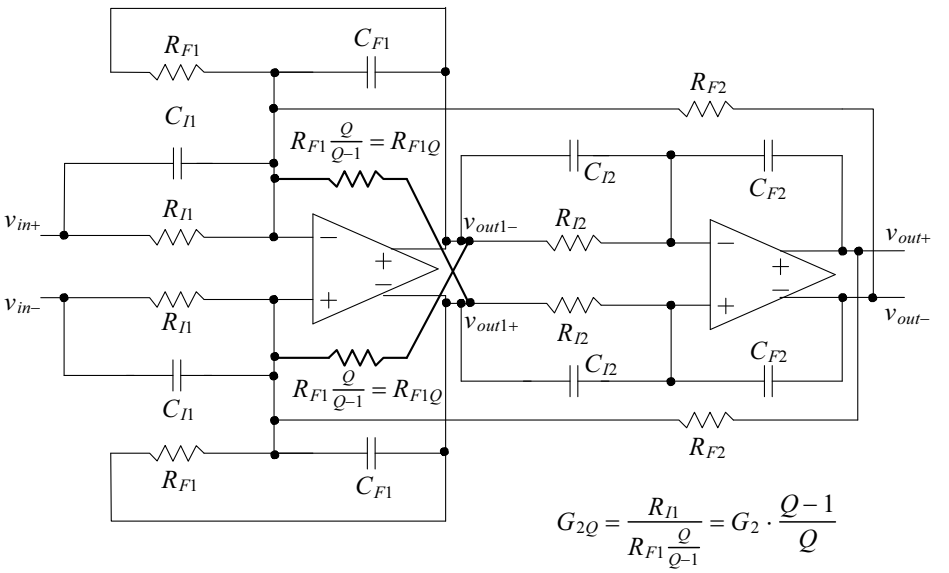


Figure 3.45 Implementation of the "high-Q" active-RC biquadratic transfer function filter. The bold lines indicate the added components.

Example 3.14

Repeat Ex. 3.13 using a switched-capacitor implementation. Assume that the filter is clocked at 100 MHz.

To implement the filter, we need to replace the resistors in Fig. 3.46 with switched capacitors. However, we notice in the gain equations that the resistors are all ratios of capacitors. This means we can reduce the size of the filter by scaling the values in Fig. 3.46. In order to do this let's divide all capacitors by 10 and multiply all resistors by 10. Therefore, we can write C_{I1} = 0.4p, C_{F1} = 2p, and C_{F2} = 2p. The resistors can be calculated using

$$R_{F1} = \frac{1}{C_{I21} \cdot f_s} = 50k \rightarrow C_{I21} = 0.2p$$

$$R_{F1Q} = \frac{1}{C_{I21Q} \cdot f_s} = 52.5k \rightarrow C_{I21Q} = 0.190p$$

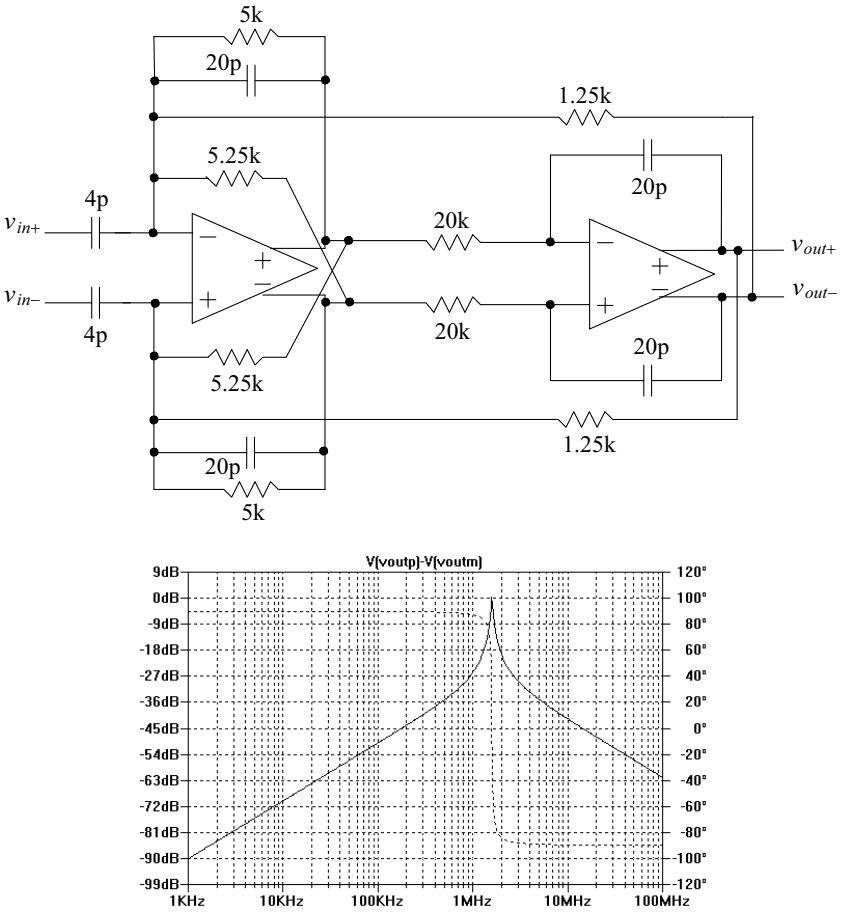


Figure 3.46 Bandpass filter discussed in Ex. 3.13.

$$R_{I2} = \frac{1}{C_{I12} \cdot f_s} = 200k \rightarrow C_{I12} = 0.05p \text{ (!)}$$

$$R_{F2} = \frac{1}{C_{I22} \cdot f_s} = 12.5k \rightarrow C_{I22} = 0.8p$$

Looking at the value of C_{I12}, we see it may be too small. Let's change its scale factor from 10 to 4. This means

$$R_{I2} = \frac{1}{C_{I12} \cdot f_s} = 80k \rightarrow C_{I12} = 0.125p$$

We have to scale C_{F2} as well (so that G_4 remains constant). Now C_{F2} = 5 pF.

Figure 3.47 shows the implementation of the filter. Note how easy it was to implement the high-Q circuitry. All we did was add two capacitors to the circuit. Also note how the circuit is simplified after removing the unused components (R_{I1} and C_{I2}).

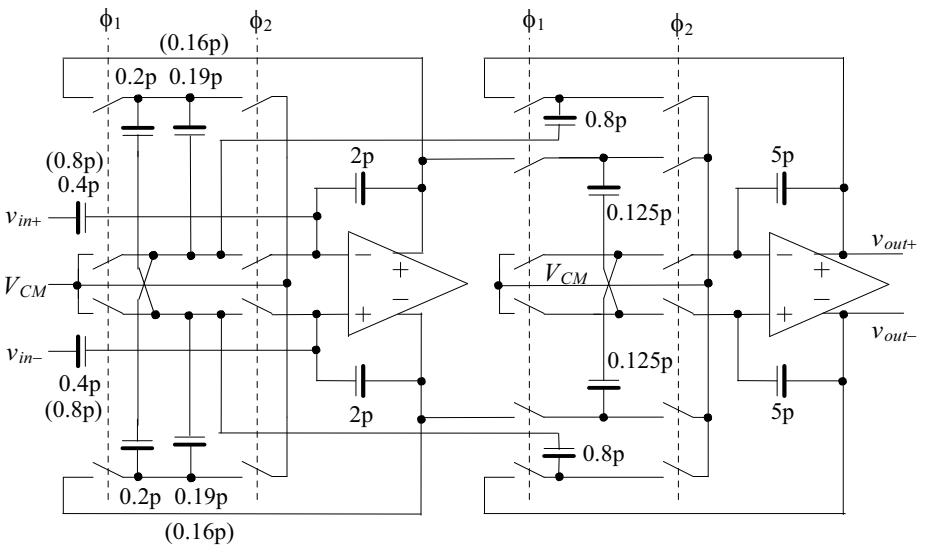


Figure 3.47 Switched-capacitor implementation of a high-Q filter; see Ex. 35.14.

Again, as in Ex. 3.6, because this circuit can only be simulated using a transient analysis, we will input a sinewave at a known frequency and verify that we get the correct output. Looking at Fig. 3.46, we see that if we apply a 1 V signal to the filter at 1.59 MHz we should get a 1 V signal out at 1.59 MHz. However, as seen in Fig. 3.48, the filter is unstable and oscillates. Using simulations it's easy to show that even if we ground the inputs of the filter, the outputs oscillate at f_0 (1.59 MHz). To understand why, remember in Fig. 3.39 that as the Q of the bandpass filter is increased, the poles move closer to the right-half plane. If, for some reason, the poles move into the right-half plane, the filter will become an oscillator (unstable). It's important to remember that when we designed the filter we approximated our discrete-time variable z as $1+\frac{s}{f_s}=1+j\frac{2\pi f}{f_s}$ (when $f << f_s$ $\cos\frac{2\pi f}{f_s}\approx 1$ and $\sin\frac{2\pi f}{f_s}\approx\frac{2\pi f}{f_s}$). We could be more exact and write

$$z=e^{j\frac{2\pi f}{f_s}}=\cos\frac{2\pi f}{f_s}+j\sin\frac{2\pi f}{f_s} \tag{3.82}$$

which clearly will not follow $1+\frac{2\pi f}{f_s}$ for frequencies f approaching the sampling frequency f_s. As we discussed in Ch. 2, sampled signals will have spectral content in excess of the sampling frequency. Practically, the spectral content is limited by the combination of the switches "on" resistance and the capacitors in the circuit.

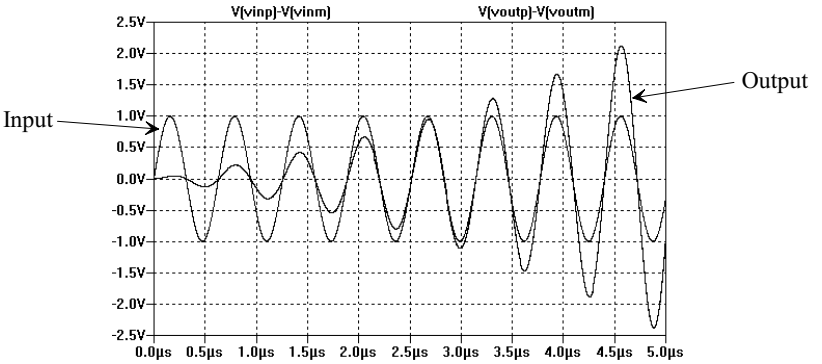


Figure 3.48 Output of the filter in Fig. 3.47 showing instability.

As f gets larger, the cosine term will decrease from one, causing the real portion to get smaller. A decrease in the real component, as seen in the complex plane in Fig. 3.39, causes the pole to move closer to the right-half plane (causing the Q to increase).

Practically, the maximum Q we can design for (but not attain) is in the neighborhood of 5. If we redesign the biquad of Fig. 3.47 to have a Q of 5, we see that all we need to change is C_{I1} (from 0.4p to 0.8p) and C_{I21Q} (from 0.19p to 0.16p). The simulation results are seen in Fig. 3.49. In this figure, we adjusted the input frequency until we reached a 3 dB point (the filter's center frequency was 1.59 MHz, as expected). This occurred at 1.52 MHz and 1.66 MHz. The Q of the circuit is not 5, but is, from Fig. 3.39, 1.59/(1.66 – 1.52) or 11.36. ■

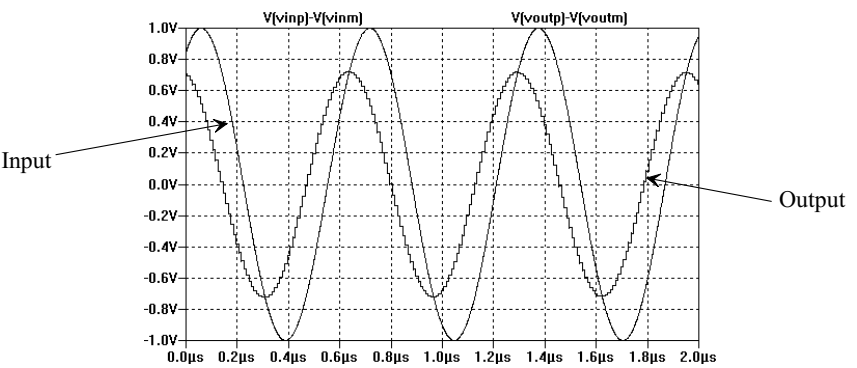


Figure 3.49 Output of the filter in Fig. 3.47 after lowering the Q to maintain stability.

Q Peaking and Instability

While it would appear the active-RC circuit is the best choice for high-Q filter implementations, we must remember that the discussion neglected the effects of the finite

gain-bandwidth product (f_{un}) of the op-amps. We can model these effects by replacing the ideal integrator gain of $1/s$ with

$$\frac{1}{s} \rightarrow \frac{1}{s\left(1+\frac{s}{2\pi f_{un}}\right)} \tag{3.83}$$

Using this result, we can rewrite the pole locations of Eq. (3.62) (see Eqs. [3.63] and [3.64]) as

$$\frac{1}{\left(s\left(1+\frac{s}{2\pi f_{un}}\right)+p_1\right)} \cdot \frac{1}{\left(s\left(1+\frac{s}{2\pi f_{un}}\right)+p_2\right)} \tag{3.84}$$

or, looking at a single term,

$$s\left(1+\frac{s}{2\pi f_{un}}\right)+p_1 = s+p_1-\overbrace{\frac{(2\pi f)^2}{2\pi f_{un}}}^{\text{Unwanted}} \tag{3.85}$$

This subtraction results in a shift in the pole toward the right-half plane, increasing the Q of the circuit; Fig. 3.50. Reviewing Eq. (3.64), we can subtract the unwanted term in Eq. (3.85) to estimate the shift in the Q or

$$\frac{\pi f_0}{Q}-\frac{(2\pi f)^2}{2\pi f_{un}} \text{ or at } f=f_0 \text{ we can write } \pi f_0\left(\frac{1}{Q}-\frac{2f_0}{f_{un}}\right) \tag{3.86}$$

The shifted Q is then

$$\frac{1}{Q_{shift}}=\frac{1}{Q}-\frac{2f_0}{f_{un}} \rightarrow Q_{shift}=\frac{Q}{1-\frac{Q2f_0}{f_{un}}} \tag{3.87}$$

So, for the filter Q to remain finite, we require

$$\frac{Q2f_0}{f_{un}} << 1 \tag{3.88}$$

Let's use this result in the following example.

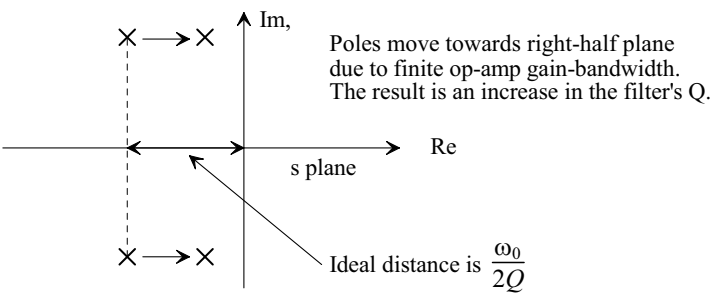


Figure 3.50 Showing Q peaking resulting from the op-amp finite gain bandwidth product.

Example 3.15
Resimulate the filter in Ex. 3.13 using op-amps that have an f_{un} of 100 MHz.

The center frequency, f_0, of this filter is 1.59 MHz and the Q is 20. Using Eqs. (3.87) and (3.88), we can estimate the increase in Q due to op-amp finite gain-bandwidth product as

$$\frac{Q2f_0}{f_{un}} = \frac{20 \cdot 2 \cdot 1.59}{100} = 0.636 \rightarrow Q_{shift} = 55$$

Practically, this is too high of a Q (the poles are too close to the right-half plane), and the filter will be unstable (noise in the circuit, or simulation noise in the simulation, will push the poles into the right-half plane). Figure 3.51 shows the simulation results (see also Ex. 3.4). The inputs to the filter are grounded. The unstable oscillation frequency is close to the ideal, f_0, but is shifted by a small amount. ■

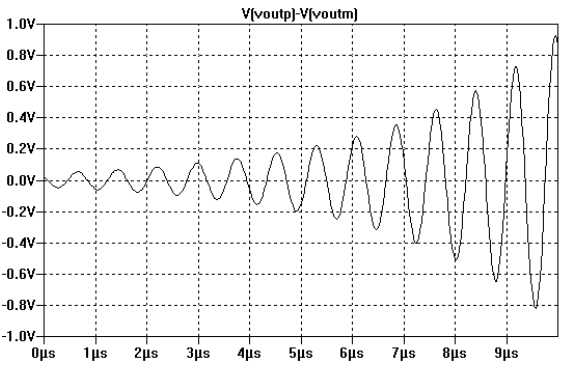


Figure 3.51 Showing how the filter of Ex. 3.13 becomes unstable due to finite op-amp bandwidth.

Transconductor-C Implementation

Let's redraw the bilinear filter in Fig. 3.31 as seen in Fig. 3.52. We redraw it like this to show how the feedback gain, G_2, is implemented. In the block diagram of the biquad filter shown in Fig. 3.43, we used a similar scheme to implement the feedback gain, G_5. Figure 3.53 shows the implementation of a biquad filter using transconductors where we have drawn it so that the transconductors appear to be connected in series. This topology can be redrawn so that it looks similar to Fig. 3.52 (showing a direct correspondence between it and Fig. 3.43). Note that we could have drawn the schematic without the crossing wires if we switched the output polarity of two of the transconductors (that is, put the minus output on the top of the output instead of the plus output).

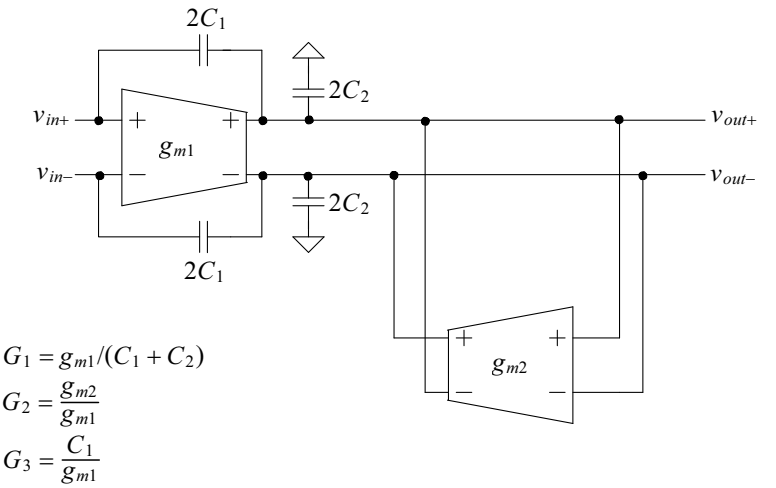


Figure 3.52 Redrawing the bilinear filter shown in Fig. 3.31.

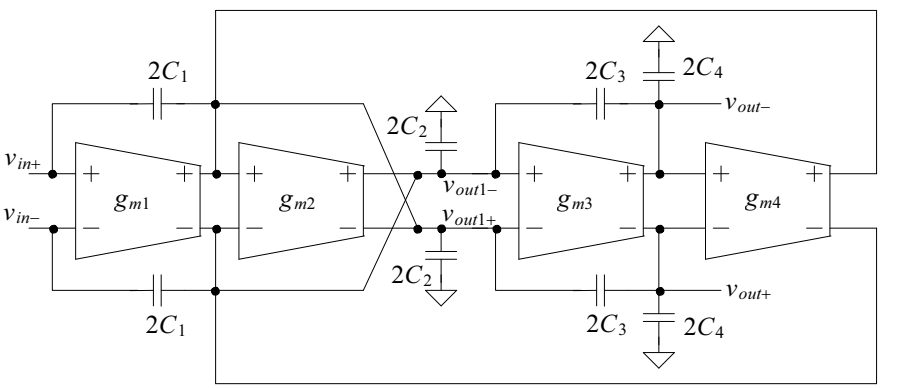


Figure 3.53 Implementing a biquadratic filter using transconductors.

ADDITIONAL READING

[1] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, Third Edition, McGraw-Hill, 2003. ISBN 978-0071207034

[2] R. Schaumann and M. E. Van Valkenburg, *Design of Analog Filters*, Oxford University Press, 2001. ISBN 978-0195118773

[3] P. R. Gray, D. A. Hodges, and R. W. Brodersen (eds.), *Analog MOS Integrated Circuits*, Wiley-IEEE, 1980. ISBN 0-471-08964-8

[4] P. R. Gray, B. A. Wooley, and R. W. Brodersen (eds.), *Analog MOS Integrated Circuits II*, Wiley-IEEE, 1989. ISBN 0-87942-246-7

[5] P. A. Lynn, *An Introduction to the Analysis and Processing of Signals*, Hemisphere Publishing Corporation, 1989. ISBN 0-89116-981-4

[6] Y. P. Tsividis and J. O. Voorman (eds.), *Integrated Continuous-Time Filters: Principles, Design, and Applications*, Wiley-IEEE, 1993. ISBN 0-7803-0425-X

[7] B. Nauta, *Analog CMOS Filters for Very High Frequencies*, Kluwer Academic Publishers, 1993. ISBN 0-7923-9272-8

QUESTIONS

3.1 Resketch Fig. 3.2 for the following circuit.

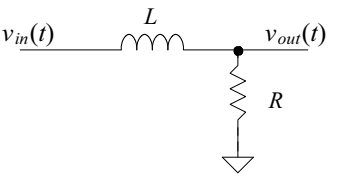


Figure 3.54 First-order lowpass filter using an inductor and a resistor.

3.2 Show that Eq. (3.6) is still valid if the circuit's inputs and outputs are referenced to the common-mode voltage, V_{CM}. (The op-amp inputs should also be at V_{CM}.)

3.3 Sketch the implementation of a first-order lowpass filter using a CAI with a 3 dB frequency of 10 MHz and a DC gain of 6 dB. Simulate your design to verify it works as expected.

3.4 Plot, in the complex plane, the ideal pole location and the actual pole locations due to finite op-amp unity gain frequency for the filter described in Ex. 3.4.

3.5 Plot Eq. (2.59) of the last chapter using SPICE and the op-amp model shown in Fig. 3.8.

3.6 Suppose an antialiasing filter was required for a 12-bit data converter. Further assume the filter is to be implemented using an active-RC topology. If *VDD* = 1.0 V, estimate the minimum value of the integration capacitor that should be used, assuming the filter's noise performance is dominated by thermal noise. Is it wise, for 12-bit system performance, to design the filter so that its SNR is equal to the SNR of the data converter?

3.7 Repeat question 3.6 if the op-amp used in the filter has a linear output swing of 80% of the power supply voltage.

3.8 Derive the transfer function for the filter shown in Fig. 3.16 if the transconductors have different g_ms. Sketch the block diagram, similar to the one seen in Fig. 3.6, for the filter.

3.9 Derive the transfer function for the following first-order transconductor filter.

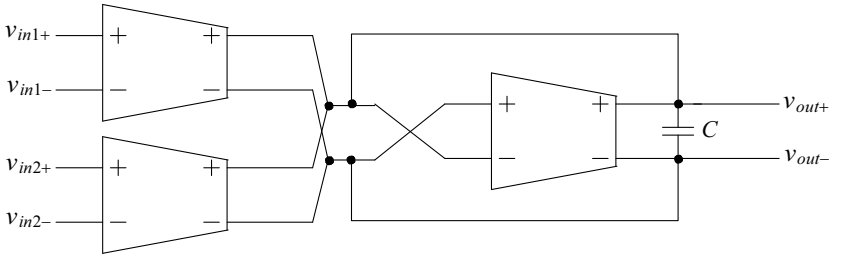


Figure 3.55 A first-order filter with two inputs.

3.10 Show the derivation details that result in Eqs. (3.44) and (3.46).

3.11 Show the details of how the gains, G, are derived in Fig. 3.30.

3.12 Is it possible to tune the gain, Q, and cutoff frequency of the lowpass biquad independently? If so, how? Give examples using the simulation netlist used to generate Fig. 3.38.

3.13 What happens to the poles in the biquadratic equation, Eq. (3.62), if the Q is less than 0.5? (Hint: The filter behaves like the cascade of two first-order filters.) Is the $f_{\max}$ equation in Fig. 3.35 valid?

3.14 Compare the size of the elements used in Exs. 3.8 and 3.9. Is there a benefit to using an active element for monolithic implementation?

3.15 Show, using the simulations from Ex. 3.14, that increasing the switch resistance, and thus the spectral content present in a switched capacitor circuit, can help to stabilize high-Q switched-capacitor bandpass filters.

3.16 Redesign and simulate the operation of the filter discussed in Ex. 3.14, with a Q of 5, while trying to minimize the difference between C_{I1} and C_{F2}. Suggest a possible modification to the filter topology (similar to how we add G_{2Q} in Fig. 3.45) to reduce this component spread.

3.17 Show how to derive the transfer function of the transconductor-C biquad filter seen in Fig. 3.53. Can this filter be orthogonally tuned? If so, how?

3.18 Repeat Ex. 3.9 using the transconductor-based biquad.

3.19 How would a "high-Q" biquad be implemented using transconductors? Repeat Ex. 3.12 using the transconductor-based biquad.

3.20 Show, using biquad sections, how the lowpass ladder filter seen in Fig. 3.56 can be implemented.

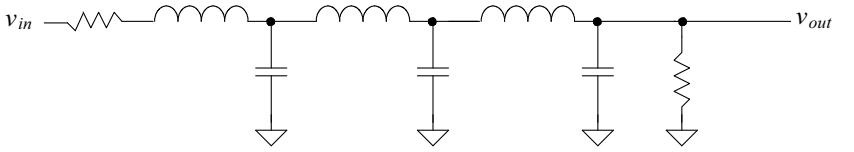


Figure 3.56 Implementing a ladder filter using biquads, see problem 3.20.