Chapter

6

Data Converter Design Basics

Mixed-signal design is powerful because it combines digital-signal processing (DSP) with analog circuit design. Using DSP, as we'll show in this chapter, reduces the required precision of the analog circuits. Perhaps a different, yet appropriate, name for this chapter is "Analog Design without using Analog Components!"

In the past five chapters, we covered topics we'll frequently use in the design of mixed-signal circuits. For example, Fig. 6.1 shows how we'll design an analog-to-digital converter (ADC) using mixed-signal circuit design techniques. Our analog input is passed through an anti-aliasing filter (AAF) to a noise-shaping (NS) modulator. The noise shaping modulator, as discussed in Sec. 5.4, uses a low-resolution quantizer (a fancy name for an ADC with 1 to a few bits resolution, like the comparator seen in Fig. 5.1) in a feedback loop to get a running average of the analog input signal. The desired digital output is extracted using a moving average filter, the lowpass filters in Sec. 4.2, and decimated. In simple words, the modulator's digital output signal is averaged to get a representation of the analog input signal. Figure 6.2 shows example modulator outputs for various DC input signals.

Note that this type of data converter is often called an *oversampled* ADC since the sampling frequency, f_s, must be much larger than the input frequencies of interest. We'll also see that these types of data converters are called *noise-shaping* ADCs or, depending on the topology used, *delta-sigma* (or *sigma-delta*) ADCs (these names are discussed in greater detail later).

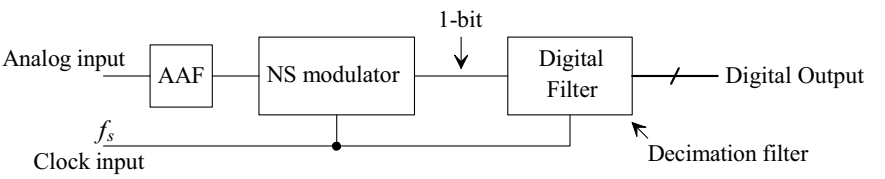


Figure 6.1 An ADC using a NS modulator and digital filter.

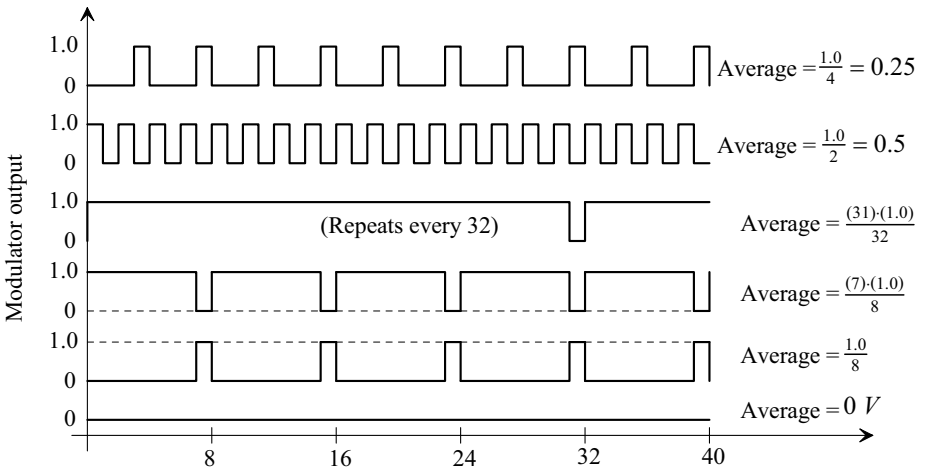


Figure 6.2 Modulator outputs and their corresponding DC averages.

The One-Bit ADC and DAC

In this chapter we'll use, exclusively, a one-bit ADC and DAC. To understand why, let's review Fig. 5.28 and 5.32. In all cases, unless the spacing of the codes is perfect in these data converters, averaging the codes will result in non-linearity. However, by using an ADC or DAC with only two output codes in our NS modulator we are guaranteed linearity (two points determine a line!). If one of the reference voltages in the ADC or DAC is offset from its ideal value then we'll get a gain error but no nonlinearity error.

In Chs. 4 and 5 we treated the clocked comparator as a 1-bit quantizer (ADC) with an LSB given by

$$1\ \text{LSB} = V_{REF+} - V_{REF-} = V_{LSB} \tag{6.1}$$

as an added noise source, Fig. 5.2. The PSD of the added noise, see Eq. (5.5), is

$$V_{Qe}^2(f) = \frac{V_{LSB}^2}{12 f_s} \tag{6.2}$$

In this chapter we'll set $V_{REF+} = VDD = 1$ V and $V_{REF-} = 0$ V so that $V_{CM} = VDD/2$ or 500 mV. We can think of the output of the comparator (the output of the NS modulator) as a binary offset number with a value of 1 or 0. After a simple conversion to two's complement numbers, the output can be changed to +1 (01) or −1 (11). Since our input signals are referenced, or swing around, V_{CM} it's useful to think in terms of two's complement numbers. For example, in Fig. 6.2, if we apply 500 mV to the input of our NS modulator we get 1010101... (second sketch) or an average of 500 mV (= V_{CM}). Since all signals are referenced to V_{CM} it may be more useful to say that we aren't applying a signal (meaning just the common-mode voltage is present at the input) and thus we get a sequence of +1, −1, +1, −1, etc. that averages to zero (V_{CM}). Figure 6.3 shows how we think about this in more detail. If we pass a signal through an inverter we are multiplying it by −1 when we think in terms of two's complement numbers.

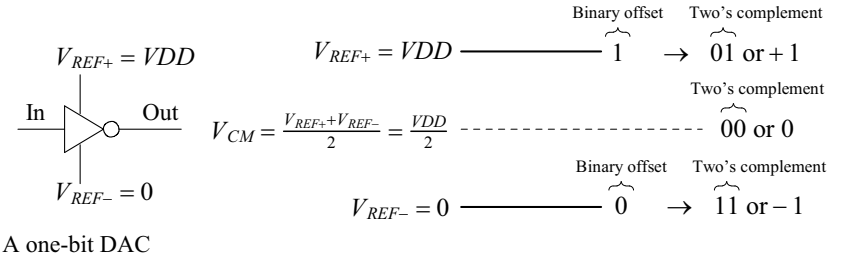


Figure 6.3 Thinking about the inverter in terms of the common-mode voltage.

6.1 Passive Noise-Shaping

Figure 6.4 shows a schematic and block diagram of a passive NS modulator. Reviewing Fig. 5.38, we see that this is a modulator topology with $B(f) = 1$. To calculate $A(f)$ let's write the output of the summing block (the resistors), or the input to the $A(f)$ block, as

$$\frac{v_{in} - v_{int}}{R} + \frac{-v_{out} - v_{int}}{R} = i_{int} \tag{6.3}$$

Note that, in Fig. 6.4b, we are assuming that the S/H response used in the model for an ADC, Fig. 5.2, is 1 ($f << f_s$). The output of the $A(f)$ block is

$$v_{int} = \frac{i_{int}}{j\omega C} \tag{6.4}$$

so,

$$v_{in} - v_{out} = v_{int} \cdot (j\omega CR + 2) \tag{6.5}$$

and therefore

$$A(f) = \frac{1}{2 + j\omega RC} \tag{6.6}$$

This is nearly the transfer function of an RC circuit, see Eq. (3.1). We can also think of this response as integrating for frequencies above $1/2\pi RC$. We'll come back to this in a moment. Using Eq. (5.66) we can write

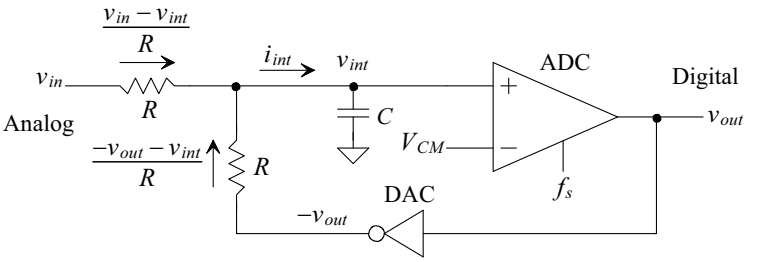
$$v_{out}(f) = \overbrace{\frac{1}{3 + j\omega RC}}^{STF(f)} \cdot v_{in}(f) + \overbrace{\frac{2 + j\omega RC}{3 + j\omega RC}}^{NTF(f)} \cdot V_{Qe}(f) \tag{6.7}$$

Notice that the AAF is built-in to this topology via the *STF*. At DC the noise transfer function appears to be 2/3. However, we know that at DC, as seen in Fig. 6.2, we can average the modulator's outputs and recover, exactly, the analog input signal (see dead zone issues for a passive modulator on page 215). This means that $NTF(0) = 0$. Let's try to get a better representation for the output of the modulator. In order to begin notice that

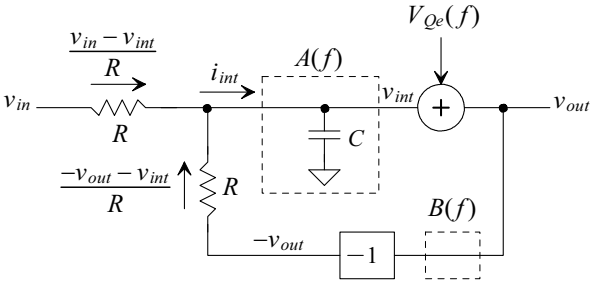
$$V_{Qe}(f) + v_{int}(f) = v_{out}(f) \tag{6.8}$$

Next, let's write

$$\left(\frac{v_{in} - v_{int}}{R} + \frac{-v_{out} - v_{int}}{R}\right) \cdot \frac{1}{j\omega C} + V_{Qe}(f) = v_{out} \tag{6.9}$$



(a) Circuit implementation of a passive NS modulator



(b) Block diagram model of a passive NS modulator.

Figure 6.4 A passive-integrator NS modulator.

and

$$v_{in} - v_{out} - 2v_{int} + V_{Qe} \cdot j\omega RC = j\omega RC \cdot v_{out} \tag{6.10}$$

$$v_{in} - 2v_{int} + V_{Qe} \cdot j\omega RC = v_{out} \cdot (1 + j\omega RC) \tag{6.11}$$

so finally

$$v_{out} = \overbrace{\frac{1}{1+j\omega RC}}^{STF(f)} \cdot v_{in} + \overbrace{\frac{j\omega RC}{1+j\omega RC}}^{NTF(f)} \cdot V_{Qe} + \underbrace{\frac{-2 \cdot v_{int}}{1+j\omega RC}}_{\text{Extra noise/distortion}} \tag{6.12}$$

The key things to note are: 1) that if we can keep v_{int} from varying we eliminate this extra distortion term (this is why we use an active integrator in later chapters), 2) the signal sees a lowpass response (so we have, as already mentioned, a built-in AAF that limits input spectral content), and 3) the noise is shaped towards the higher frequencies (the noise is high passed filtered). If our quantization noise is flat, as seen in Fig. 5.12, then high-pass filtering the noise gives the PSD seen in Fig. 6.5. Quantization noise that has been shaped in this way is called *modulation noise*. Note that the faster we clock the comparator (the larger f_s) the less variation we'll get in v_{int}. Also note, again, that the (digital) output of the modulator is the average of the (analog) input signal.

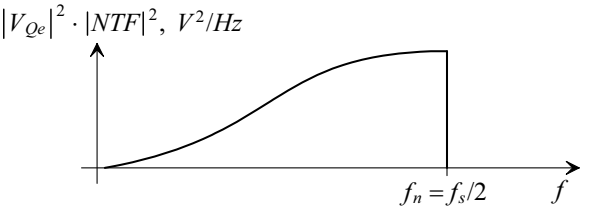


Figure 6.5 Modulation noise spectral density.

Example 6.1
Simulate the operation of the NS modulator seen in Fig. 6.4 when *R* is 10k, *C* is 10 pF, and the clocking frequency is 100 MHz. Comment on the resulting simulation results and the operation/limitations of the circuit.

Figure 6.6 shows the input (a sinewave at 500 kHz) and (digital) output of the circuit. Notice that as the input signal moves towards ground the output signal stays low more often. As the input signal moves towards *VDD* the output is high, or a logic 1, more often. While we can use a digital filter to change this one-bit code into an *N*-bit word (and we will!) let's show that a simple RC filter can be used to get our original signal back from the digital data, Fig. 6.7.

Note that for proper operation of a continuous-time (CT) NS data converter, like the one seen in Fig. 6.4, the comparator's gain and delay become very important. If the *comparator's delay varies* (and it will in a practical circuit) we get a degradation in *SNR* that appears like it's from clock jitter (see Sec. 5.2.2). Varying comparator delay is a **serious practical limitation** of CT NS converters for high-frequency conversions (it's much less of a concern for low frequency conversions) causing *amplitude modulation* in the converter's output. Adding an amplifier in the forward path of the modulator (see example in Fig. 6.24) can help ensure that the signal swing on the input of the comparator is large to minimize the comparator's delay. Adding an edge-triggered latch (a D-Flip-Flop) on the output of the comparator can be used to ensure a stable comparator output signal but adds delay (and thus makes stabilizing the system more challenging). ■

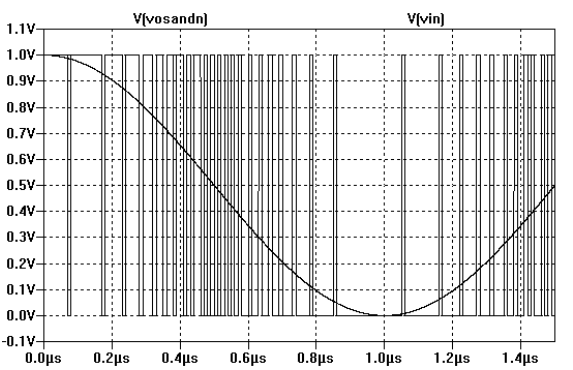


Figure 6.6 Simulating the operation of the passive NS modulator seen in Fig. 6.4.

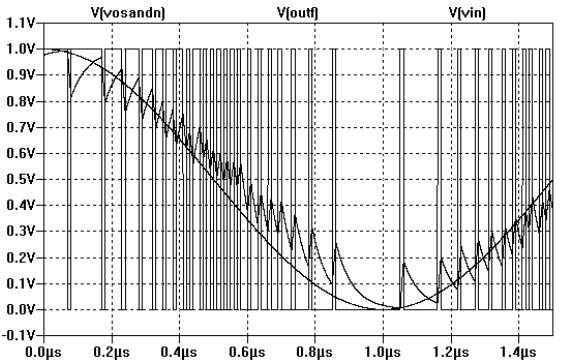


Figure 6.7 Using an RC circuit to filter the digital output in Fig. 6.6.

6.1.1 Signal-to-Noise Ratio

Let's calculate the SNR for the first-order noise-shaping modulator seen in Fig. 6.4 and characterized by Eq. (6.12). In the following we'll ignore the extra noise/distortion resulting from variations in v_{int}. Further note that the pole associated with both the STF and NTF won't affect the SNR since it's common to both. We know the output of the modulator is passed through a lowpass filter with a bandwidth B to remove the modulation noise, Fig. 6.8. The smaller B the lower the noise in the final digital output word and the larger the *SNR*. Again, the trade-off with using smaller lowpass filter bandwidth is that the frequency range of the allowable input signals shrinks. Let's calculate the RMS noise in the filter's output using

$$V_{noise,RMS}^2 = 2\int_0^B |NTF(f)|^2 |V_{Qe}(f)|^2 \cdot df = 2 \cdot \frac{V_{LSB}^2}{12 f_s} \cdot \int_0^B (2\pi f \cdot RC)^2 \cdot df \tag{6.13}$$

or

$$V_{noise,RMS}^2 = 2 \cdot \frac{V_{LSB}^2}{12 f_s} \cdot (2\pi RC)^2 \cdot \frac{B^3}{3} \tag{6.14}$$

again noting that using a smaller digital lowpass filter bandwidth, B, reduces the noise.

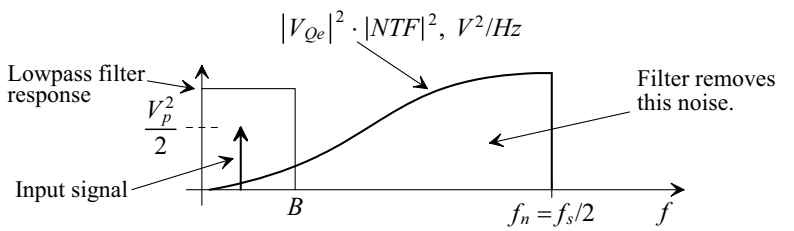


Figure 6.8 Filtering out modulation noise to calculate SNR.

We spent a great deal of time in Ch. 4 using Sinc-shaped lowpass filters for decimation. Let's use these filters here for filtering and decimating the output of the NS modulator. Let's set the bandwidth of the filter, see Fig. 4.17, to

$$B = \frac{f_s}{2K} \tag{6.15}$$

noting that we assumed, when deriving Eq. (6.14), a brickwall-shaped lowpass filter response. We can reduce the noise further, after decimation, by passing the digital data through additional lowpass filtering (perhaps using the biquad filters discussed in Ch. 4 with peaking to account for the droop introduced with the Sinc filter). Making the substitution gives

$$V_{noise,RMS}^2 = \frac{V_{LSB}^2}{12} \cdot (2\pi RC)^2 \cdot \frac{f_s^2}{12 \cdot K^3} \tag{6.16}$$

The value of RC must be much longer (at least five times) than the period of the sampling clock, T_s, to keep v_{int} from varying too much. Following the procedures used to derive Eqs. (5.10) to (5.13) we get

$$SNR_{ideal} = 20 \cdot \log \frac{V_p/\sqrt{2}}{V_{noise,RMS}} = 6.02N + 1.76 - 20 \log \frac{2\pi RC \cdot f_s}{\sqrt{12}} + 20 \log K^{3/2} \tag{6.17}$$

If we set $RC = 4.4/f_s = 4.4T_s$ then we can write

$$SNR_{ideal} = 20 \cdot \log \frac{V_p/\sqrt{2}}{V_{noise,RMS}} = 6.02N + 1.76 - 18.06 + 30 \log K \tag{6.18}$$

For $K = 4$ this equation is the same as Eq. (5.13). However, for every doubling of K beyond 4 we get an increase in resolution, N_{inc}, of 1.5 bits or an increase in SNR_{ideal} of 9 dB

$$N_{inc} = \frac{30 \log K - 18.06}{6.02} \tag{6.19}$$

$$SNR_{ideal} = 6.02(N + N_{inc}) + 1.76 \tag{6.20}$$

Figure 6.9 compares the first-order NS modulator to simple oversampling, Fig. 5.31 and Eq. (5.58). It's important to note that Bennett's criteria need not be valid using the oversampling feedback modulator discussed in this section (e.g. the input doesn't have to be busy).

6.1.2 Decimating and Filtering the Modulator's Output

It's important to note that Eq. (6.17) was derived assuming the output of the modulator was passed through a perfect lowpass filter with a bandwidth of B, $f_s/2K$. Passing the output through a Sinc averaging filter, see Fig. 4.14, will result in a poorer SNR because the higher frequency noise components will not be entirely filtered out. In this section we want to answer two questions: (1) what order, L (see Eq. [4.19]), of Sinc lowpass filter should be used in the digital filter on the output of the NS modulator, and (2) assuming we use only this filter (no additional filtering), how will the ideal SNR of the first-order NS modulator be affected?

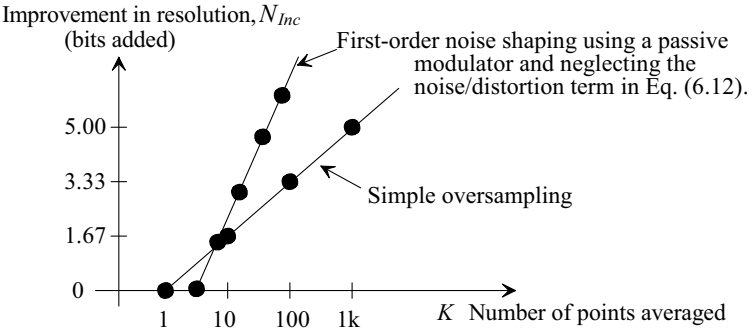


Figure 6.9 Comparing first-order noise-shaping to simple oversampling (Fig. 5.29).

We begin to answer the first question by noting that the increase in the number of bits, N_{inc}, was specified by Eq. (6.19). If our NS modulator uses a 1-bit ADC, then the final, after the digital filter, resolution of the resulting data converter is N_{inc} + 1 bits. (An NS modulator using a 5-bit ADC [often called a multibit NS modulator] would ideally have an output resolution of N_{inc} + 5 bits.) Further, we saw in Ex. 4.3 and Fig. 4.14 that the word size increased by $\log_2 K$ bits in each Sinc filter stage. For a cascade of L filters we can require

$$L \cdot \log_2 K \geq \frac{30 \log K - 18.06}{6.02} \tag{6.21}$$

For $K \leq 256$ we only need one lowpass Sinc filter or $L = 1$.

Example 6.2

Sketch the implementation of a $K = 16$ decimating filter for the NS modulator discussed in Ex. 6.1. Simulate the operation of the resulting ADC (modulator and filter). Estimate the *SNR*, number of final bits, and Nyquist frequency.

The decimating filter's transfer function is

$$\frac{1 - z^{-16}}{1 - z^{-1}} \tag{6.22}$$

and seen in Fig. 6.10 (see Sec. 4.2.5). The filter's output clock rate is 100 MHz/16 or 6.25 MHz so the Nyquist frequency is half of this or 3.125 MHz. The increase in the number of bits is 3, using Eq. (6.19), so the final output word size, based on

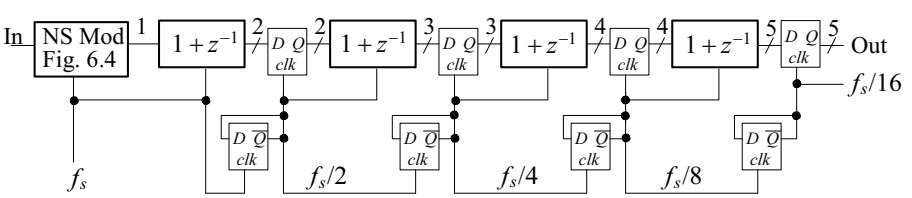


Figure 6.10 Lowpass and decimating filter used in Ex. 6.2.

the *SNR* (= 25.78 dB), is 4-bits. Our filter causes the word size to increase by 1-bit through each of the 4 stages so that our final output word size is 5-bits. We can throw the MSB of this word out; however, notice that the largest word we get out of the filter is when the filter's input remains a 1 at all times. In this case the filter's output (the output of the ADC made using the NS modulator and filter) is 16 or 1 0000. When the filter's input is a 0 at all times our filter's output is 0 0000. The output can swing from 1 0000 to 0 0000 around the common-mode code of 0 1000 (8). By removing the MSB we can make the output swing from 1111 (15) to 0000 (0) around 1000 (8). However if the NS modulator's input moves close to V_{REF+} (here *VDD*) then the output of the filter can **overflow**.

Figure 6.11 shows the simulation results. The input frequency, as in Ex. 6.1, is 500 kHz. Looking at the frequency response of our filter, Eq. (4.20) and Fig. 4.17, we should only see a minor amount of attenuation through the filter. However, looking at Fig. 6.11 we see more than a minor amount of output signal reduction. We've, up to this point, ignored the extra distortion/noise term seen in Fig. 6.12. In the next section we'll discuss this term in more detail and how matching and offsets effect the performance of the modulator. ■

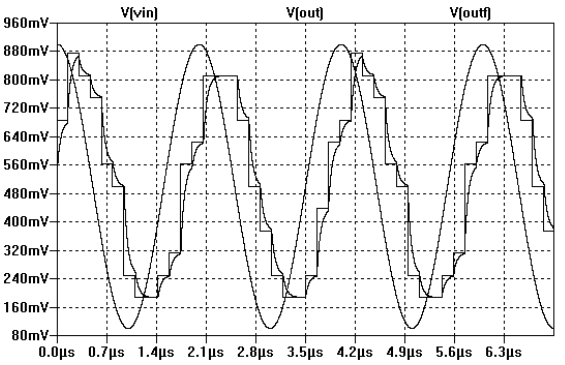


Figure 6.11 Simulating the ADC (modulator and filter) discussed in Ex. 6.2.

SNR Calculation using a Sinc Filter

Let's now consider how filtering with a Sinc filter instead of the ideal lowpass filter effects the *SNR* of the modulator/filter implementation of a data converter. Remember the SNR_{ideal} was calculated in Eq. (6.18) assuming the modulation noise was strictly bandlimited to *B*. Figure 6.12 shows the PSD of the $NTF^2(f)$ and $|V_{Qe}(f)|^2$ (the modulation noise) in a first-order passive NS modulator. Also shown in this figure is the shape of the averaging filter's magnitude response squared that is normalized to unity by dividing by *K*, see Eq. (4.20). Here we are showing the shape of a filter with $K = 16$ and a range of $f_s/2$ (see Fig. 5.12).

We can calculate the RMS quantization noise resulting from a cascade of a first-order modulator and an averaging filter, $L = 1$, using

$$V_{Qe,RMS}^2 = 2\int_0^{f_s/2} |NTF(f)|^2 \cdot |V_{Qe}(f)|^2 \cdot |H(f)|^2 \cdot df \qquad (6.23)$$

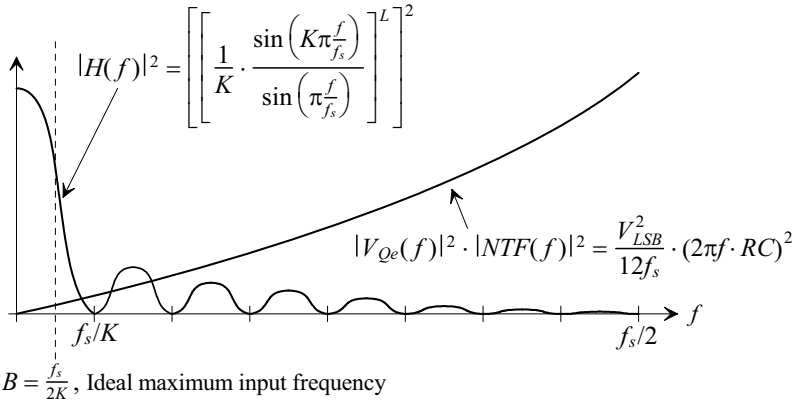


Figure 6.12 Showing modulation noise and filter response.

or

$$V_{Qe,RMS}^2 = 2\cdot\frac{V_{LSB}^2}{12f_s}\cdot\int_0^{f_s/2}(2\pi f\cdot RC)^2\frac{1}{K^2}\cdot\frac{\sin^2\left(K\pi\frac{f}{f_s}\right)}{\sin^2\left(\pi\frac{f}{f_s}\right)}\cdot df \qquad (6.24)$$

For the frequency range of interest $f << f_s$ so $\sin x \approx x$ and we get

$$V_{Qe,RMS}^2 = 2\cdot\frac{V_{LSB}^2}{12f_s}\cdot(2f_s\cdot RC)^2\cdot\frac{1}{K^2}\cdot\int_0^{f_s/2}\sin^2\left(K\pi\frac{f}{f_s}\right)\cdot df \qquad (6.25)$$

Let's let $\theta = \pi\cdot\frac{f}{f_s}$ so

$$V_{Qe,RMS}^2 = 2\cdot\frac{V_{LSB}^2}{12f_s}\cdot(2f_s\cdot RC)^2\cdot\frac{f_s}{K^3\pi}\cdot\overbrace{\int_0^{\frac{\pi}{2}}\sin^2 K\theta\cdot d\theta}^{=\frac{\pi}{4}} \qquad (6.26)$$

and

$$V_{Qe,RMS}^2 = \frac{V_{LSB}^2}{12}\cdot(2\pi RC)^2\cdot\frac{f_s^2}{2\pi^2K^2} \qquad (6.27)$$

Comparing this result to what we got in Eq. (6.16) we see that using the Sinc lowpass filter is nearly ideal for removing modulation noise. The more important concern, when using the Sinc lowpass filter, is the droop that the desired signal undergoes.

6.1.3 Offset, Matching, and Linearity

Examine the passive NS-modulator with offsets and mismatched resistors seen in Fig. 6.13. In this section we want to discuss how non-ideal behavior affects the performance of the modulator. To begin, notice that a comparator offset has the effect of causing the average value of v_{int} to be $V_{CM}\pm V_{OS}$ and thus the offset passes directly to the output of the modulator. This means that if we apply the common-mode voltage to the input the average of the output voltage is $V_{CM}\pm V_{OS}$.

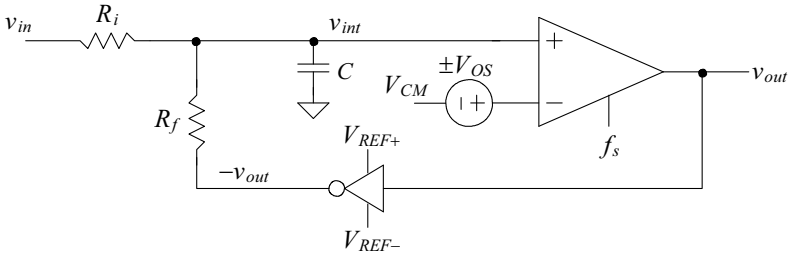


Figure 6.13 Passive modulator with mismatch and offsets.

Resistor Mismatch

In order to determine the effects of resistor mismatch we can re-write Eqs. (6.9) to (6.12), neglecting the effects of the offset voltage, as

$$\left(\frac{v_{in}-v_{int}}{R_i}+\frac{-v_{out}-v_{int}}{R_f}\right)\cdot\frac{1}{j\omega C}+V_{Qe}(f)=v_{out} \tag{6.28}$$

$$R_f\cdot(v_{in}-v_{int})-R_i\cdot(v_{out}+v_{int})+j\omega R_iR_f\cdot C\cdot V_{Qe}=j\omega R_iR_f\cdot C\cdot v_{out} \tag{6.29}$$

$$R_f\cdot v_{in}-(R_i+R_f)\cdot v_{int}+j\omega R_iR_f\cdot C\cdot V_{Qe}=(j\omega R_iR_f\cdot C+R_i)\cdot v_{out} \tag{6.30}$$

$$v_{out}=\frac{\frac{R_f}{R_i}}{1+j\omega CR_f}\cdot v_{in}+\frac{j\omega CR_f}{1+j\omega CR_f}\cdot V_{Qe}+\frac{-v_{int}\cdot\frac{R_i+R_f}{R_i}}{1+j\omega CR_f} \tag{6.31}$$

The effect of mismatched resistors is a gain error (but no non-linearity, and thus, distortion). Note that the absolute value of the capacitor isn't critical or important for precision operation.

The Feedback DAC

The feedback DAC is the most critical component in the modulator for precision operation. Consider the waveforms seen in Fig. 6.14. In this figure we show the ideal shapes of the DAC's output (remember our DAC here is a simple inverter so we get

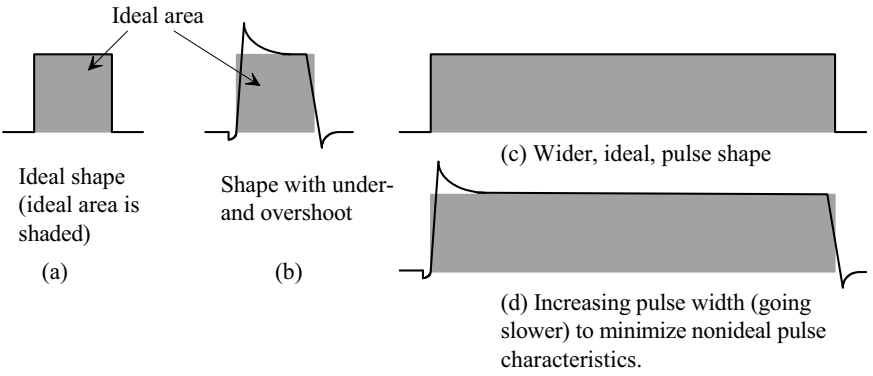


Figure 6.14 Comparator output pulse shapes, input to the integrator.

perfect linearity, Fig. 6.15). As seen in the figure, the shape of the pulse affects the amount of charge, or current, we send back to the capacitor. In part (a) we see the ideal pulse shape and the ideal area under the pulse (the shaded area). In part (b) we see how the finite rise time and fall time can affect the actual area under the curve and thus the output of the integrator. In order to minimize these unwanted effects we can use wider pulses as shown in parts (c) and (d), which means we run the modulator at a slower clocking frequency. Increasing the width of the pulses minimizes the percentage of the area affected by the transition times. Note that the feedback signal directly subtracts from the input signal so that any noise or unwanted variation in the fed back signal, such as an amplitude variation, can be considered as adding noise to the input (and thus degrading the modulator's SNR). This is important. In the coming chapters we will use switched-capacitor circuits that simply have to fully-discharge in order to make the shape of the feedback pulse less important.

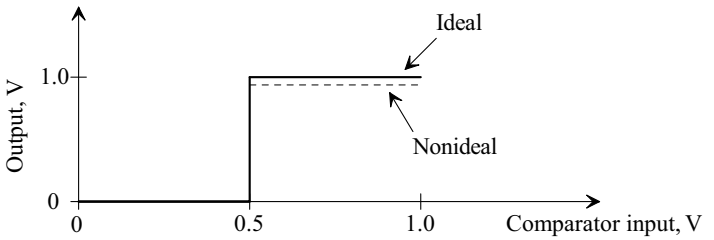


Figure 6.15 Ideal and nonideal transfer curves for a 1-bit DAC.

DAC Offset

Notice, in Fig. 6.15, that if our DAC's reference voltages are offset from their ideal values of V_{REF+} and V_{REF-} that, like mismatched resistors, all we get is a gain error (no non-linearity). Possibly the most important concern when using a single-bit inverter topology DAC is the on-resistance of the transistors used to drive the feedback resistors. The drive strength of the MOSFETs should be so high that little voltage is dropped across them (so the output of the DAC swings between V_{REF+} and V_{REF-}). This (limited DAC drive) is, again, another reason we'll soon start to focus on switched-capacitor implementations of NS modulators.

Linearity of the First-Order Modulator

We've ignored the effects of the extra noise/distortion term seen in Eq. (6.12) because it's a nonlinear error highly dependent on the input signal's characteristics (and thus hard to quantify). Let's use simulations to look at the linearity of the first-order NS modulator and digital filter seen in Fig. 6.10 (with a DAC connected to the output of the digital filter to show the digital data as an analog waveform). Figure 6.16 shows the input/output of Fig. 6.10 with a slow ramp applied to the modulator's input. Note that when the input ramp voltage is close to the power supply rails the digital output becomes nonlinear (too high when the input is close to ground and to low when the input is close to *VDD*). Also seen in this figure, as mentioned in Ex. 6.2, is the digital filter overflowing. In order to avoid this situation we can use a selector, like the one seen in Fig. 4.40, with the *Sel* input connected to the MSB of the filter (remember we do a multiply by 2 by removing the filter's MSB to scale the filter's output to full scale as discussed in Ex. 6.2). When the

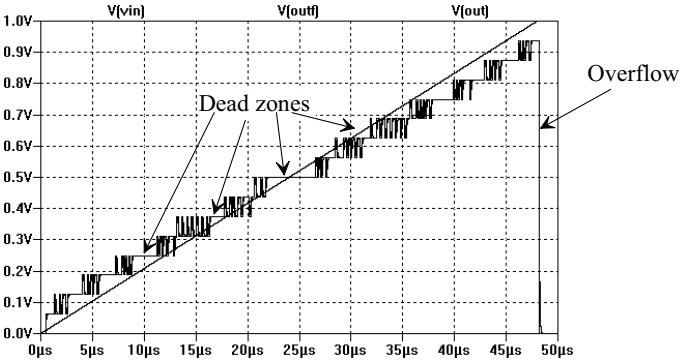


Figure 6.16 Simulating the linearity of the first-order NS modulator.

MSB of the filter's output is a 0 we simply pass the multiplied-by-2 output of the filter through the selector to the final output. When the MSB of the filter's output is a 1, we use the selector to clamp the final output to 1111 and thus avoid overflow.

Dead Zones

Besides the nonlinearity seen in Fig. 6.16, notice that for some ranges of input voltages the output doesn't move or, rather, *the output is dead*. A simple example of a dead output is seen when the input signal is close to the common-mode voltage, 500 mV. These *dead zones* are the result of a repeating modulator output code (e.g., 010101, 110110, 0000100001, etc.). The question is why does the modulator output code repeat for a relatively wide range of input voltages (e.g. 460 mV < v_{in} < 540 mV)? In order to answer this question examine the modulator seen in Fig. 6.13. With an input voltage of 500 mV the output of the modulator is 101010... so that the average of the output is 500 mV. Now suppose the input voltage is increased to 510 mV. Because the voltage v_{int} varies with time, it's possible for the average current supplied from the input, $[v_{in} - v_{int}(t)]/R_i$ to equal the fed back current $[-v_{out} - v_{int}(t)]/R_f$ when the modulator's output is 1010101... By using an active integrator, Sec. 6.2.4, we can hold v_{int} constant and eliminate dead zones.

6.2 Improving SNR and Linearity

In this section we discuss techniques for improving signal-to-noise ratio and linearity. We'll start out by discussing the second-order passive (uses two capacitors) noise-shaping modulator. This topology is considerably more useful than the first-order topology discussed in the last section because it has better linearity, randomizes the output code (to avoid dead zones), and lower modulation noise in the signal bandwidth of interest. Then we'll discuss using switched-capacitors instead of resistors in the feedback paths. The big benefit of switched-capacitor circuits over continuous-time circuits is that, Fig. 6.14, we remove the effects of non-ideal pulse shapes. The drawback is the need for a non-overlapping clock generator (which consumes power and layout area). Next we'll discuss putting NS modulators in parallel. This is useful for increasing SNR while not lowering the final output clocking frequency (at all or as much). Finally, we'll end the section by showing how an active circuit, e.g. an op-amp, can be used to improve linearity and noise by removing the extra term seen, for example, in Eq. (6.12).

6.2.1 Second-Order Passive Noise-Shaping

After examining the first-order modulator seen in Fig. 6.4 we might wonder if we can get better performance by double filtering the input signal and removing the comparator's connection to V_{CM}. Figure 6.17 shows the resulting circuit. In this circuit we have two feedback paths. We've connected the largest amount of feedback to the inverting input of the comparator to ensure negative, overall, feedback. Note that, because the output is fed back to both integrating nodes v_1 and v_2, the circuit will act to drive these nodes to the same value and thus attempt to keep them equal to each other.

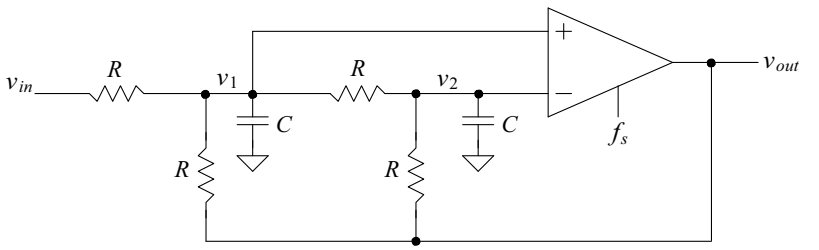


Figure 6.17 Second-order passive modulator.

To attempt to describe the operation of the circuit let's write

$$\left(\frac{v_{in}-v_1}{R}+\frac{v_{out}-v_1}{R}-\frac{v_1-v_2}{R}\right)\cdot\frac{1}{j\omega C}=v_1 \tag{6.32}$$

and

$$\left(\frac{v_1-v_2}{R}+\frac{v_{out}-v_2}{R}\right)\cdot\frac{1}{j\omega C}=v_2 \tag{6.33}$$

If the quantization noise added to v_1 and v_2 is V_{Qe1} and V_{Qe2} then $v_1+V_{Qe1}=v_{out1}$ and $v_2+V_{Qe2}=v_{out2}$. We can then write

$$v_{in}-3v_1+v_2+j\omega RC\cdot V_{Qe1}=v_{out1}(j\omega RC-1) \tag{6.34}$$

$$v_1-2v_2+j\omega RC\cdot V_{Qe2}=v_{out2}(j\omega RC-1) \tag{6.35}$$

Adding these two equations gives

$$v_{in}-2v_1-v_2+j\omega RC\cdot(V_{Qe1}+V_{Qe2})=(v_{out1}+v_{out2})\cdot(j\omega RC-1) \tag{6.36}$$

As a quick check to ensure that this equation is correct, notice that if we pass the output signal through a lowpass filter with a bandwidth approaching 0, $\omega\rightarrow 0$ and we use a large RC then for a DC input, $v_{in}\approx v_1\approx v_2$ and $v_{in}-2v_1-v_2=-2v_{out}$ (so $v_{out}\approx v_{in}$). Next, adding the random signal powers together (see, for example, Eq. [5.55] and the associated discussion) gives

$$(\omega RC)^2\cdot\left(V_{Qe1}^2+V_{Qe2}^2\right)=(\omega RC)^2\cdot\frac{V_{Qe}^2}{2} \tag{6.37}$$

and

$$\left(v_{out1}^2 + v_{out2}^2\right) \cdot \left((\omega RC)^2 + (-1)^2\right) = \left(1 + (\omega RC)^2\right) \cdot \left(v_{out,noise}^2 + v_{out,signal}^2\right) \quad (6.38)$$

Finally, we can write

$$v_{out,noise}^2 = \frac{(\omega RC)^2}{1 + (\omega RC)^2} \cdot \frac{V_{Qe}^2}{2} \quad (6.39)$$

$$v_{out,signal}^2 = \frac{1}{1 + (\omega RC)^2} \cdot v_{in}^2 \quad (6.40)$$

noting the quantization noise power is cut in half. Equation (6.18) can be rewritten for the second-order passive noise-shaping topology as

$$SNR_{ideal} = 20 \cdot \log \frac{V_p/\sqrt{2}}{V_{noise,RMS}} = 6.02N + 1.76 - 15.13 + 30 \log K \quad (6.41)$$

The modest increase in *SNR*, however, is not the big benefit of this topology. Rather the better linearity and reduction in dead zones are the major benefits of the topology. The extra noise/distortion term can be written as

$$\frac{2v_1 + v_2}{1 + (\omega RC)^2} \quad (6.42)$$

Note that this topology attempts to drive v_1 and v_2 to the same value, that is v_{in}. The drawback of this is that the comparator must operate with an input range extending from *VDD* to ground. Figure 6.18 shows the simulation results where we repeated the simulation seen in Fig. 6.16 but used the second-order modulator. Clearly both the linearity and extent of dead-zones are much better using the second-order modulator.

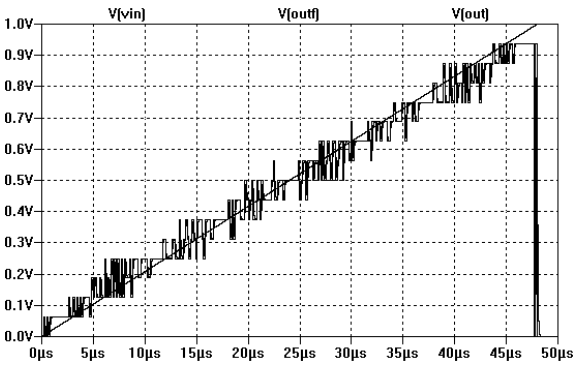


Figure 6.18 Repeating the simulation seen in Fig. 6.16 but with a second-order modulation.

Example 6.3

Repeat the simulation seen in Fig. 6.11 and Ex. 6.2 using the second-order modulator seen in Fig. 6.17.

The simulation results are seen in Fig. 6.19. The output amplitude more closely resembles the input amplitude. ■

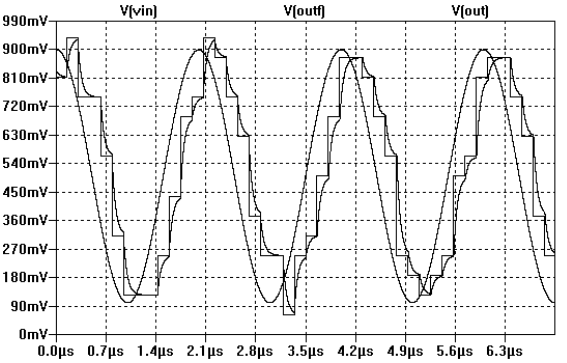


Figure 6.19 Repeating the simulation seen in Fig. 6.11 but with a second-order modulation.

6.2.2 Passive Noise-Shaping Using Switched-Capacitors

Figure 6.20 shows the first-order modulator seen in Fig. 6.4 implemented using switched-capacitor (SC) resistors, Fig. 2.35 (the resistors in Fig. 6.4 are replaced with SC resistors). Figure 6.21 shows the simulation results similar to Fig. 6.7 but using this new implementation. Again the benefit of this implementation over the continuous-time implementation seen in Fig. 6.4a is that the shape of pulse coming out of the feedback DAC, here an inverter, isn't important as long as the capacitors fully charge and discharge.

To characterize the operation of this topology let's write, again see Fig. 2.35,

$$R_{SC} = \frac{1}{f_s C} \tag{6.43}$$

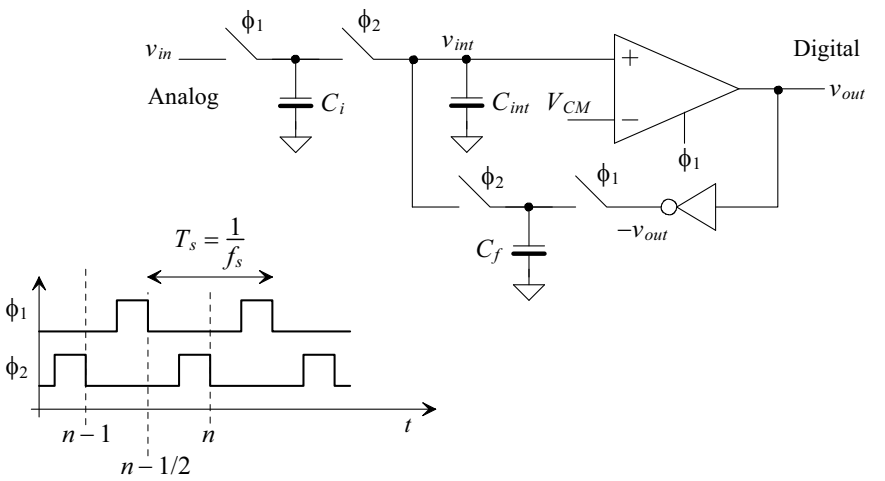


Figure 6.20 First-order passive modulator using switched-capacitors.

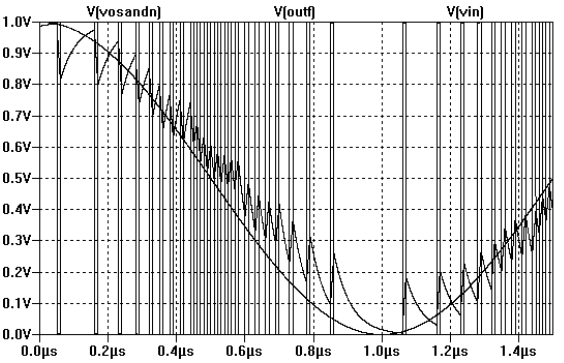


Figure 6.21 Regenerating Fig. 6.7 using a passive switched-capacitor modulator.

The operation of this topology can be described by simply substituting Eq. (6.43) into Eq. (6.31). The signal gain can then be written as

$$\frac{R_f}{R_i} = \frac{C_i}{C_f} \tag{6.44}$$

If C_i isn't exactly equal to C_f then the input signal undergoes a gain error. In order to eliminate this gain error, and to simplify the implementation of the modulator, consider sharing the feedback and input capacitors, Fig. 6.22. Simulations showing the operation of this circuit are found at CMOSedu.com. Reviewing the derivations in Sec. 2.2.3, we see that the input signal, in Fig. 6.22, is subtracted from the fed back signal and summed together using C_{int}. The inputs of the comparator are swapped, from Fig. 6.20, to ensure the polarity of the output signal matches the input signal's polarity. Notice that we connected the input and fed back signal's to the bottom plate of C_i. Remember that this is the plate with the largest parasitic capacitance. When the ϕ_1 switches are closed, the bottom plate of C_i, and its parasitic, are charged to v_{in}. Noise coupled into this bottom plate, from the substrate, sees the low-impedance input so that ideally none of the noise passes through to C_{int}. When the ϕ_2 switches close the bottom plate of C_i charges to v_{out}. Since the bottom-plate parasitic charges back and forth between v_{in} and v_{out}, none of the charge from this parasitic is transferred to C_{int}.

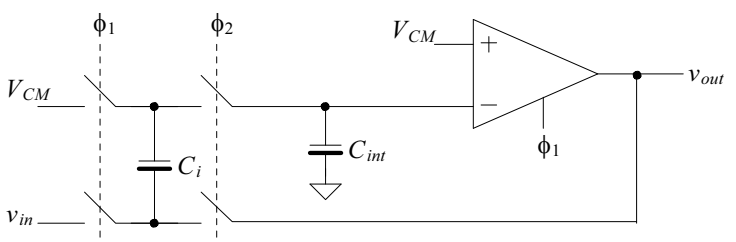


Figure 6.22 Switched-capacitor implementation of the passive modulator without gain error.

6.2.3 Increasing SNR using K-Paths

By increasing the sampling rate, f_s, we can spread the quantization noise out over a wider frequency range, Figs. 5.12 and 5.26. Thus, for a fixed digital averaging filter bandwidth (see Fig. 6.1), the amount of noise in a digital output signal can be reduced. As discussed earlier in Secs. 2.1.6 and 5.3 we can increase the effective sampling frequency by using *K*-paths (putting *K* modulators in parallel). Since we've used the same variable, *K*, for both the number of points averaged in the digital filter on the output of a modulator, Sec. 4.2, and the number of paths used, Sec. 2.1.6, let's, in this section, use variables with differentiating subscripts to describe the operation of a modulator implemented with *K*-paths and oversampling

$$K_{avg} = \text{number of samples averaged in the digital filter} \tag{6.45}$$

and

$$K_{path} = \text{number of paths used in the modulator} \tag{6.46}$$

The digital filter connected to the output of the modulator can then be described using

$$H(z) = \left[\frac{1 - z^{-K_{avg}}}{1 - z^{-1}} \right]^L \tag{6.47}$$

By using *K*-paths our sampling frequency changes from f_s to $K_{path} \cdot f_s$ so that the PSD of the quantization noise, Fig. 5.26, gets spread out over a wider frequency range

$$V_{Qe}^2(f) = \frac{V_{LSB}^2}{12 \cdot K_{path} \cdot f_s} \tag{6.48}$$

For the noise-shaping topologies we would replace *K* (for example, see Eq. [6.18]) with $K_{avg} \cdot K_{path}$ while the bandwidth of our desired signal spectrum ranges from DC to *B when decimation is used* where

$$B = \frac{f_s}{2K_{avg}} \tag{6.49}$$

The next question that we need to answer is "Is it practical to implement parallel paths of noise-shaping modulators or Nyquist-rate data converters?" Clearly there will be an increase in layout area using this approach. Is the increase in SNR worth the increase in chip size, power draw, or complexity? Well, **let's not spend any time** on Nyquist-rate converters (e.g., flash or pipeline) in a *K*-path configuration (called a *time-interleaved* converter) since the input signal would have to meet Bennett's criteria (pages 165-166, consider problems with a DC input). Reviewing Fig. 2.37 we see that using a SC modulator like the one seen in Fig. 6.22 may be a possibility. However, notice that we need to multiply up the clock frequency from f_s to Kf_s then pass the resulting signal through the non-overlapping clock generator seen in Fig. 2.38. Further, the SC modulators would have to settle (fully charge/discharge their capacitors) within T_s/K seconds (an even bigger concern if the modulator uses an active element like an op-amp). If this is possible why not simply use a single path clocked at the higher rate, Kf_s (or better yet two paths clocked at $Kf_s/2$ like the topology seen in Fig. 2.36)? We get the same performance as the *K*-paths but with a much simpler implementation. Since we have to direct, and process, the input signal to the various paths, again Fig. 2.37, at a high-rate the use of *K*-paths in SC circuits may be limited (more on this in a moment and in Ch. 9).

What about using the modulator seen in Fig. 6.4 in a *K*-path implementation? Figure 6.23 shows a 2-path, or *time-interleaved*, implementation. There are several benefits to this topology including: 1) the input can be continuously connected to the *K*-paths of modulators, 2) no active device (e.g. an op-amp) with settling time issues, and 3) the comparators are triggered on the rising edge of a clock signal (so the feedback operation can occur over the entire clock period, T_s for each path). The drawback of this topology is the mismatched gains through each path. Notice that we've combined the digital outputs of the modulator into a two-bit word (so the possible outputs are 00, 01, and 10). This addition, we should recognize, is a filter with a transfer function

$$H(z) = 1 + z^{-1} = \frac{1 - z^{-2}}{1 - z^{-1}} = \frac{1 - z^{-K_{path}}}{1 - z^{-1}} \text{ where } f_{s,new} = K_{path} \cdot f_s,\ z^{-1} = e^{-j2\pi \cdot \frac{f}{f_{s,new}}} \tag{6.50}$$

or an average of two filter. If we were to use 8-paths we would get a 4-bit output ranging from 0000 to 1000 (which may result in the same overflow problems we saw in Figs. 6.16 and 6.18 when the input of the topology is near V_{REF+}, or *VDD*, here). A simple solution to the overflow problem, other than using a selector to keep overflow from occurring as discussed earlier, is to use only 7-paths (instead of 8) so the final output code ranges from 000 to 111.

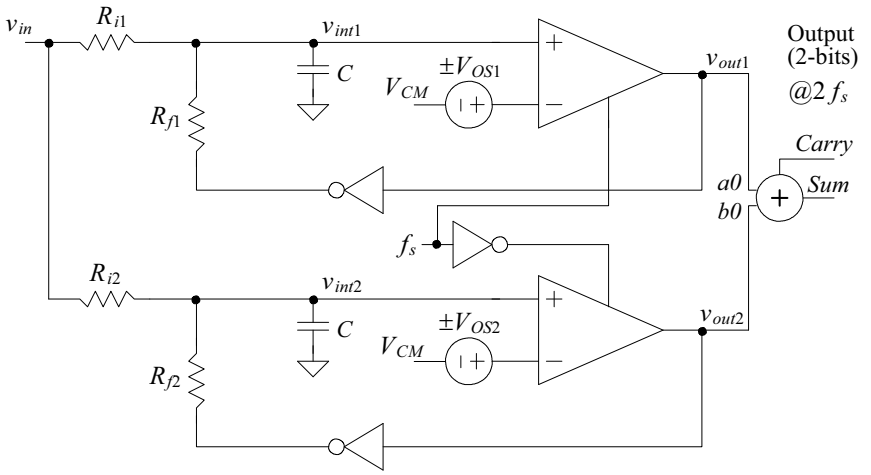


Figure 6.23 Two-path, time-interleaved, passive modulator with mismatch and offsets.

Note that each path, in Fig. 6.23, will attempt to hold the input of each comparator at a different voltage, dependent on the offset voltage of the comparator,

$$v_{int1} \rightarrow V_{CM} \pm V_{OS1} \text{ and } v_{int2} \rightarrow V_{CM} \pm V_{OS2} \tag{6.51}$$

so combining the input resistors and capacitors into a single path and the comparators and feedback paths into *K*-paths, to simplify the circuit and to reduce the effects of path mismatch, requires some thought. Consider the 4-path topology seen in Fig. 6.24. Here we've added an amplifier, with a gain of *G*, in series with the input path. Each comparator's offset is referred back to the integrating capacitor by dividing by this gain. If *G* = 100, for example, the differing offsets will have little effect on the circuit's operation.

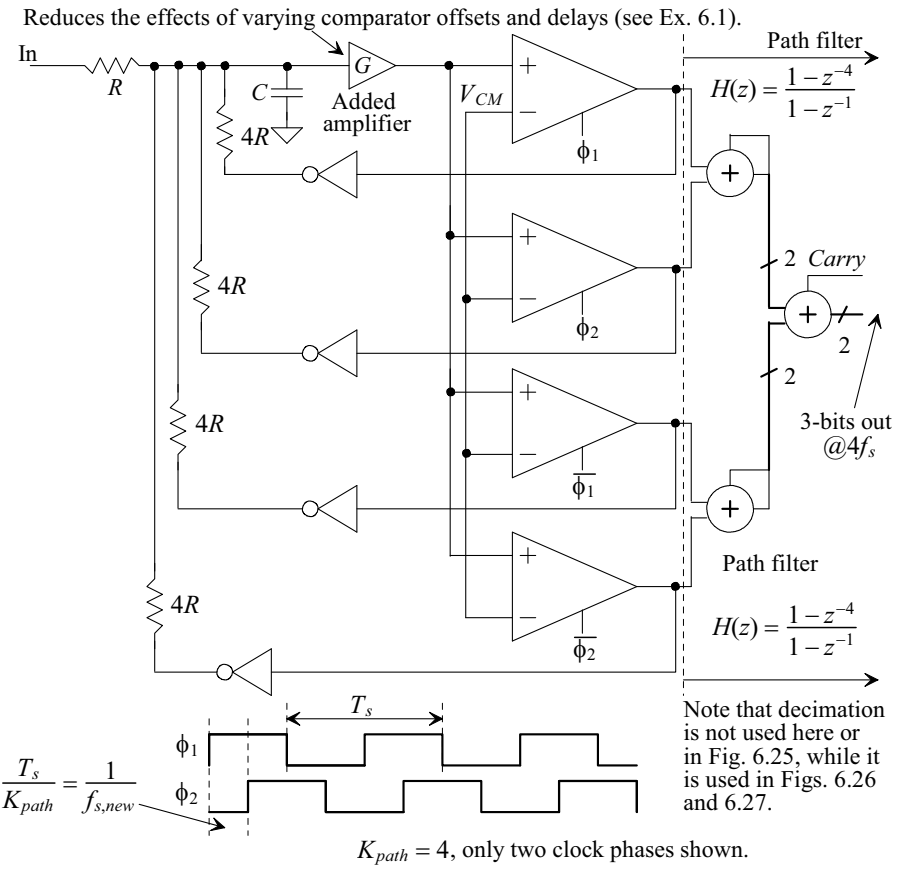


Figure 6.24 Four-path passive modulator. No longer time-interleaved since the integrator is common to all feedback paths (we'll call this the K-Delta-1-Sigma topology).

Another design concern, when using this topology, is the delay around each feedback path. If there is excessive phase shift through the forward or feedback paths, the modulator will be unstable. Using an open-loop (no feedback) amplifier, like a diff-amp, will ensure minimum delay (again noting the gain, and thus frequency response, of this amplifier aren't important as long as the gain is high enough to eliminate the offset effects of the comparators and the delay through the amplifier is comparable to T_s/K_{path}). Using an op-amp, in a feedback configuration, can ultimately limit the maximum speed of this topology. Figure 6.25 shows the output of the modulator in Fig. 6.24 with the same input signals and values used to generate Figs. 6.7 and 6.21. In Fig. 6.25 we've displayed the digital output word in analog form. Notice that the RC filtered output of this circuit is much smoother (contains less noise) than the outputs seen in Fig. 6.7 and 6.21. The extra smoothing from the inherent filtering when adding the outputs of the modulators together, (see filter transfer function in Fig. 6.24), helps to reduce the noise in the signal. Because of this inherent filtering it's easy to perform decimation directly on the output of the modulator. Figure 6.26 shows adding a register to re-time the output of the modulator (decimate) back down to f_s. Also seen in this figure is the digital filter seen in Fig. 6.1 that is used to remove the modulation noise. Regenerating the simulation results in Fig. 6.25

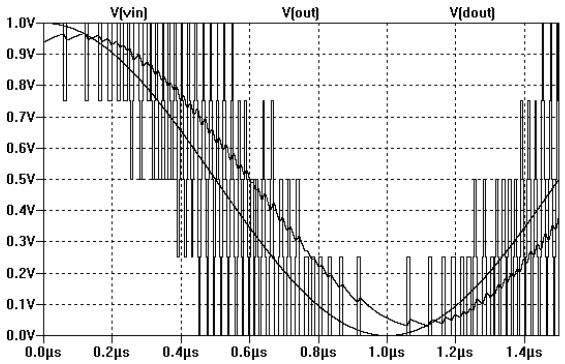


Figure 6.25 Simulating the operation of the 4-path modulator in Fig. 6.24.

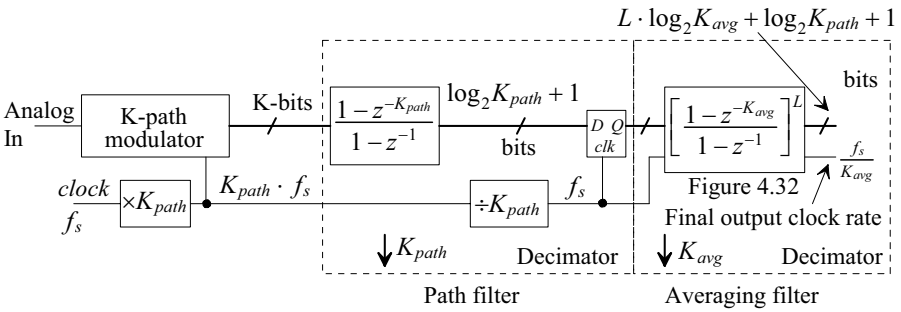


Figure 6.26 Performing decimation on the output of the modulator.

using decimation of 4 we get the results seen in Fig. 6.27. The rate of the digital word output by the path filter is f_s (just as it is when using a Nyquist-rate converter). Further, the path filter in Fig. 6.26 has the same frequency response as the S/H used in a Nyquist-rate ADC (a droop of −3.9 dB at $f_s/2$, Fig. 2.17). Thus, with some thought, we can use this topology to implement high-speed Nyquist-rate ADCs.

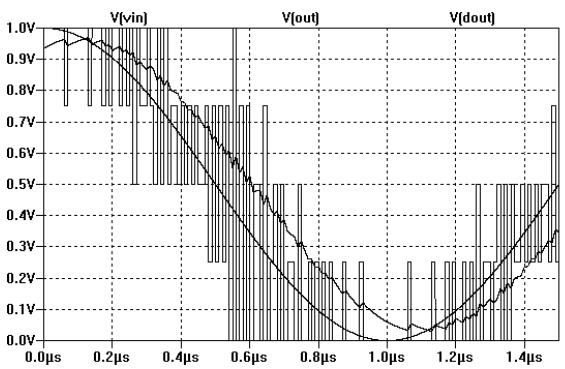


Figure 6.27 Regenerating the signals seen in Fig. 6.25 with a decimation of 4.

Revisiting Switched-Capacitor Implementations

At the beginning of the section, we dismissed the option of using switched-capacitor noise-shaping topologies in a *K*-path configuration, Fig. 2.37, because the capacitors would have to charge or discharge within T_s/K seconds (comparator delay < T_s/K is a challenge). We said that if this were possible why not use two paths, clocked on opposite phases of a clock (Fig. 2.36), but at the higher clock frequency of $K \cdot f_s$? In the next chapter we'll show that a first-order noise-shaping delta-sigma modulator implemented using switched-capacitors has an input/output relationship given, see Eq. (7.2), by

$$v_{out}(z) = \overbrace{z^{-1}}^{STF(f)} \cdot v_{in}(z) + \overbrace{(1-z^{-1})}^{NTF(f)} \cdot V_{Qe}(z) \tag{6.52}$$

The signal-transfer-function (*STF*) is simply one clock cycle delay, z^{-1} while the quantization noise is differentiated, Fig. 1.20. In other words the noise-transfer-function (*NTF*) is that of a differentiator, $(1-z^{-1})$. Note the similarity to the differentiation, $j\omega RC$, the quantization noise sees at low frequencies, $1 >> j\omega RC$, in the continuous-time passive NS modulator, Eq. (6.12). If we put *K* of these switched-capacitor topologies described by the above equation in parallel, Fig. 2.37, we can write the corresponding output of the topology, see Eq. (2.56), as

$$v_{out}(z) = \overbrace{z^{-K}}^{STF(f)} \cdot v_{in}(z) + \overbrace{(1-z^{-K})}^{NTF(f)} \cdot V_{Qe}(z) \tag{6.53}$$

Note that the data is changing, on the output of this topology, at a rate of $K \cdot f_s = f_{s,new}$, so that $z = e^{j2\pi \cdot f/f_{s,new}}$. While the quantization noise PSD, as indicated in Eq. (6.48), will be spread out over a wider frequency range the fact that our *NTF* has the shape of a comb filter, Fig. 1.25, instead of differentiation *limits the use of SC modulators in K-path ADCs using clock signals like those seen in Fig.* 2.37 *for high-speed conversion*.

One may wonder why the *STF* is z^{-K} or such a long delay? Looking at the timing of the clock signals in Fig. 2.37 we see that each path is only activated every T_s seconds. If $z = e^{j2\pi \cdot f/f_{s,new}}$ or $z = e^{j2\pi \cdot f/(Kf_s)}$ then to represent a single path delay of T_s seconds we have to use z^{-K}. In this scenario, Fig. 2.37 where *H*(*z*) represents the transfer function of a modulator, each of the modulators is independent, that is, not sharing the integrating capacitor (integrator) as we did in the topology seen in Fig. 6.24. With some thought *we can implement a practical K-path ADC using SC circuits sharing a common integrator, Fig.* 6.24*, with clock signals, also seen in Fig.* 6.24*, having a width of* T_s *and leading edge spacing of* T_s/K *seconds so that the effective sampling frequency is* $K \cdot f_s$ (Ch. 9).

Effects of the Added Amplifier on Linearity

We added the amplifier with a gain, *G*, in Fig. 6.24 in order to reduce the effects of comparator offset and make combining *K*-paths of quantizers sharing a common integrating capacitor a practical analog-to-digital converter topology. We haven't analyzed how this added amplifier can affect the linearity and performance of the topology. Let's do that here. Rewriting Eqs. (6.8) to (6.12) with this gain included we get

$$V_{Qe}(f) + G \cdot v_{int}(f) = v_{out}(f) \tag{6.54}$$

$$\left(\frac{v_{in} - v_{int}}{R} + \frac{-v_{out} - v_{int}}{R}\right) \cdot \frac{G}{j\omega C} + V_{Qe}(f) = v_{out} \tag{6.55}$$

$$v_{in} - v_{out} - 2v_{int} + V_{Qe} \cdot j\omega R\frac{C}{G} = j\omega R\frac{C}{G} \cdot v_{out} \tag{6.56}$$

$$v_{in} - 2v_{int} + V_{Qe} \cdot j\omega R\frac{C}{G} = v_{out} \cdot (1 + j\omega R\frac{C}{G}) \tag{6.57}$$

and finally

$$v_{out} = \overbrace{\frac{1}{1 + j\omega R\frac{C}{G}}}^{STF(f)} \cdot v_{in} + \overbrace{\frac{j\omega R\frac{C}{G}}{1 + j\omega R\frac{C}{G}}}^{NTF(f)} \cdot V_{Qe} + \underbrace{\frac{-2 \cdot v_{int}}{1 + j\omega R\frac{C}{G}}}_{\text{Extra noise/distortion}} \tag{6.58}$$

It would appear that by using a very large gain, G, we can eliminate the lowpass filtering effect of the input signal (and thus pass very wideband signals to the modulator's output, useful for Nyquist-rate analog-to-digital conversion) and remove the modulation noise from the output of the modulator. The extra noise/distortion term, however, remains in the modulator's output. Again, the only way to get rid of the noise/distortion term is to hold v_{int} fixed so that it doesn't vary. This can be accomplished using relatively large f_s or an active element discussed next.

Before getting too excited about removing the modulation noise we'll find out, in the next chapter, that we can think of the comparator as also having a gain, G_c, in series with the added amplifier that varies keeping the forward gain of the modulator (a feedback system) equal to unity. In other words, if we increase the amplifier gain G we get an effective decrease in the comparator's gain G_c.

6.2.4 Improving Linearity Using an Active Circuit

Figure 6.28a shows the integrating topology we've used in our passive modulator. The input to the comparator, v_{int}, in this circuit can be written as

$$v_{int} = i_{in} \cdot \frac{1}{j\omega C} \tag{6.59}$$

In (b) we've replaced the passive integrator (the capacitor) with an active integrator. We can write

$$v_c = -G \cdot v_{int} \text{ and } i_{in} = \frac{v_{int} - v_c}{1/j\omega C} \tag{6.60}$$

If the amplifier's gain, G, is big we can write

$$v_c \approx -i_{in} \cdot \frac{1}{j\omega C} \tag{6.61}$$

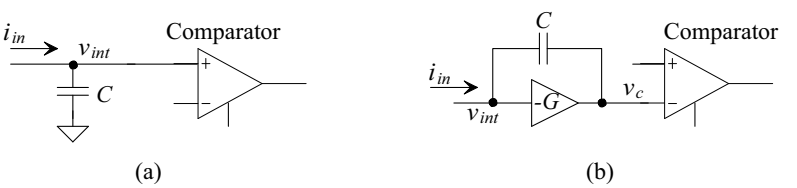


Figure 6.28 Replacing the passive integrator (a) with an active integrator (b).

where we've switched the inputs of the comparator to account for the inversion. Remember our goal is to keep v_{int} constant so that we reduce the noise/distortion term in, for example, Eq. (6.58). We can then write

$$v_{int} \approx \frac{i_{in}}{j\omega C \cdot G} \tag{6.62}$$

As $G \to \infty$ we get $v_{int} \to 0$. Figure 6.29 shows the implementation of a first-order continuous-time noise-shaping modulator using an active integrator. The same equations derived earlier, Eqs. (6.12), (6.19), and (6.20), apply to this configuration.

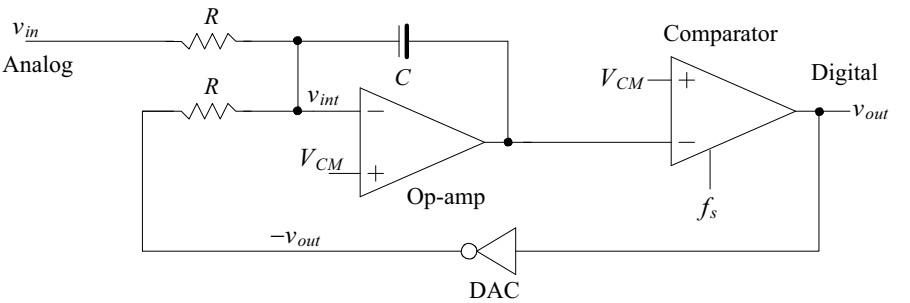


Figure 6.29 An active-integrator NS modulator.

Example 6.4

Repeat Ex. 6.1 using the modulator seen in Fig. 6.29.

The simulation results are seen in Fig. 6.30. In the simulation we can show that v_{int} doesn't vary (the point of adding the op-amp to the modulator). In order to show the better performance in linearity/distortion let's pass the 1-bit digital output through an average of 16 filter, see Ex. 6.2, and regenerate the results seen in Fig. 6.16 (see Fig. 6.31). Clearly, the active topology in Fig. 6.29 shows better linearity than the passive topology seen in Fig. 6.4. ■

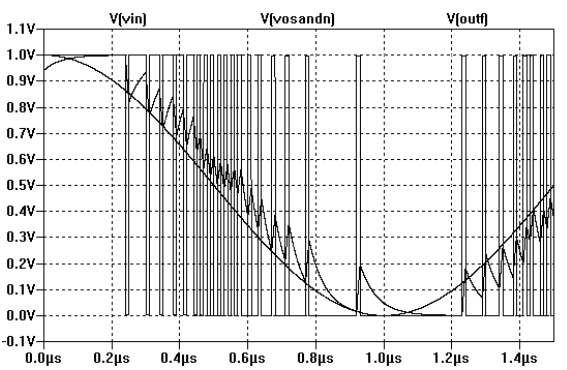


Figure 6.30 Repeating Ex. 6.1 for the first-order active NS modulator.

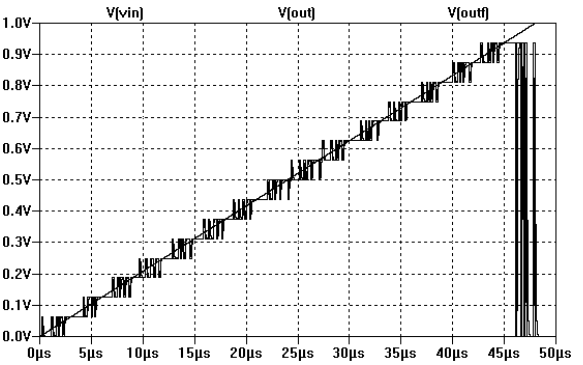


Figure 6.31 Linearity of the active NS modulator, compare to Fig. 6.16.

Second-Order Noise-Shaping

Figure 6.32 shows a second-order active noise-shaping modulator based on the passive topology seen in Fig. 6.17. Knowing that all voltages are referenced to V_{CM} (so that we don't include V_{CM} in the following derivations to keep the equations simpler) we can write

$$v_1 = -\left(\frac{v_{in} - v_{out}}{R}\right) \cdot \frac{1}{j\omega C} \tag{6.63}$$

$$v_2 = -\left(\frac{v_1 + v_{out}}{R}\right) \cdot \frac{1}{j\omega C} \tag{6.64}$$

Treating the comparator as adding noise to v_2, Fig. 6.4,

$$v_{out} = v_2 + V_{Qe}(f) \tag{6.65}$$

we can write

$$\left((v_{in} - v_{out}) \cdot \frac{1}{j\omega RC} - v_{out}\right) \cdot \frac{1}{j\omega RC} + V_{Qe} = v_{out} \tag{6.66}$$

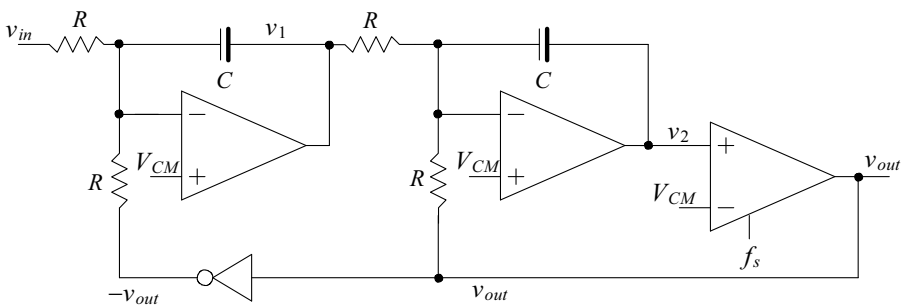


Figure 6.32 Second-order noise-shaping modulator, version I.

and finally

$$v_{out} = \overbrace{\frac{1}{(j\omega RC)^2 + j\omega RC + 1}}^{STF} \cdot v_{in} + \overbrace{\frac{(j\omega RC)^2}{(j\omega RC)^2 + j\omega RC + 1}}^{NTF} \cdot V_{Qe} \tag{6.67}$$

The *STF* has a second-order response, Sec. 3.2.2. Poor selection of the resistor and capacitor will cause instability. Note that for low frequencies the *NTF* increases as the square of frequency so we expect better *SNR*, for a given bandwidth *B* (see Eq. [6.15]), using this topology. Let's try to make this topology more robust by using only a single feedback path, Fig. 6.33. The transfer relationship for this modified topology is then

$$v_{out} = \overbrace{\frac{1}{(j\omega RC)^2 + 1}}^{STF} \cdot v_{in} + \overbrace{\frac{(j\omega RC)^2}{(j\omega RC)^2 + 1}}^{NTF} \cdot V_{Qe} \tag{6.68}$$

Reviewing Fig. 3.35, the poles fall on the y-axis and so the topology is unstable.

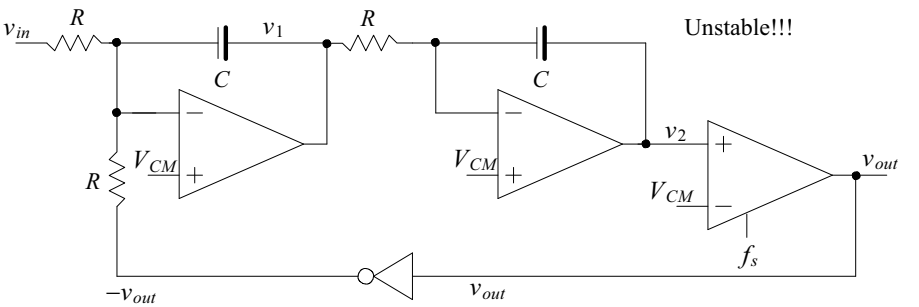


Figure 6.33 Second-order noise-shaping modulator with a single feedback path (bad).

Consider the single-feedback path modulator seen in Fig. 6.34. We've added a resistor in series with the feedback capacitor in the first integrator. We can now write

$$v_1 = -\left(\frac{v_{in} - v_{out}}{R}\right) \cdot \left(\frac{1}{j\omega C} + R\right) \tag{6.69}$$

$$v_2 = -\left(\frac{v_1}{R}\right) \cdot \frac{1}{j\omega C} = (v_{in} - v_{out}) \cdot \frac{1}{j\omega RC} \cdot \left(\frac{1}{j\omega RC} + 1\right) \tag{6.70}$$

$$v_{out} = \overbrace{\frac{j\omega RC + 1}{(j\omega RC)^2 + j\omega RC + 1}}^{STF} \cdot v_{in} + \overbrace{\frac{(j\omega RC)^2}{(j\omega RC)^2 + j\omega RC + 1}}^{NTF} \cdot V_{Qe} \tag{6.71}$$

The benefits of this topology, other than the better *SNR* and only a single feedback loop, are that we can select *RC* so that the *STF* is closer to one over a wider bandwidth and there is smaller delay between the input and output of the modulator (which is of critical importance in a *K*-path topology). Setting, for example,

$$RC = 2T_s = 2/f_s \tag{6.72}$$

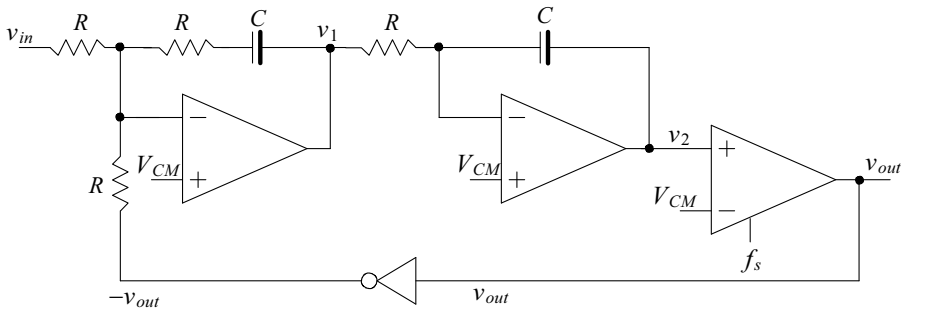


Figure 6.34 Second-order noise-shaping modulator, version II.

this equation reduces to, for frequencies of interest much less than the Nyquist frequency of $f_s/2$,

$$v_{out} \approx v_{in} + (j\omega RC)^2 \cdot V_{Qe} \tag{6.73}$$

Signal-to-Noise Ratio

Following the procedure for calculating *SNR* seen in Sec. 6.1.1

$$V_{noise,RMS}^2 = 2\int_0^B |NTF(f)|^2 |V_{Qe}(f)|^2 \cdot df = 2 \cdot \frac{V_{LSB}^2}{12 f_s} \cdot \int_0^B (2\pi f \cdot RC)^4 \cdot df \tag{6.74}$$

$$V_{noise,RMS}^2 = 2 \cdot \frac{V_{LSB}^2}{12 f_s} \cdot (2\pi RC)^4 \cdot \frac{B^5}{5} \tag{6.75}$$

Again with $B = f_s/2K$ we get

$$V_{noise,RMS}^2 = \frac{V_{LSB}^2}{12} \cdot (2\pi RC)^4 \cdot \frac{f_s^4}{80 \cdot K^5} \tag{6.76}$$

$$SNR_{ideal} = 20 \cdot \log \frac{V_p/\sqrt{2}}{V_{noise,RMS}} = 6.02N + 1.76 - 20\log \frac{(2\pi RC \cdot f_s)^2}{\sqrt{80}} + 20\log K^{5/2} \tag{6.77}$$

Setting $RC = 2.69/f_s$ (noting that we might have to increase the *RC* to avoid saturating the integrators, discussed in more detail in the next chapter)

$$SNR_{ideal} = 6.02N + 1.76 - 30.10 + 50\log K \tag{6.78}$$

$$N_{inc} = \frac{50\log K - 30.10}{6.02} \tag{6.79}$$

$$SNR_{ideal} = 6.02(N + N_{inc}) + 1.76 \tag{6.80}$$

For every doubling in *K* above *K* = 4 we get 2.5 bits increase in resolution or 15 dB increase in SNR_{ideal}. To estimate the order, *L*, of the decimating filter let's write, see Eq. (6.21),

$$L \cdot \log_2 K \geq \frac{50\log K - 30.10}{6.02} \tag{6.81}$$

For $16 \leq K \leq 1024$ we can use a second-order filter, *L* = 2.

Example 6.5

Simulate the operation of the second-order NS modulator in Fig. 6.34 clocked at 100 MHz, with $RC = 20$ ns, and decimated with a filter having a transfer function

$$\left[\frac{1-z^{-16}}{1-z^{-1}}\right]^2$$

Estimate the bandwidth, B, of the output signal, the increase in the number of bits, N_{inc}, and SNR_{ideal}.

The simulation results are seen in Fig. 6.35. The final output clock frequency is 6.25 MHz and the bandwidth of the desired signal, B, is 3.125 MHz. Using Eq. (6.79) we estimate the increase in the number of bits as 5. Using Eq. (6.80) the ideal SNR is 37.88 dB. Note that the number of bits coming out of the filter is 9 bits, the input 1-bit word size increases 8-bits. We can throw the lower 5-bits out or throw the MSB out to divide by 2 and throw the lower 4-bits out (just not continue to pass them along in the system since they are simply noise). ■

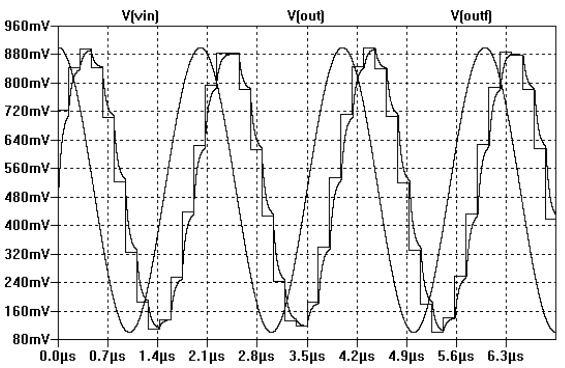


Figure 6.35 Simulation results for Ex. 6.5.

Discussion

The second-order active NS modulator is the workhorse for analog-to-digital converters using noise-shaping. The increase in resolution of 2.5 bits for every doubling in K is significant. This topology can also be used in a K-path configuration, Fig. 6.24, replacing the capacitor and amplifier (see simulation examples at CMOSedu.com). The challenge is keeping the forward delay through the modulator small (so the modulator remains stable). This dictates using simple op-amp topologies that are very fast with moderate gains, e.g., self-biased diff-amps. Finally, for high-speed we focused on using K-path topologies. The drawback of this approach is the need for several clock phases whose rising edges are spaced by T_s/K. A delay-locked loop (DLL) can be used for generating these clocks and is straightforward to design. The benefits of the K-path approach are that the matching of the resistors undergoes averaging via the K feedback paths, the pulse rising/falling edges are made less important since relatively wide pulses are used in each feedback path, and there is an inherent filtering when we combine the outputs of the paths together. Clearly further research in the design of these topologies is warranted; however, we leave this work to the refereed literature and continue to focus on the fundamentals.

ADDITIONAL READING

[1] J. C. Candy and G. C. Temes (eds.), *Oversampling Delta-Sigma Data Converters*, IEEE Press, 1992. ISBN 0-87942-285-8

[2] S. K. Tewksbury and R. W. Hallock, *Oversampled, Linear Predictive and Noise-Shaping Coders of Order N*>1, IEEE Trans. Circuits and Sys., Vol. CAS-25, pp. 436-447, July 1978.

[3] H. Inose, Y. Yasuda, *A Unity Bit Coding Method by Negative Feedback*, Proc. IEEE, Vol. 51, pp. 1524-1535, November 1963

QUESTIONS

6.1 Suggest a topology for a passive-integrator NS modulator where the input and fed back signals are currents. Derive a transfer function for your design. Does your topology have the extra noise/distortion term seen in Eq. (6.12)? Why or why not? Simulate the operation of your design.

6.2 Simulate the operation of the NS modulator seen in Fig. 6.4a but using a 4-bit quantizer (ADC). Use a 100 MHz clock frequency and an input sinewave at 500 kHz (as used to generate Fig. 6.7).

6.3 Using Eqs. (6.14) and (6.17) compare the noise performance of passive NS modulators using a 1-bit quantizer to those using a 4-bit quantizer.

6.4 Repeat Ex. 6.2 if C is changed to 1 pF and a 1 GHz clock frequency is used. Estimate the frequency where the output of the digital filter is −3 dB (0.707) from the input signal. Verify your answer with simulations.

6.5 Suppose the comparator used in the NS modulator and filter used in Ex. 6.2 has a 50 mV input-referred offset voltage. How will this offset voltage affect the conversion from analog to digital? Verify your answer with SPICE simulations.

6.6 Figure 6.36 shows the implementation of an op-amp using mixed-signal design techniques. Assuming the comparator is powered with a 1 V supply, simulate the circuit in the inverting op-amp configuration with the non-inverting input held at 0.5 V, a 10k resistor connected from the inverting input to the input source, and a feedback resistor of 100k from the op-amp's output back to the inverting input (for a closed loop gain of −10). Set the input source to have a DC offset of 500 mV, and a peak-to-peak amplitude of 20 mV at 500 kHz. Explain how the circuit operates. Note that using an active integrator, instead of the passive integrator results in more ideal behavior (less variation on the op-amp's inputs).

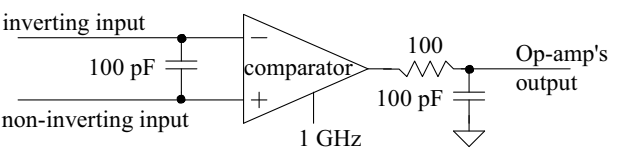


Figure 6.36 An op-amp implemented using mixed-signal techniques.

6.7 In your own words explain why dead zones in the second-order passive modulator seen in Fig. 6.17 are less of a problem than the first-order modulator seen in Fig. 6.4a.

6.8 Verify, using simulations, that the modulator seen in Fig. 6.20 suffers from capacitor mismatch while the one in Fig. 6.22 does not.

6.9 What is a time-interleaved data converter? Why is a time-interleaved converter different from the converter seen in Fig. 6.24?

6.10 Show the details of how to derive the transfer function of the path filter seen in Fig. 6.24.

6.11 Repeat question 6.7 if an active integrator, Fig. 6.28, is used in place of the passive integrator.

6.12 Repeat Ex. 6.5 if K is changed from 16 to 8.