

# Noise-Shaping Data Converters

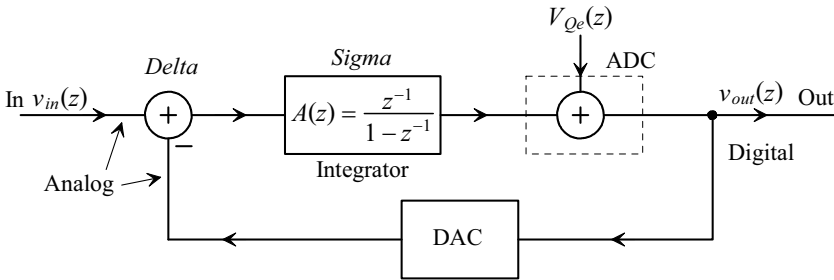
In this chapter we continue our discussion of first-order noise-shaping data converters. We start out discussing first-order topologies and then move on to higher-order topologies including second-order noise-shaping and cascaded modulators.

## 7.1 First-Order Noise Shaping

The block diagram of a NS feedback modulator is shown in Fig. 7.1. At the end of Ch. 5 we showed, but in the  $s$  domain, that the output of the modulator,  $v_{out}(z)$ , can be related to the input,  $v_{in}(z)$ , and the ADC's quantization noise,  $V_{Qe}(z)$ , by

$$v_{out}(z) = \underbrace{\frac{A(z)}{1+A(z)}}_{STF(z)} \cdot v_{in}(z) + \underbrace{\frac{1}{1+A(z)}}_{NTF(z)} \cdot V_{Qe}(z) \quad (7.1)$$

where, as in the last chapter,  $STF(z)$  is the signal's transfer function and  $NTF(z)$  is the noise's transfer function.



**Figure 7.1** Block diagram of a noise-shaping (NS) modulator.

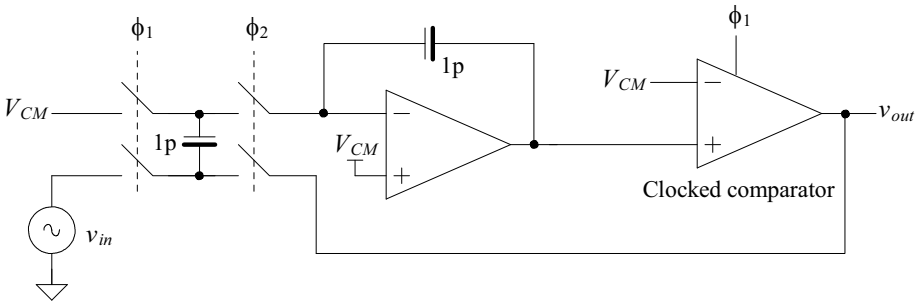
Consider what happens if  $A(z)$  is an integrator (implemented using a DAI, Sec. 2.2.3) as shown in the figure. Equation 7.1 becomes

$$v_{out}(z) = z^{-1} v_{in}(z) + (1 - z^{-1}) \cdot V_{Qe}(z) \quad (7.2)$$

This equation is important! It shows that the input signal simply passes through the modulator with a delay while the quantization noise is differentiated (see Fig. 1.20 for the magnitude response of a digital differentiator with a transfer function  $1 - z^{-1}$ ). We can think of the noise differentiation as pushing the quantization noise to higher frequencies. We'll come back to how NS affects the quantization noise spectral density,  $V_{qe}(f)$ , in a moment. But first let's attempt to understand what's happening here.

In Fig. 7.1 the summer takes the difference (*Delta*) between the input signal and the fed back signal. The integrator accumulates or sums (*Sigma*) this difference and feeds the result back, via the ADC and DAC, to the summer. This forces the output of the modulator to track the average of the input. Sometimes the fed back signal will have a value greater than the input signal, while at other times the fed back signal will be less than the input signal. The *average* signal fed back, however, should ideally be the same as the input signal. Note that this type of NS modulator is often called a *Delta-Sigma* or *Sigma-Delta* modulator. Also, at this point, we should see the need for the averaging filters discussed earlier.

A circuit implementation of a first-order NS modulator is shown in Fig. 7.2. For the moment we use a single-bit ADC and DAC (both implemented using the clocked comparator) for gain linearity reasons (discussed in more detail later). The analog voltage coming out of the integrator is compared to the common-mode voltage (this is our 1-bit ADC) using the comparator. For the 1-bit DAC a logic-0 has an analog voltage of  $0 V$ , while a logic-1 has an analog voltage of  $V_{DD}$  ( $= 1 V$  here) so that the comparator's output can be used directly (fed back to the DAC).



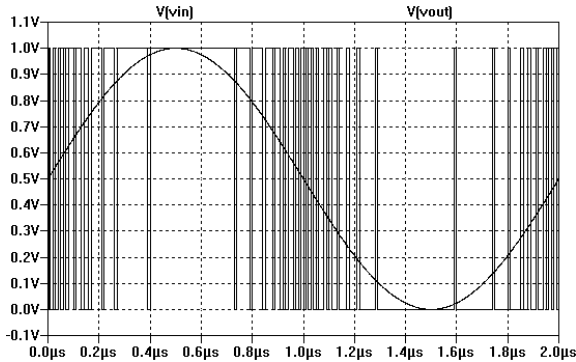
**Figure 7.2** Circuit implementation of a first-order NS modulator.

The comparator is clocked on the rising edge of  $\phi_1$  resulting in a  $T_s$  delay ( $z^{-1}$ ) in series with the fed back signal and a delay of  $T_s/2$  ( $z^{-1/2}$ ) in series with the input signal. To understand this statement, remember that the nonoverlapping clock dead time (the time both  $\phi_1$  and  $\phi_2$  are low) is short and, practically, the falling edge of  $\phi_2$  occurs at the same instance as the rising edge of  $\phi_1$  (and so we could also use  $\overline{\phi_2}$  to clock the comparator). This results in a transfer function, see Table 2.2, to the input of the comparator (which can also be thought of as the ADC output since the fed back signal and modulator output are the same signal) of

$$\text{Desired ADC input/output} = \frac{z^{-1}}{1 - z^{-1}}(v_{in} - v_{out}) \quad (7.3)$$

After careful review we should see that the circuit implementation of Fig. 7.2 corresponds to the NS modulator represented by the block diagram shown in Fig. 7.1.

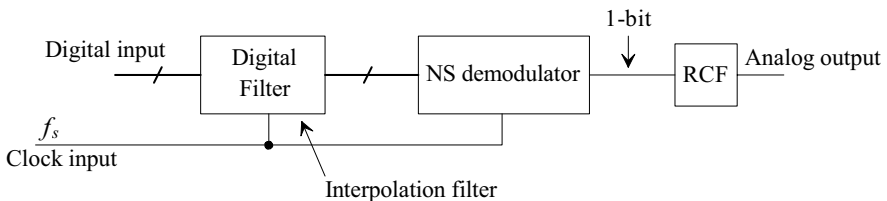
We can use the SPICE models developed earlier to demonstrate the operation of the NS modulator of Fig. 7.2. Assuming our sampling frequency is 100 MHz, the input is a 500 kHz sinewave centered around  $V_{CM}$  ( $= 0.5$  V) with a peak amplitude of 0.5 V. The input and output of the modulator are shown in Fig. 7.3.



**Figure 7.3** Simulating the operation of the modulator in Fig. 7.2.

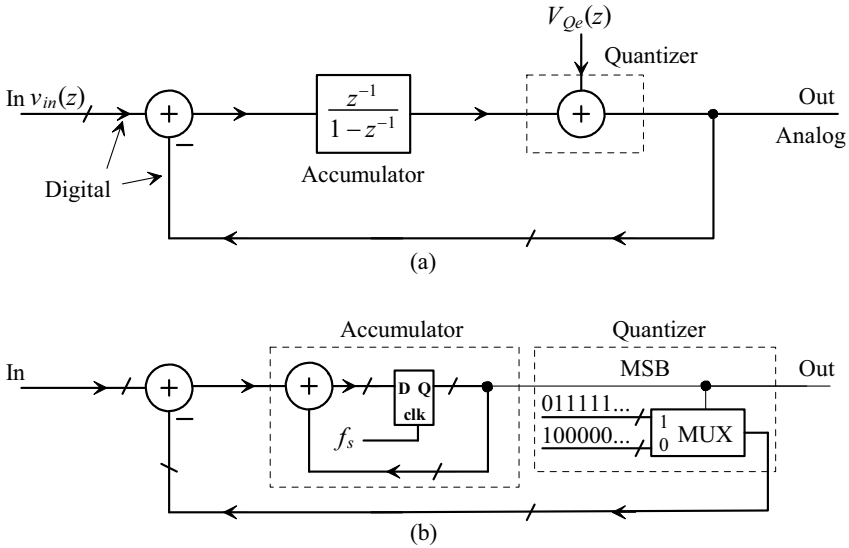
#### *A Digital First-Order NS Demodulator*

So far our noise-shaping discussion has centered around analog-to-digital conversion. Figure 7.4 shows a first-order NS demodulator-based topology for digital-to-analog conversion. While the discussion concerning selection of the digital interpolating and reconstruction filters is given in Ch. 4, we are interested here in the topology of the first-order NS demodulator for use in a DAC.



**Figure 7.4** DAC using a NS modulator and digital filter.

Figure 7.5a shows a block diagram of a first-order NS demodulator for use in a DAC. Figure 7.5b shows the practical implementation. The only differences between this circuit and the circuit of Fig. 7.1 is that the DAI is replaced with an all-digital integrator (see Fig. 1.28), and the quantizer (comparator) is replaced with a circuit that performs quantization by selecting (using the MSB of the accumulator output word) digital  $V_{REF+}$  ( $= 011111$  in two's complement) or  $V_{REF-}$  ( $= 100000$  in two's complement) which, for our current discussion, are  $V_{DD}$  and ground. Note that this topology isn't the preferred way to implement a DAC using noise-shaping. Using the error-feedback topology, discussed later, is the preferred method.



**Figure 7.5** Block diagram of (a) a NS demodulator and, (b) a more detailed implementation for use in a DAC.

**7.1.1 Modulation Noise in First-Order NS Modulators**

Here we present a more detailed discussion of the quantization noise spectrum for a first-order NS modulator. To begin, let's write Eq. (7.1) in the time domain,

$$v_{out}[nT_s] = v_{in}[(n - 1)T_s] + v_{Qe}[nT_s] - v_{Qe}[(n - 1)T_s] \tag{7.4}$$

which shows the output is a function of the first difference (order) of the quantization noise  $v_{Qe}[nT_s] - v_{Qe}[(n - 1)T_s]$ . Intuitively note that the smaller we make  $T_s$  (the faster we sample since  $T_s = 1/f_s$ ), the closer our digital output  $v_{out}[nT_s]$  approaches the analog input  $v_{in}[nT_s]$ .

Next, using Eq. (7.1), let's write the product of the noise transfer function and  $v_{Qe}[z]$  (the modulation noise) of the first-order NS modulator in the frequency domain as

$$NTF(z)V_{Qe}(z) = (1 - z^{-1})V_{Qe}(z) \rightarrow NTF(f)V_{Qe}(f) = \left(1 - e^{-j2\pi\frac{f}{f_s}}\right) \cdot \frac{V_{LSB}}{\sqrt{12f_s}} \tag{7.5}$$

where we have used, see Fig. 5.12,

$$V_{Qe}(f) = \frac{V_{LSB}}{\sqrt{12f_s}} \left(\text{units, V}/\sqrt{\text{Hz}}\right) \text{ for } 0 \leq f \leq f_s/2 \tag{7.6}$$

and, once again (see Eq. [4.1] or, for the 1-bit ADC [comparator], Eq. [6.1]),

$$V_{LSB} = \frac{V_{REF+} - V_{REF-}}{2^N} \tag{7.7}$$

where  $N$  is the number of bits used in the low-resolution ADC/DAC in the modulator. Using a single-bit ADC/DAC in a NS modulator,  $N = 1$ , results in this book in  $V_{LSB} = 1$  V. This again shows that we are not reducing the quantization noise, but are pushing it to higher frequencies so that it can be filtered out. Using Eq. (1.46), we can write the PSD of the  $NTF$  as

$$|NTF(f)|^2 \cdot |V_{Qe}(f)|^2 = \frac{V_{LSB}^2}{12f_s} \cdot 4 \sin^2 \pi \frac{f}{f_s} \quad \left( \text{units, V}^2/\text{Hz} \right) \quad (7.8)$$

Figure 7.6 shows the PSD of the first-order NS modulation noise for  $V_{LSB} = 1$  V and  $f_s = 100$  MHz. Note that we are discussing modulation noise instead of quantization noise. *The modulation noise is the quantization noise after being differentiated by the NS modulator.* The modulation noise is the unwanted signal added to the input signal. After reviewing Fig. 7.6 we see that the magnitude of the modulation noise is significant. However, after passing this signal through a lowpass filter, we can remove the higher frequency noise resulting in a lower value of data converter RMS quantization noise,  $V_{Qe,RMS}$ . By restricting the bandwidth of the modulation noise we can drive the RMS quantization noise in our signal to zero. Of course, by lowering the bandwidth of the digital filter on the output of the modulator we also limit the possible bandwidth,  $B$ , of the input signal. Notice that we have violated Bennett's criteria, Sec. 5.1.1, by utilizing a quantizer with an LSB that is comparable to the input signal. Now, however, we are using feedback that adds or subtracts a signal from the input and ultimately affects the quantizer input.

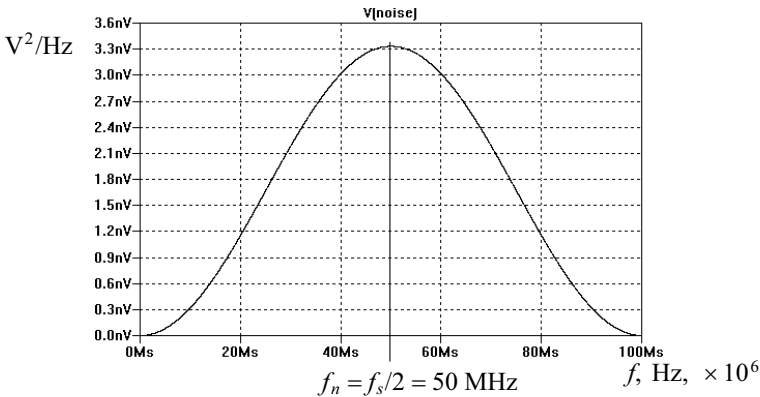


Figure 7.6 Modulation noise for a first-order NS modulator.

### 7.1.2 RMS Quantization Noise in a First-Order Modulator

The RMS quantization noise present in a bandwidth,  $B$ , can be calculated, see Eq. (6.13), using

$$V_{Qe,RMS}^2 = 2 \int_0^B |NTF(f)|^2 |V_{Qe}(f)|^2 \cdot df = 2 \cdot \frac{V_{LSB}^2}{12f_s} \cdot 4 \cdot \int_0^B \sin^2 \pi \frac{f}{f_s} \cdot df \quad (7.9)$$

Remembering that the maximum bandwidth of our input signal is related to the sampling frequency,  $f_s$ , and the oversampling ratio,  $K$ , by

$$B = \frac{f_s}{2K} \quad (7.10)$$

and, for small values of  $x$ ,

$$\sin x \approx x \quad (7.11)$$

then

$$V_{Qe,RMS} \approx \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\pi}{\sqrt{3}} \cdot \frac{1}{K^{3/2}} \quad (7.12)$$

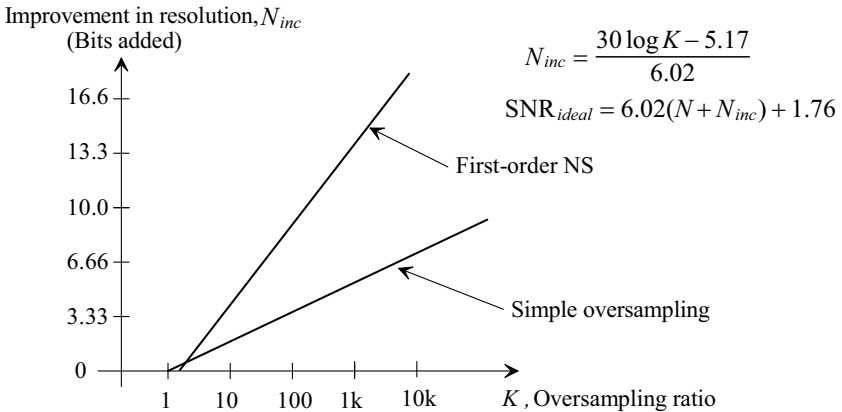
This equation should be compared to Eq. (5.56). Further, we can describe the ideal data converter SNR using first-order NS, see Eqs. (5.10) - (5.13) as

$$SNR_{ideal} = 20 \cdot \log \frac{V_p / \sqrt{2}}{V_{Qe,RMS}} = 6.02N + 1.76 - 20 \log \frac{\pi}{\sqrt{3}} + 20 \log K^{3/2} \quad (\text{in dB}) \quad (7.13)$$

or

$$SNR_{ideal} = 6.02N + 1.76 - 5.17 + 30 \log K \quad (\text{in dB}) \quad (7.14)$$

This equation should be compared to Eq. (5.58) where we saw every doubling in the oversampling ratio,  $K$ , results in a 0.5-bit increase in resolution (called simple oversampling). Here we see that *every doubling in the oversampling ratio results in 1.5 bits increase in the resolution* (or a 9 dB increase in  $SNR_{ideal}$ ). A first-order NS modulator's performance is compared to simple oversampling in Fig. 7.7 (see also Sec. 6.1.1 and Fig. 6.9).



**Figure 7.7** Comparing simple oversampling to first-order noise-shaping.

### Example 7.1

Determine the ideal signal-to-noise ratio and the maximum signal bandwidth allowed,  $B$ , for the first-order NS modulator of Fig. 7.1 if 16 of its output samples are averaged ( $K = 16$ ).

Because the sampling frequency,  $f_s$ , is 100 MHz, we can use Eq. (7.10) to determine the maximum input signal bandwidth,  $B$ , is 3.125 MHz. Using Eq.

(7.14) we can solve for the  $SNR_{ideal}$  as (knowing that the NS modulator of Fig. 7.1 uses a 1-bit quantizer) 38.73 dB. This corresponds to an equivalent data converter (ADC) resolution, using Eq. (5.13), of 6.14 bits (number of bits added is 5.14). Note that the ADC is made with the components, modulator, and digital filter, shown in Fig. 6.1. ■

### 7.1.3 Decimating and Filtering the Output of a NS Modulator

It's important to note that Eq. (7.14) was derived assuming the output of the modulator was passed through a perfect lowpass filter with a bandwidth of  $B$ . Passing the output through a Sinc averaging filter, see Figs. 4.10 and 4.13, will result in a poorer SNR because the higher frequency noise components will not be entirely filtered out. In this section we want to answer two questions: (1) what order,  $L$  (see Eq. [4.19]), of Sinc averaging filter should be used in the digital filter on the output of the NS modulator, and (2) assuming we use only this filter (no additional filtering), how will the ideal SNR of the first-order NS modulator be affected.

We begin to answer to the first question by writing the increase in the number of bits,  $N_{inc}$ , as

$$N_{inc} = \frac{30 \log K - 5.17}{6.02} \quad (7.15)$$

If our NS modulator uses a 1-bit ADC, then the final, after the digital filter, resolution of the resulting data converter is  $N_{inc} + 1$  bits. (An NS modulator using a 5-bit ADC [often called a multibit NS modulator] would ideally have an output resolution of  $N_{inc} + 5$  bits.) Further, we saw in Sec. 4.2.5 that the word size increased by  $\log_2 K$  bits in each stage so that we can require

$$L \cdot \log_2 K \geq \frac{30 \log K - 5.17}{6.02} \quad (7.16)$$

Solving this equation results in  $L$  being greater than or equal to 2. In general, we can write

$$L = 1 + M \quad (7.17)$$

where  $M$  is the order of the modulator. For a first-order modulator we use two stages in the averaging filter, or,

$$H(z) = \left[ \frac{1}{K} \frac{1 - z^{-K}}{1 - z^{-1}} \right]^2 \quad (7.18)$$

In the next section we discuss second-order NS modulators ( $M = 2$ ). For these modulators we use a Sinc averaging filter with  $L = 3$ .

#### Example 7.2

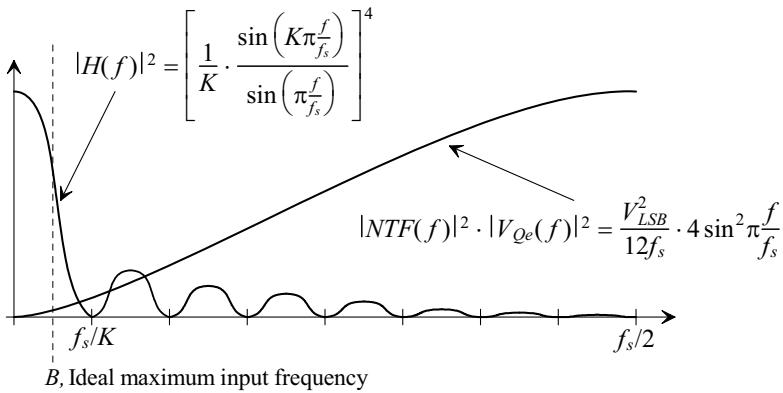
Comment on the implementation of the digital decimation filter for the modulator described in Ex. 7.1. Assume the final output clocking frequency is 100 MHz/16 or 6.25 MHz.

The transfer function of the digital filter is

$$H(z) = \left[ \frac{1 - z^{-16}}{1 - z^{-1}} \right]^2$$

The block diagram of the filter is seen in Fig. 4.32 using 4 stages and  $L = 2$ . The increase in resolution through each  $(1 + z^{-1})^2$  stage is 2 bits (see Fig. 6.10 for the filter when  $L = 1$ ). The resolution calculated in Ex. 7.1 was 6.14 bits, which we round up to 7-bits. Because the output of the digital filter is 9-bits (8-bits through the four stages plus the 1-bit coming out of the modulator), we drop the lower two bits (divide by 4) to get our final 7-bit resolution. ■

Next let's examine how filtering with a Sinc filter affects the SNR of the data converter. Remember the  $SNR_{ideal}$  was calculated in Eq. (7.14) assuming the modulation noise was strictly bandlimited to  $B$ . Figure 7.8 shows the PSD of the  $NTF^2(f) \cdot |V_{Qe}(f)|^2$  (the modulation noise) of the first order NS modulator. Also shown in this figure is the shape of the averaging filter's magnitude response squared, Eq. (4.20). Here we are showing the shape of a filter with  $L = 2$  (set by Eq. [7.17] for a first-order modulator) and  $K = 16$ . We limit our range to  $f_s/2$ .



**Figure 7.8** Showing modulation noise and filter response.

We can calculate the RMS quantization noise on the output of the Sinc filter in a cascade of a first-order modulator and an averaging filter using (see Sec. 6.1.2)

$$V_{Qe,RMS}^2 = 2 \int_0^{f_s/2} |NTF(f)|^2 \cdot |V_{Qe}(f)|^2 \cdot |H(f)|^2 \cdot df \tag{7.19}$$

$$V_{Qe,RMS}^2 = \frac{V_{LSB}^2}{12f_s} \cdot \frac{8}{K^4} \cdot \int_0^{f_s/2} \frac{\sin^4(K\pi\frac{f}{f_s})}{\sin^2(\pi\frac{f}{f_s})} \cdot df \tag{7.20}$$

If we let  $\theta = \pi \frac{f}{f_s}$ , then this equation can be written as

$$V_{Qe,RMS}^2 = \frac{V_{LSB}^2}{12f_s} \cdot \frac{8}{K^4} \cdot \frac{f_s}{\pi} \cdot \int_0^{\overbrace{\frac{\pi}{2}}^{=K \cdot \frac{\pi}{4}}} \frac{\sin^4(K\theta)}{\sin^2\theta} d\theta \tag{7.21}$$



and finally,

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\sqrt{2}}{K^{3/2}} \quad (7.22)$$

This equation should be compared to Eq. (7.12), which was derived assuming the digital filter was ideal with a bandwidth of  $B$ . The  $SNR$  resulting from using a first-order ( $M = 1$ ) NS modulator and a second-order ( $L = 2$ ) Sinc averaging filter is

$$SNR_{Sinc} = 6.02N + 1.76 - 3.01 + 30 \log K \text{ (in dB)} \quad (7.23)$$

Comparing this to  $SNR_{ideal}$  given in Eq. (7.14), we see that using a Sinc filter for averaging results in only a 2.16 dB difference (increase) in SNR over the ideal filter. If we remember that using a Sinc filter results in a droop in the desired signal, Fig. 2.31, the  $SNR$  will be lower than what is predicted by Eq. (7.23). (Note that an analysis of higher order modulators using Sinc averaging filters would show that as long as Eq. [7.17] is valid the deviation from  $SNR_{ideal}$  is negligible.)

#### 7.1.4 Pattern Noise from DC Inputs (Limit Cycle Oscillations)

In the ideal Nyquist-rate ADC, a DC input signal results in a single output code. In other words the output code doesn't vary. In a NS-based ADC the output code varies as seen in Fig. 7.3 (the average of the output is equal to the input signal). When this code is applied to a digital filter the output of the filter shows a ripple or variation. Unfortunately, this ripple on the output of the filter can cause noise in the spectrum of interest. The frequency of the ripple and the amplitude of the ripple depend on the DC input value. Figure 7.9 shows an example of this ripple. The input signal for the modulator in Fig. 7.2 is 0.5 V (the common-mode voltage) while the modulator is clocked at 100 MHz. The modulator's output is a square wave of alternating ones and zeroes. The first harmonic of this signal is at half the clocking frequency or, in this example, 50 MHz. Since the ripple frequency lies outside our base spectrum (which, from Ex. 7.2, is from DC to 3.125 MHz) it will not, in a significant way, affect the SNR. (The digital filter will likely have a zero in its transfer function that falls at half the clocking frequency eliminating the ripple altogether and resulting in a constant filter output value.) If we increase the input signal to 510 mV we get the digital filter output ripple seen in Fig. 7.10. A component of the ripple is at a

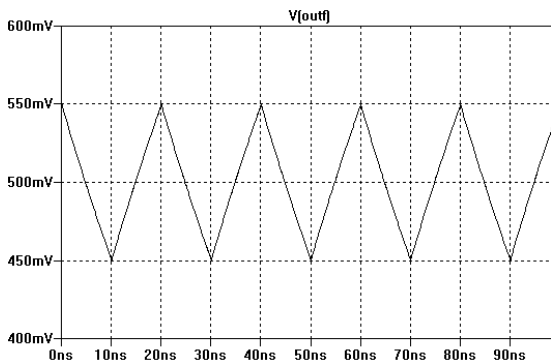
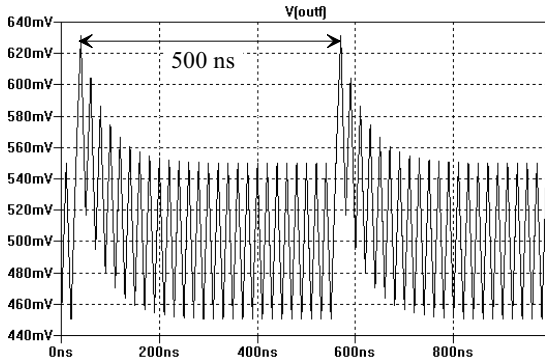
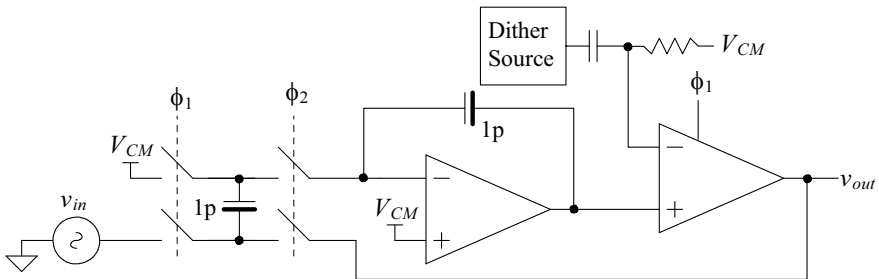


Figure 7.9 Showing how filtering the output of a modulator results in ripple.



**Figure 7.10** Showing a lower frequency ripple in the modulator's output.

frequency that is roughly  $1/500$  ns or 2 MHz, which is well within our base spectrum. The resulting tone will lower the SFDR and the SNR of the data converter. The question now becomes, "How do we minimize the possibility of unwanted tones appearing in the data converter's output spectrum?" Looking at the digital output of the modulator we see that it would be better to spread or flatten the repeating data out so that we don't get repeating tones (as discussed in the dead zone discussion in Sec. 6.1.3). Although we may still have a tone, or repeating sequence, at a frequency in the base spectrum, the amplitude of the tone will be well below the  $V_{Qe,RMS}$  of the data converter (and so it won't affect the SFDR of the data converter). In order to accomplish this spread or randomization we can add a noise dither source (see Sec. 5.3.3) to our basic NS modulator, as seen in Fig. 7.11. By applying the dither to the input of the comparator (quantizer) the dither will be noise-shaped like the quantization noise (the spectral content of the dither, Eq. [5.62], is less important).

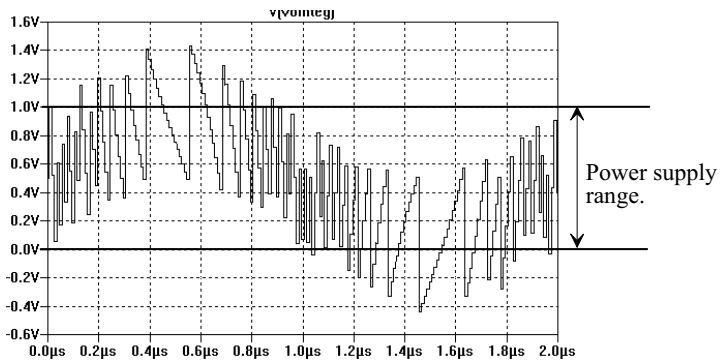


**Figure 7.11** Adding a dither source to a first-order NS modulator.

Finally, note that unwanted tones are usually not a problem if the input signal is busy and random (not DC as discussed in this section). Later in the chapter, we discuss second-order modulators that utilize two integrators. The second integration helps to spread the repeating sequences out over a longer period of time so that, hopefully, negligible unwanted tone energy is present in the base spectrum.

### 7.1.5 Integrator and Forward Modulator Gain

So far we haven't discussed the shape or amplitude of the integrator's output. Because we are using near-ideal components in our simulations, we haven't seen any limitations due to the finite op-amp output swing. Figure 7.12 shows the integrator's output for the input and output signals shown in Fig. 7.3 (using the modulator of Fig. 7.2). Clearly the output swing of the op-amp is beyond the power supply rails. If the transistor-level model of the op-amp were to replace the ideal op-amp, the integrator's output would *saturate* at voltages less than  $V_{DD}$  ( $= 1.0$  V here) or greater than ground. While in some situations op-amp saturation is not necessarily bad (the gain of the integrator goes to zero), it is desirable to understand how decreasing forward loop gain affects the performance of the modulator. Note also, in Fig. 7.12, that the output of the integrator makes the largest change when it passes through the comparator reference voltage,  $V_{CM} = 0.5$  V, since the fed back signal, the comparator output (a full-scale signal), is input to the integrator.



**Figure 7.12** Output swing limitations in the op-amp (integrator).

Consider the linearized model of our first-order NS modulator shown in Fig. 7.13. The gain of the integrator, see Eq. (2.103) or Fig. 2.55, is given by

$$G_I = \frac{C_I}{C_F} \quad (7.24)$$

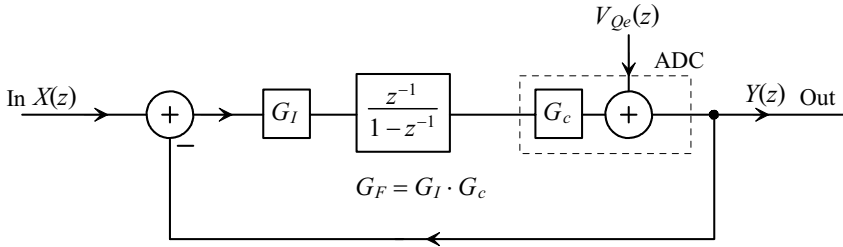
We have also drawn the comparator with a gain. Up until this point we have assumed the gain of the comparator is unity. We'll comment on this more in a moment. Let's define the modulator's forward gain as

$$G_F = G_I \cdot G_c \quad (7.25)$$

We can rewrite Eq. (7.2) using this gain as

$$v_{out}(z) = \frac{z^{-1} \cdot G_F}{1 + z^{-1}(G_F - 1)} \cdot v_{in}(z) + \frac{1 - z^{-1}}{1 + z^{-1}(G_F - 1)} \cdot V_{Qe}(z) \quad (7.26)$$

If  $G_F$  approaches zero (the integrator saturates while the comparator gain stays finite), then the output of the modulator is the sum of the integrated input and the quantization noise. (This is bad.) Since the quantization noise is not spectrally shaped it will be difficult to filter the modulator's output to recover the input signal. If the forward gain is



**Figure 7.13** Block diagram of a NS modulator showing forward gains.

greater than two, then, as seen in Fig. 4.38 and the associated discussion, the poles of the transfer function reside outside the unit circle and the modulator will be unstable. We can restrict the values of the forward gain to

$$0 \leq G_F \leq 2 \quad (7.27)$$

Ideally, however, the gain is one.

### Example 7.3

Show, using SPICE simulations and the modulator of Fig. 7.2, that an integrator gain of 0.4 will result in an op-amp output range well within the power supply range.

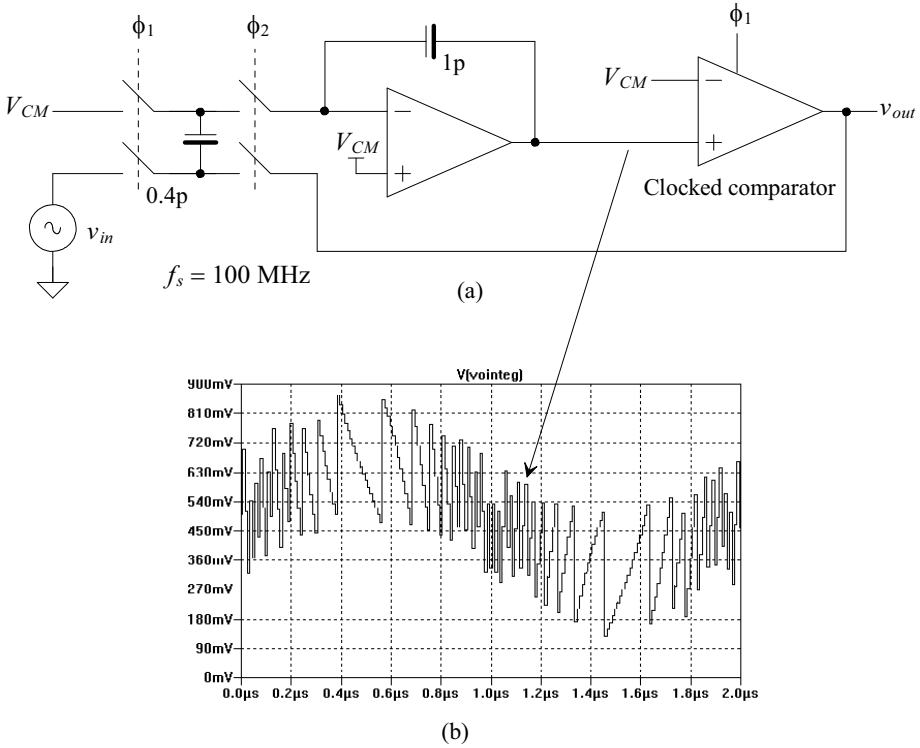
Figure 7.14a shows a schematic of the modulator with  $G_I = 0.4$ . Figure 7.14b shows the output of the integrator (the output of the op-amp) in the modulator of part (a) with the input sinewave shown in Fig. 7.3. The output swing is limited to roughly 80% of the supply range. *For general design it is desirable to set our integrator gain to 0.4.* This ensures our integrator doesn't saturate unless the input to the modulator goes outside the supply voltage range.

It's interesting to note that in both modulators, Fig. 7.2 and Fig. 7.14a, the forward gain is unity. This is a result of the effective gain of the comparator changing forcing the forward gain, controlled by the fed back signal, to unity. What this means is that our modulator functions as expected with a signal gain of one (Eq. [7.2] is valid) whether  $G_I$  is 1 or 0.4. Next we discuss how this change in comparator gain occurs. ■

Figure 7.15 shows the transfer curves for the comparator. The x-axis, the comparator input, is the output of the integrator in our modulator. Shrinking the integrator's output swing while holding the output swing of the comparator at the supply rails (1 V) results in an increase in effective comparator gain. This gain variation, with the integrator output swing, helps to set the forward gain of the modulator to precisely 1. We can write this using equations as

$$\underbrace{\frac{\text{Integrator output}}{\text{Modulator input}}}_{\text{Integrator gain, } G_I} \cdot \underbrace{\frac{\text{Comparator(modulator) output}}{\text{Integrator output}}}_{\text{Comparator gain, } G_c} = \underbrace{\frac{\text{Modulator output}}{\text{Modulator input}}}_{G_F} \quad (7.28)$$

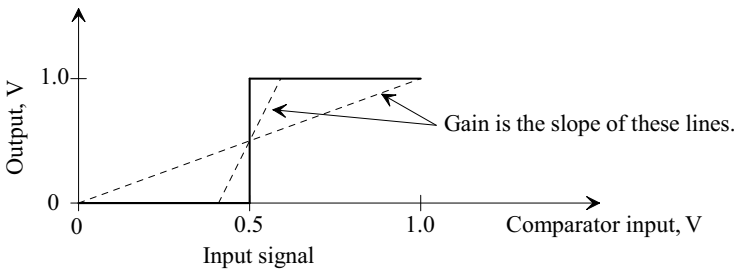
If the modulator is functioning properly, then the average value of the modulator output will be equal to the modulator input and thus  $G_F = 1$ . It's interesting to note that this result



**Figure 7.14** (a) First-order NS modulator with an integrator gain of 0.4, and (b) the output of the op-amp.

(precise integrator gain isn't important) will apply to any integrator that is directly followed by an ADC.

Before leaving this section, let's point out a couple of problems with a noise-shaping modulator that uses a multibit ADC, Fig. 7.16. Since the output of the integrator is the input signal to the ADC, the limited integrator output swing will directly effect the range of ADC output codes. Limiting the range of ADC output codes will then limit the allowable range of modulator inputs unless scaling is used (shifting the output codes or



**Figure 7.15** Comparator gain as a function of input voltage.

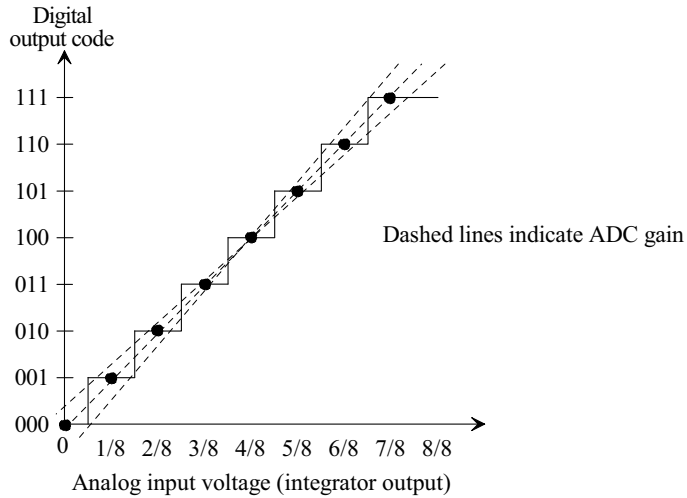


Figure 7.16 A 3-bit ADC.

sizing of capacitors in the DAI). Next, notice in Fig. 7.16 that the variation in the gain of the ADC, with input signal, is more limited than the gains attainable with the simple comparator seen in Fig. 7.15. Limiting the range of ADC gains can result in modulator forward gains that are not exactly unity. This is especially true at high input frequencies where the gain of the integrator is low. However, if the integrator gain is high, the effective gain of the ADC is not important. The point here is that using a multibit ADC will increase the open-loop gain requirements of the op-amp used in the integrator.

7.1.6 Comparator Gain, Offset, Noise, and Hysteresis

It's of interest to determine how the performance of the comparator influences the operation of the modulator. Both the comparator's offset and input-referred noise, Fig. 7.17a, can be referred back to the modulator's input, Fig. 7.17b. By doing so we can determine how they effectively change the input signal seen by the modulator. As seen in Fig. 7.17, the high gain of the integrator,  $A(f)$ , reduces the effect of the comparator's noise and offset on the input signal. For example, if the gain of the integrator at DC is 1,000 and the offset voltage of the comparator is 50 mV, then the input-referred offset is only 50  $\mu$ V.

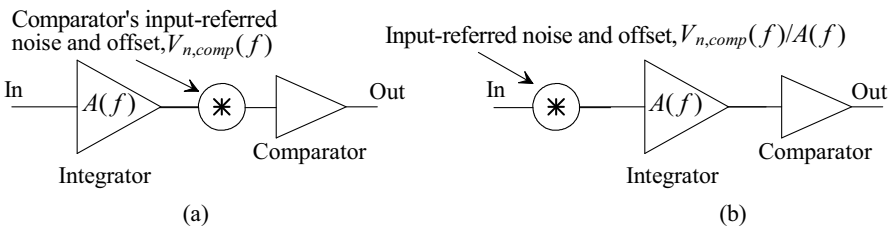


Figure 7.17 (a) Referring the comparator offset and noise to (b) the input of the modulator.

In order to determine the minimum gain and maximum allowable hysteresis requirements of the comparator, let's review Fig. 7.14. We see that when the output of the comparator changes states, the output of the integrator changes by at least

$$\text{Change in integrator output} = G_I \cdot (VDD - V_{CM}) = \frac{C_I}{C_F} \cdot \frac{V_{REF+} - V_{REF-}}{2} \quad (7.29)$$

For the modulator of Fig. 7.14 this equation can be evaluated as 0.2 V. As long as the hysteresis is much less than this value and the gain of the comparator (1/0.2 or 5) is large enough so that the comparator can make a full output transition with this input difference, then the modulator will function properly. Very simple, low-performance comparator designs can be used while not affecting the modulator's performance.

### 7.1.7 Op-Amp Gain (Integrator Leakage)

Now that we've discussed the gain of the comparator, let's determine how high the open-loop gain of the op-amp must be for proper integrator action. With low op-amp gain, some of the charge stored on the integrator's input capacitor,  $C_I$ , is not transferred to the feedback capacitor,  $C_F$ . This loss of charge is sometimes referred to as *integrator leakage*. The charge on the input capacitance effectively leaks off when it is transferred to the feedback capacitance.

We can write the open-loop, frequency-dependent gain of the op-amp as  $A_{OL}(f)$ . The output voltage of the op-amp is then  $v_{out} = A_{OL}(f)(v_+ - v_-)$ , where  $v_+$  is our common-mode voltage  $V_{CM}$  (the noninverting terminal of the op-amp), see Fig. 2.54, and  $v_-$  is the op-amp's inverting input terminal. Following the procedure to derive Eq. (2.102), we can rewrite Eq. (2.100) with finite op-amp gain as

$$Q_2 = C_I \left( V_{CM} - \frac{v_{out}[nT_s]}{A_{OL}(f)} - v_2[nT_s] \right) \quad (7.30)$$

or, rewrite Eq. (2.102) to include the effects of finite op-amp gain to get

$$v_{out}(z) = \frac{C_I}{C_F} \cdot \frac{v_1(z) \cdot z^{-1/2} - v_2(z)}{\left( 1 + \frac{C_I}{C_F A_{OL}(f)} \right) - z^{-1}} \quad (7.31)$$

Using this result in Eq. (7.1) and, as discussed in the last section, assuming the forward gain of the modulator,  $G_F$ , is one gives

$$v_{out}(z) = \frac{z^{-1}}{1 + \frac{C_I}{C_F A_{OL}(f)}} \cdot v_{in}(z) + \frac{1 + \frac{C_I}{C_F A_{OL}(f)} - z^{-1}}{1 + \frac{C_I}{C_F A_{OL}(f)}} \cdot V_{Qe}(z) \quad (7.32)$$

The gain error term

$$\varepsilon_{gain} = \frac{C_I}{C_F} \cdot \frac{1}{A_{OL}(f)} \quad (7.33)$$

is ideally zero so that Eq. (7.32) reduces to Eq. (7.2). Note that reducing the integrator's gain,  $C_I/C_F$ , reduces the gain error while increasing the gain required of the comparator. Note also that the denominator term is common in both the signal and the noise. This term results in a data converter gain error (it behaves as if it were an op-amp offset voltage that is a function of the integrator's output amplitude [which results in the gain error] and frequency), but it will not affect the modulator's SNR. In order to determine the

increase in the modulator's output noise (the change in the shape of the modulation noise) we need to look at the noise transfer function including the effects of the gain error

$$NTF_{\epsilon}(z) = (1 + \epsilon_{gain}) - z^{-1} \quad (7.34)$$

or, in the frequency domain,

$$|NTF(f)|^2 = 2(1 + \epsilon_{gain}) \left( 1 - \cos 2\pi \frac{f}{f_s} \right) + \epsilon_{gain}^2 \quad (7.35)$$

Following the same procedure used to arrive at Eq. (7.12) and assuming constant op-amp gain,  $A_{OL}(f)$ , from DC to  $B$ , results in

$$V_{Qe,RMS}^2 = 2 \cdot \frac{V_{LSB}^2}{12f_s} \cdot \left[ 4(1 + \epsilon_{gain}) \frac{\pi^2}{f_s^2} \cdot \frac{1}{3} \cdot \left( \frac{f_s}{2K} \right)^3 + \epsilon_{gain}^2 \cdot \frac{f_s}{2K} \right] \quad (7.36)$$

noting that if  $\epsilon_{gain} = 0$ , this equation reduces to Eq. (7.12).

If we assume the contribution to the noise from the error term squared,  $\epsilon_{gain}^2$ , is small, which is valid for op-amp gain

$$A_{OL}(f) > K \text{ (the oversampling ratio)} \quad (7.37)$$

over the frequency range of DC to  $B$ , then we can rewrite Eq. (7.13), to include the effects of finite op-amp gain, as

$$SNR_{ger} = 6.02N + 1.76 - 20 \log \frac{\pi}{\sqrt{3}} + 20 \log K^{3/2} - 10 \log (1 + \epsilon_{gain}) \quad (7.38)$$

The largest degradation in the  $SNR$ , resulting from integrator leakage, can be estimated as 0.5 dB if  $K \geq 8$  ( $\epsilon_{gain} \approx 1/8$  neglecting  $G_I$ ). The minimum gain·bandwidth product of the op-amp is estimated as

$$\text{Op-amp unity gain frequency, } f_{un} = K \cdot B = f_s/2 \quad (7.39)$$

assuming the op-amp is rolling off at 20 dB/decade at  $B$  (a dominant pole compensated op-amp). Otherwise, the minimum gain of the op-amp can be estimated simply as the oversampling ratio,  $K$ .

In order to illustrate typical op-amp requirements, let's consider the modulator of Fig. 7.14 with  $K = 16$  and  $B = 3.125$  MHz (see Ex. 7.1). The  $f_{un}$  of the op-amp is estimated, using Eq. (7.39), as 50 MHz. If the open-loop response of the op-amp starts to roll off at 10 kHz, then the DC gain of the op-amp must be at least 5,000. However, we could also use an op-amp with a DC gain of 100 (remembering low integrator gain increases the undesirable effects [noise and offset] of the comparator on the performance of the modulator) that rolls off at 500 kHz.

### 7.1.8 Op-Amp Settling Time

Equation (7.39) can be used, for the moment, to provide an estimate for the settling time requirements of the op-amp in a first-order modulator. *Assuming* the settling time is linear, and not slew-rate limited, we can write the change in the op-amp's output assuming a dominant pole compensated op-amp as

$$v_{out} = V_{outfinal}(1 - e^{-t/\tau}) \text{ where } \tau = \frac{1}{2\pi f_u \cdot \beta} \quad (7.40)$$



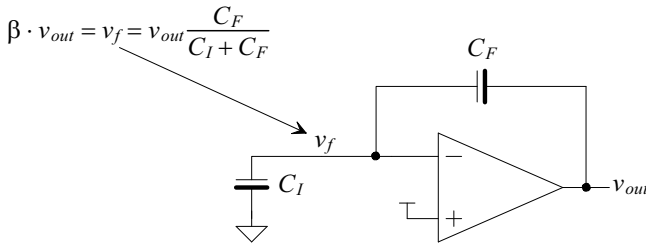
where, for the DAI (see Fig. 7.18), the feedback factor is

$$\beta = \frac{C_F}{C_F + C_I} \quad (7.41)$$

The feedback factor is 0.714 in the modulator of Fig. 7.14. The output of the DAI,  $v_{out}$ , must settle in a time,  $t$  ( $t < T_s/2$ ), to some percentage of an ideal value,  $V_{outfinal}$ . Solving for this percentage using Eqs. (7.39), (7.40), and (7.41) and assuming  $T_s/2 = t$  results in

$$\frac{v_{out}}{V_{outfinal}} \times 100\% = 1 - \exp\left[-\frac{\pi}{2} \cdot \frac{C_F}{C_F + C_I}\right] \times 100\% \quad (7.42)$$

The output will only reach 67% of its ideal final value in the modulator of Fig. 7.14 when the op-amp used has a unity gain frequency of  $f_s/2$ .



**Figure 7.18** The feedback factor in the DAI.

In deriving Eq. (7.42), we used an op-amp unity gain frequency specified by Eq. (7.39) to determine the settling response of the integrator. If the settling is linear then incomplete settling will result in a constant DAI gain error (0.67 above). Every time the output changes it will change by some constant percentage of its ideal value. Rewriting the transfer function of our DAI to include this constant gain error results in

$$V_{out}(z) = \frac{C_I}{C_F} \cdot \overbrace{(1 - e^{-\pi\beta \cdot (f_{un}/f_s)})}^{\text{Settling gain error, } G_s} \cdot \frac{V_1(z) \cdot z^{-1/2} - V_2(z)}{1 - z^{-1}} \quad (7.43)$$

Full, or complete, settling requires that the op-amp's unity gain frequency,  $f_{un}$ , be much larger than the sampling frequency,  $f_s$  (in other words we can't use Eq. [7.39] to specify the required bandwidth of the op-amp if settling time is important). The constant gain error, resulting from incomplete settling, can be tolerated in the first-order modulator because the integrator is directly followed by a comparator, as discussed earlier. In some of the modulator topologies, though, the integrator is not followed by a comparator so settling time becomes more important. In order to determine to what percentage the integrator output must settle in these topologies, a gain term, say  $G_s$ , is added to the linearized block diagram of the modulator (integrator). The transfer function of the modulator is then evaluated to determine the allowable values of  $G_s$  for the application.

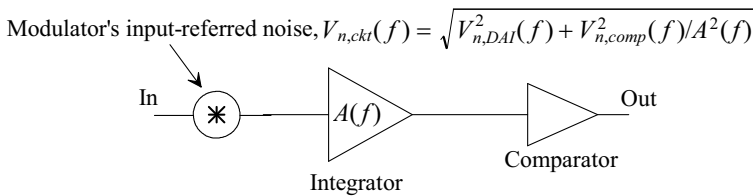
It's important to realize that we are assuming the op-amp doesn't experience slew-rate limitations. If slewing is present, then the added gain term, in Eq. (7.43), will not be a constant and will introduce *distortion* into the modulator's output spectrum (whether a comparator follows the integrator or not).

### 7.1.9 Op-Amp Offset

The operation of the DAI is subject to the op-amp's offset. It can be shown that this offset will effectively add (or subtract) from the common-mode voltage,  $V_{CM}$ , and thus effectively shift the input signals upwards or downwards. The resulting modulator output will then show an offset equal to the op-amp's offset. In order to circumvent this problem, offset storage can be used in the integrator.

### 7.1.10 Op-Amp Input-Referred Noise

Here we discuss how the DAI's unwanted noise contributions affect the SNR of the modulator, assuming we know the DAI's input-referred noise PSD  $V_{n,DAI}^2(f)$ . Figure 7.19 shows the modulator's input-referred noise source,  $V_{n,ckt}(f)$ , in series with the input signal. This noise source, with units of  $V/\sqrt{\text{Hz}}$ , includes both the integrator's and the comparator's contributions. However, as discussed earlier, the noise contributions from the comparator are usually negligible because of the high-gain of the integrator.



**Figure 7.19** The modulator's input-referred noise contributions from both the comparator and the integrator.

Because the modulator's input-referred noise adds directly to the input signal, we can use the derivations developed earlier in the chapter. As specified in Eq. (7.2), the modulator's input, and thus its input-referred noise, pass through the modulator with a delay of  $z^{-1}$ . If we assume the modulator's input-referred noise is white and bandlimited to  $f_s/2$  such that

$$V_{n,ckt}(f) = \frac{V_n}{\sqrt{f_s}} \text{ for } f < f_s/2 \quad (7.44)$$

then passing the output of the modulator through an ideal lowpass filter with a bandwidth of  $B (= f_s/[2K])$  results in

$$V_{ckt,RMS} = \sqrt{2 \cdot \int_0^B \frac{V_n^2}{f_s} \cdot df} = \frac{V_n}{\sqrt{K}} \quad (7.45)$$

Noting that not passing the output of the modulator through a lowpass filter results in an RMS output noise of  $V_n$ , we see that the averaging filter (the lowpass filter) reduces the noise by the root of  $K$ . We could also think of the filtering as reducing the PSD of the modulator's input-referred noise by  $K$ . Remembering the jitter discussion from Ch. 5, we see a direct parallel in the derivations of how averaging affects the RMS value of a random signal (noise or jitter).

Finally, as used in Ex. 5.13, we can estimate the finite SNR of a data converter from quantization noise, jitter, and circuit noise using

$$V_{n,RMS} = \sqrt{V_{Qe,RMS}^2 + V_{jitter,RMS}^2 + V_{ckt,RMS}^2} \tag{7.46}$$

and

$$SNR = 20 \cdot \log \frac{V_p/\sqrt{2}}{V_{n,RMS}} \tag{7.47}$$

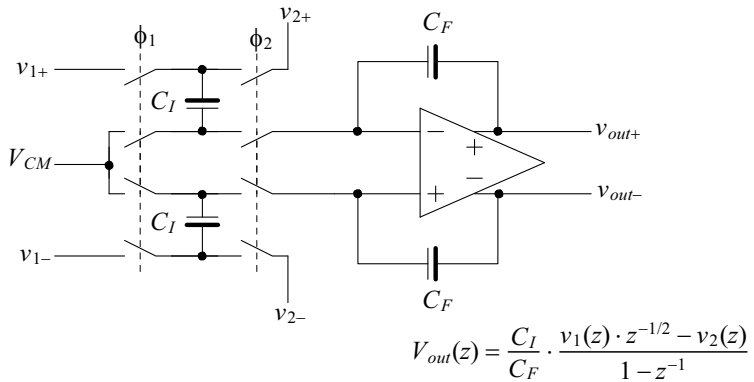
where  $V_p$  is, again, the peak amplitude of an input sinewave and

$$V_{jitter,RMS} = \sqrt{P_{AVG,jitter}} \text{ (see Eq. [5.51])} \tag{7.48}$$

### 7.1.11 Practical Implementation of the First-Order NS Modulator

Switched-capacitor circuits suffer from the problems of capacitive feedthrough and charge injection. To reduce these effects, fully-differential circuit topologies are used. It could be stated that if reasonable size capacitors and dynamic range are required, fully-differential topologies are a necessity simply because they subtract out, to a first-order, the voltage changes on the switched-capacitors resulting from these problems. In addition fully-differential topologies are used because they improve power supply and substrate-coupled noise rejection and improve distortion (even-order harmonics cancel).

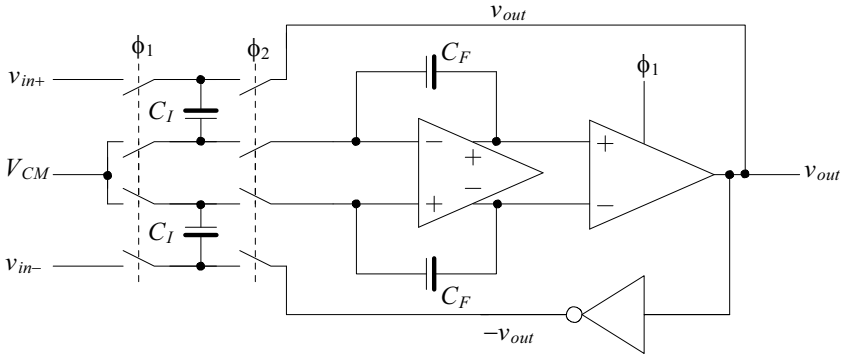
Figure 7.20 shows the fully-differential implementation of the DAI of Fig. 2.54. The inputs are now differential, that is, now  $v_1 = v_{1+} - v_{1-}$  and  $v_2 = v_{2+} - v_{2-}$ , as is the output of the integrator,  $v_{out} = v_{out+} - v_{out-}$ . The fully-differential DAI has the same transfer function as the single-ended DAI assuming the input signals are differential.



**Figure 7.20** Fully-differential discrete-analog integrator (DAI) implementation.

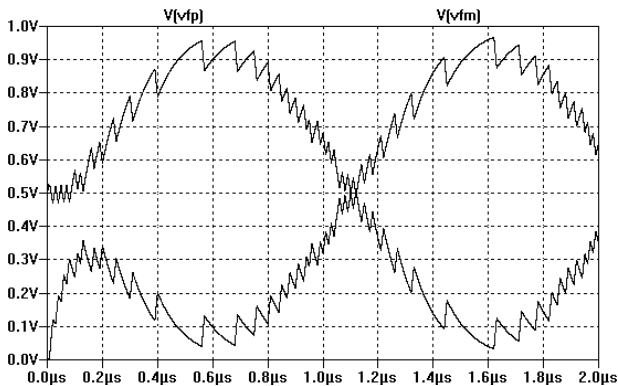
It's important to understand the signal levels in the fully-differential DAI. Let's assume  $V_{CM} = 0.5$  V and the input voltages can range in amplitude from 0 to 1 V. Assuming the input is balanced correctly if  $v_{1+} = 0.85$  V, then  $v_{1-}$  must equal 0.15 V. The maximum input voltage is  $v_{1max} = 1 - 0 = 1$  V. The minimum input signal, on the other hand, is  $v_{1min} = 0 - 1 = -1$  V. The range of inputs, or outputs, is then 2 V or twice the range of the single-ended DAI.

Figure 7.21 shows the implementation of a first-order NS modulation utilizing a fully-differential DAI. Let's simulate the operation of this modulator with the input signals and capacitor sizes used in Fig. 7.14 ( $f_s = 100$  MHz,  $C_I = 0.4$  pF, and  $C_F = 1$  pF,  $f_{in} = 500$  kHz, and a 0.5 V peak input sinewave [the input sinewave,  $v_{in+} - v_{in-}$ , has a peak amplitude of 1 V]).



**Figure 7.21** Fully-differential implementation of a first-order NS modulator.

Figure 7.22 shows the simulation results for the outputs of the modulator of Fig. 7.21 after being passed through two RC filters with time constants of 100 ns. Passing a single modulator output to the decimating filter would result in an output that is half the input signal amplitude, which can be compensated for at the output of the filter by a shift-left operation (multiply by two). Note that the input common-mode voltage of the op-amp remains at 0.5 V. This is important as the design of the op-amp becomes more challenging if the common-mode voltage is not constant. The finite op-amp common-mode rejection ratio (CMRR) can introduce distortion into the output of the modulator.



**Figure 7.22** Outputs of the fully-differential first-order modulator after RC filtering.

## 7.2 Second-Order Noise-Shaping

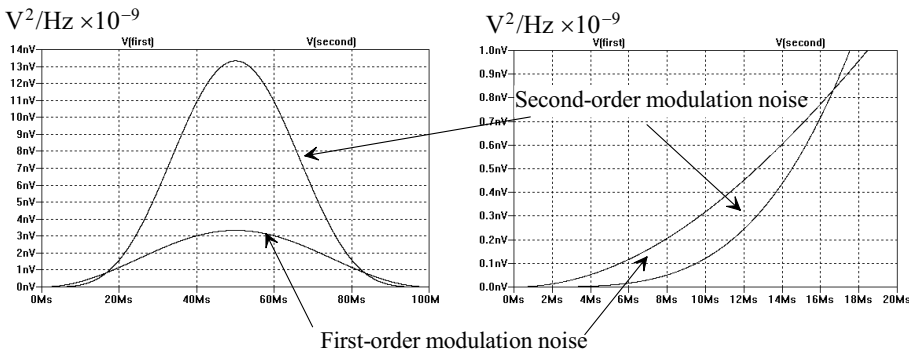
If we review Eq. (7.2), we might wonder if further filtering of the quantization noise,  $V_{Qe}(z)$ , can result in an improvement in the data converter's SNR over an input signal bandwidth  $B$ . The second-order modulator's output shows a double differentiation of the quantization noise

$$v_{out}(z) = z^{-1}v_{in}(z) + (1 - z^{-1})^2 V_{Qe}(z) \tag{7.49}$$

The modulation noise may then be written, see Eq. (7.8), as

$$|NTF(f)|^2 \cdot |V_{Qe}(f)|^2 = \frac{V_{LSB}^2}{12f_s} \cdot 16 \sin^4 \pi \frac{f}{f_s} \tag{7.50}$$

Figure 7.23 shows a comparison between the modulation noise of first- and second-order NS modulators. Notice that the modulation noise is "flatter" in the bandwidth of interest.



**Figure 7.23** Comparing first- and second-order NS modulator's modulation noise.

Following the procedure used earlier to calculate the RMS quantization noise in a bandwidth  $B$  results in

$$V_{Qe,RMS} \approx \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\pi^2}{\sqrt{5}} \cdot \frac{1}{K^{5/2}} \tag{7.51}$$

with an increase in the SNR of

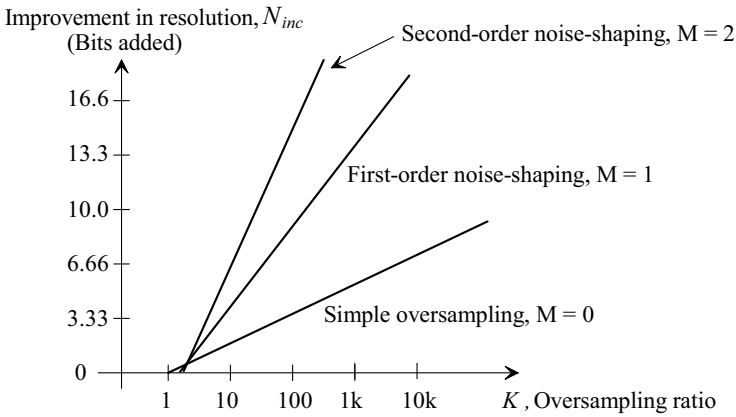
$$SNR_{ideal} = 6.02N + 1.76 - 12.9 + 50 \log K \tag{7.52}$$

*Every doubling in the oversampling ratio results in an increase in SNR of 15 dB or 2.5 bits increase in resolution!* Figure 7.24 shows a comparison between simple oversampling, first-order NS, and second-order NS-based data converters. Note that, as discussed earlier, the oversampling ratio is generally greater than or equal to eight.

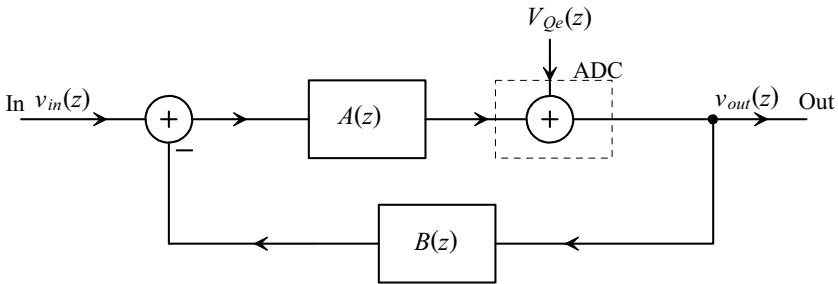
### 7.2.1 Second-Order Modulator Topology

Consider the block diagram of a NS modulator shown in Fig. 7.25 (see Fig. 5.39). The transfer function of this modulator may be written as

$$v_{out}(z) = \frac{A(z)}{1 + A(z)B(z)} \cdot v_{in}(z) + \frac{1}{1 + A(z)B(z)} \cdot V_{Qe}(z) \tag{7.53}$$



**Figure 7.24** Comparing improvement in modulator resolution.



**Figure 7.25** Block diagram of a feedback modulator.

Comparing this equation to Eq. (7.49), we can solve for the forward and fed-back circuit blocks,  $A(z)$  and  $B(z)$ , by equating coefficients

$$STF(z) = \frac{A(z)}{1 + A(z)B(z)} = z^{-1} \tag{7.54}$$

and

$$NTF(z) = \frac{1}{1 + A(z)B(z)} = (1 - z^{-1})^2 \tag{7.55}$$

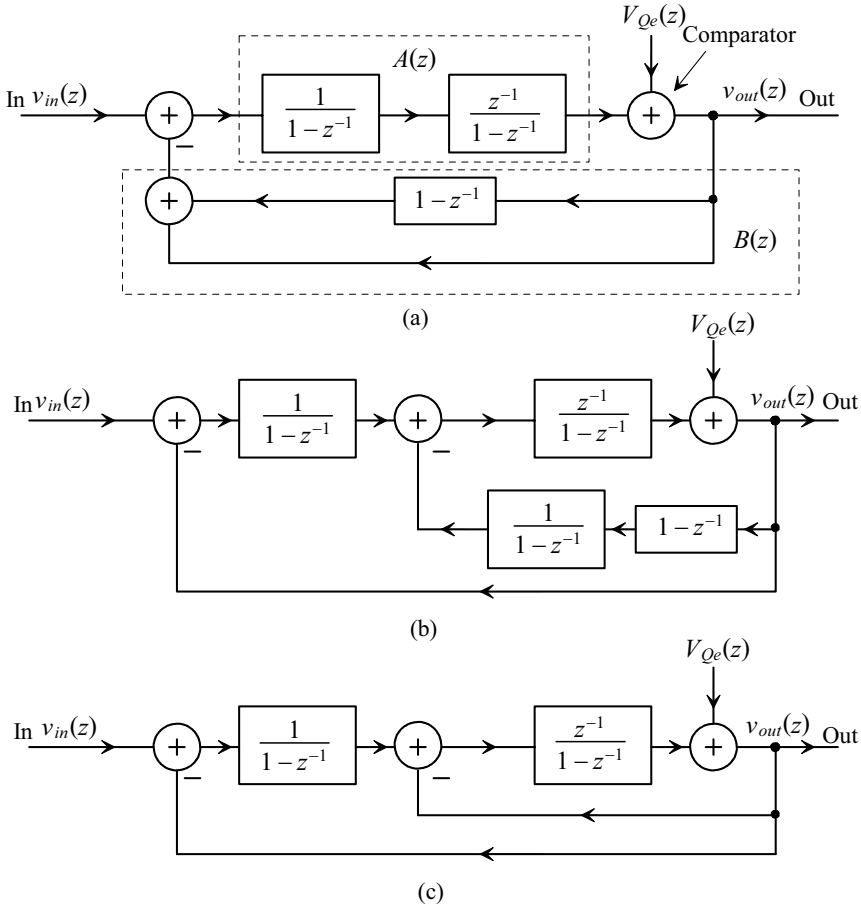
The results are

$$A(z) = \frac{z^{-1}}{(1 - z^{-1})^2} \tag{7.56}$$

and

$$B(z) = 2 - z^{-1} \tag{7.57}$$

The second-order modulator can be implemented using the topology shown in Fig. 7.26a. The output of  $B(z)$  is the sum of the modulator output and the differentiated,  $(1 - z^{-1})$ ,

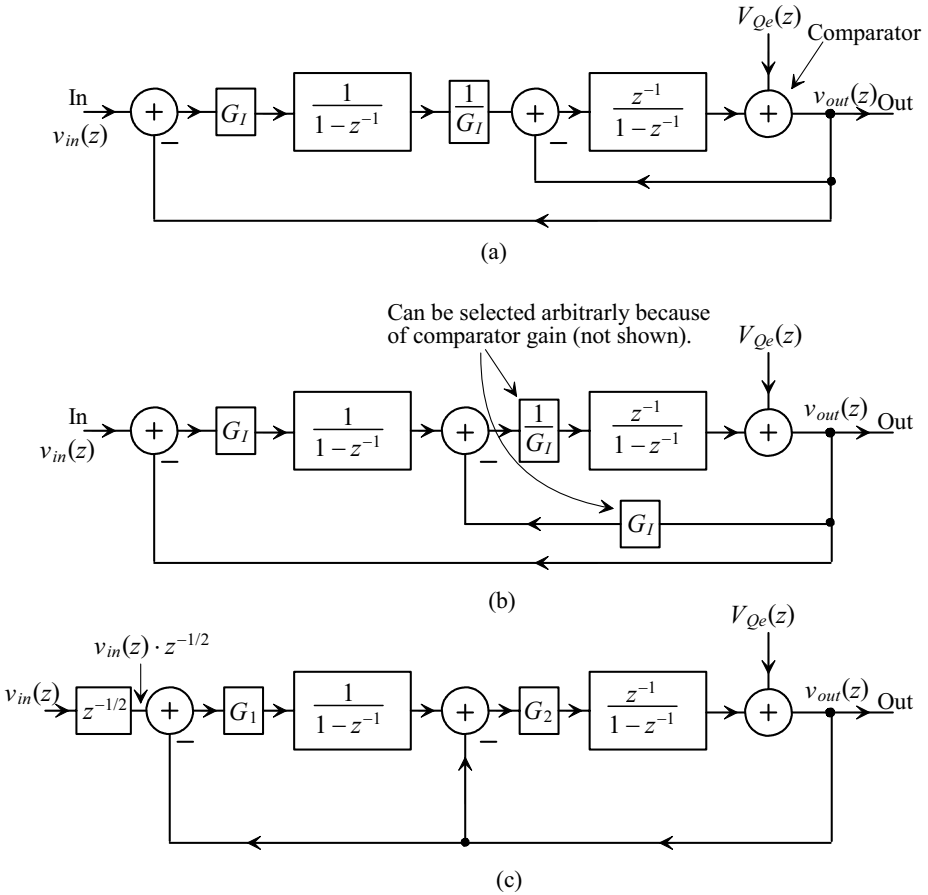


**Figure 7.26** Block diagrams of second-order modulators.

modulator output. We can redraw the block diagram in (a), as shown in Fig. 7.26b, resulting in the implementation of a second-order NS modulator shown in Fig. 7.26c.

The second-order (de) modulator topology of Fig. 7.26c can be used directly to implement a NS DAC (see Figs. 7.4 and 7.5). However, this topology doesn't lend itself directly to implementation using the DAI. The major concern, as discussed in the last section, is the op-amp's output going to the power-supply rails (integrator saturation). This is more of a concern in the second-order modulator since the output of the first integrator isn't connected directly to a comparator.

Figure 7.27a shows how we can add an integrator gain to the block diagram of Fig. 7.26c without changing the system's transfer function. Figure 7.27b shows pushing the gain,  $1/G_I$ , through the second summer so that it is directly preceding the second integrator. Notice that in Fig. 7.27b this (the second integrator's gain) is in series with the comparator's gain (not shown; see Fig. 7.15 and the associated discussion). This means we can arbitrarily change the second integrator's gain because the comparator gain



**Figure 7.27** Block diagrams of second-order modulator introducing integrator gains.

changes to force the loop gain to unity. Figure 7.27c shows the resulting configuration where the second integrator has the a gain of  $G_2$  and the first integrator has a gain of  $G_1$ . Also notice that we have added a delay in series with the input signal. This delay was added to show how using a DAI results in an added delay in series with the input signal (see Fig. 2.55 and the associated discussion). The delay doesn't affect the magnitude of modulator's transfer function but rather indicates the input signal arrives half a clock cycle later.

Figure 7.28 shows the DAI implementation of the second-order modulator of Fig. 7.27c. Note how the output of the modulator is fed back and immediately passes through the first integrator and is applied to the second integrator (no delay as seen in Fig. 7.27c). This is a result of switching the phases of the clock signals in the first integrator. We should also see how the input signal sees an added half-clock cycle delay. Note that at this point it should be straightforward to sketch the circuit implementation of the fully-differential, second-order modulator (see Fig. 7.21).



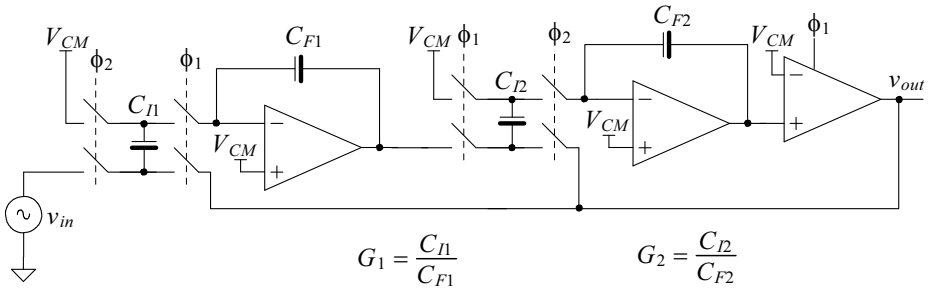


Figure 7.28 Implementation of the second-order modulator of Fig. 7.27c.

### 7.2.2 Integrator Gain

As we showed in Eq. (7.28) for the first-order modulator, the forward gain of a second-order modulator will also be unity when the modulator is functioning properly. We now need to discuss how to select the integrator gains to avoid harmful integrator saturation. If noise and offsets were not a concern, as shown in Fig. 7.17 and the associated discussions, then we could make our integrator gains very small (ultimately limited by imperfections in the switches such as clock feedthrough and charge injection). In a practical modulator, integrator saturation (the integrator's gain going to zero) can also lead to modulator instability, as shown in Eq. (7.27), and the associated discussion.

Figure 7.29 shows the integrator outputs for the modulator of Fig. 7.28 if both integrator gains are set to 0.4. Notice that both outputs go outside the supply voltage range. If we replace the ideal op-amps in the simulation with transistor-based op-amps, the integrator outputs will saturate at some voltage within the supply range. This saturation can be thought of as noise and ultimately limits the data converter's SNR. Integrator saturation can be avoided by limiting the input signal range, designing with small integrator gain, and using op-amps that have a wide output swing.

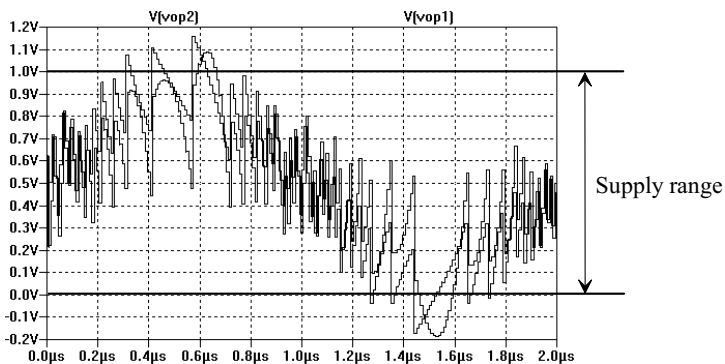


Figure 7.29 Showing integrator outputs in a second-order modulator with the integrator gains both set to 0.4.

For a more quantitative view of how the gains in a second-order NS modulator affect performance, let's consider a couple of different topologies. Figure 7.30 shows the block diagram of the second-order NS modulator topology of Fig. 7.25, with an integrator gain coefficient,  $G_I$ , and a comparator gain,  $G_c$ , added. Deriving the transfer function of this linearized model with  $G_F = G_I \cdot G_c$  results in

$$v_{out}(z) = \frac{G_F \cdot z^{-1} \cdot v_{in}(z)}{1 + z^{-1} \cdot 2(G_F - 1) + z^{-2} \cdot (1 - G_F)} + \frac{(1 - z^{-1})^2 \cdot V_{Qe}(z)}{1 + z^{-1} \cdot 2(G_F - 1) + z^{-2} \cdot (1 - G_F)} \quad (7.58)$$

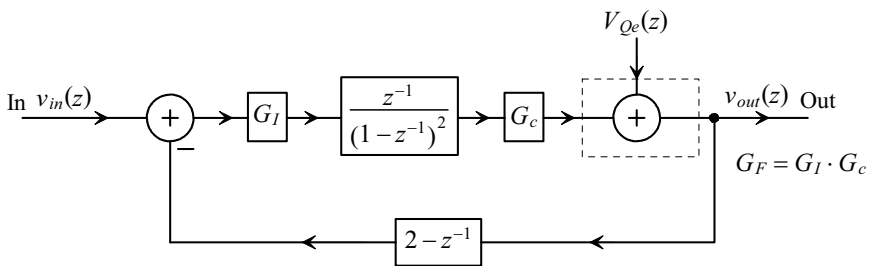
The poles of this transfer function are located at

$$z_{p1,p2} = (1 - G_F) \pm \sqrt{(1 - G_F)^2 - (1 - G_F)} \quad (7.59)$$

We know that for the modulator to remain stable the poles must reside within the unit circle. This means that our values of forward gain are restricted to

$$0 \leq G_F \leq 1.333 \quad (7.60)$$

Again, if the modulator is functioning properly,  $G_F = 1$  (because of the comparator's gain variation as seen in Fig. 7.15 and the associated discussion).

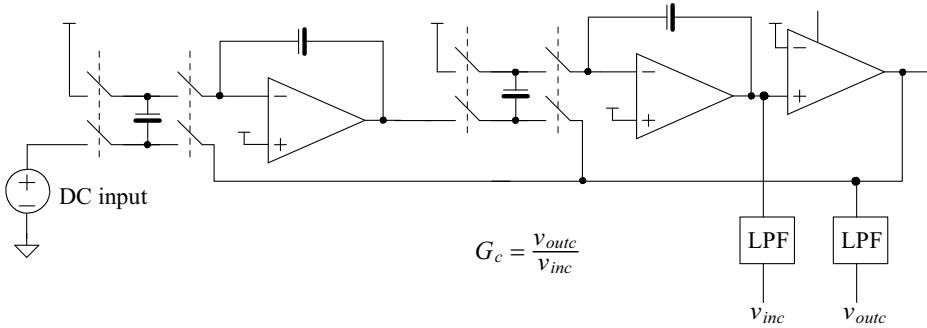


**Figure 7.30** Block diagram of a second-order feedback modulator with gains.

We should make some observations at this point. Reviewing Eq. (7.27), we see that the allowable range of forward gain, in the first-order modulator, is larger than the allowable range in the second-order modulator. However, as long as the integrators don't saturate ( $G_I$  doesn't approach zero), stability for either modulator is easy to attain. An analysis of the stability of higher-order modulators show that the range of allowable forward gains decreases with the order of the modulator. For example, a third-order modulator can have a forward gain of at most 1.15. Finally, notice that the input signal range is more restricted for the second-order modulator, in order to avoid integrator saturation, as seen in Fig. 7.29. We'll discuss methods to attain wider input signal range and more robust stability criteria by adjusting the feedback gains later.

Notice that we are treating our modulator as a linear system even though it isn't linear; the comparator gain is a nonlinear variable. The linear approximation is useful in order to give an idea of the stability of the modulator under certain operating conditions. Generally, a DC input is applied to the modulator in the simulation, while lowpass filters

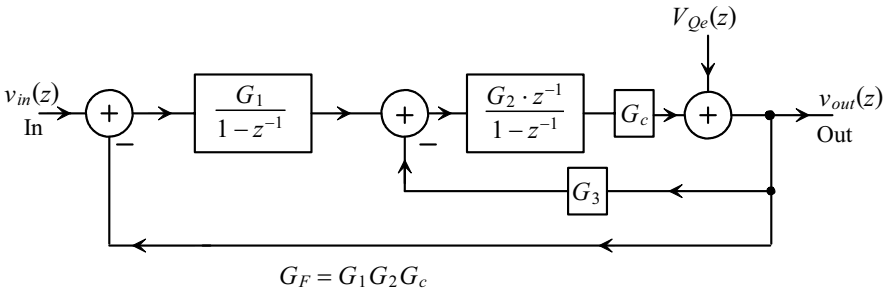
are added to determine the average comparator gain,  $G_c$ . Figure 7.31 shows this schematically. Assuming we know  $G_I$  (the gain coefficient of the integrators), we can then look at the stability and forward gain of the modulator for varying DC input signal voltages.



**Figure 7.31** Simulating the gain of the comparator.

Next, consider the more generic block diagram of the second-order NS modulator shown in Fig. 7.32. In a moment we'll discuss how to implement the feedback gain,  $G_3$ , using the DAI. The transfer function of this topology can be written as

$$v_{out}(z) = \frac{G_1 G_2 G_c \cdot z^{-1} v_{in}(z) + (1 - z^{-1})^2 \cdot V_{Qe}(z)}{1 + z^{-1} \cdot (G_1 G_2 G_c + G_2 G_3 G_c - 2) + z^{-2} \cdot (1 - G_2 G_3 G_c)} \quad (7.61)$$



**Figure 7.32** Generic block diagram of a second-order NS modulator.

Notice that if  $G_1 = G_2 = G_3 = G_c = 1$  (where  $G_1 G_2 G_c = G_F$ ), then this equation reduces to Eq. (7.49). The poles of this equation are located at

$$z_{p1,p2} = \frac{2 - G_1 G_2 G_c - G_2 G_3 G_c \pm \sqrt{(2 - G_1 G_2 G_c - G_2 G_3 G_c)^2 - 4(1 - G_2 G_3 G_c)}}{2} \quad (7.62)$$

When the modulator is functioning properly we require the (linearized) coefficient of the input,  $v_{in}(z)$  in Eq. (7.61), to be unity

$$\left| \frac{G_1 G_2 G_c}{(z - z_{p1})(z - z_{p2})} \right| = 1 \quad (7.63)$$

Again, if we set  $G_1 = G_2 = G_3 = 1$  (and  $G_c = 1$ ), then the poles are located at DC, that is,

$$z_{p1,p2} = 0 \tag{7.64}$$

Equation (7.62) is useful to estimate the modulator's stability when scaling amplitudes by adjusting the integrator gain coefficients,  $G_1$ ,  $G_2$ , and  $G_3$ .

*Implementing Feedback Gains in the DAI*

Consider the modified DAI shown in Fig. 7.33. Notice that if  $C_{I2} = C_{I3}$ , this topology reduces to the DAI shown in Fig. 2.54. Also note that some of the switches can be combined to simplify the circuitry. Assuming that the output is connected through the  $\phi_2$  switches (or that there are no switches connected to the output of the op-amp, see Eq. [2.102]) we can write the transfer function of the integrator as

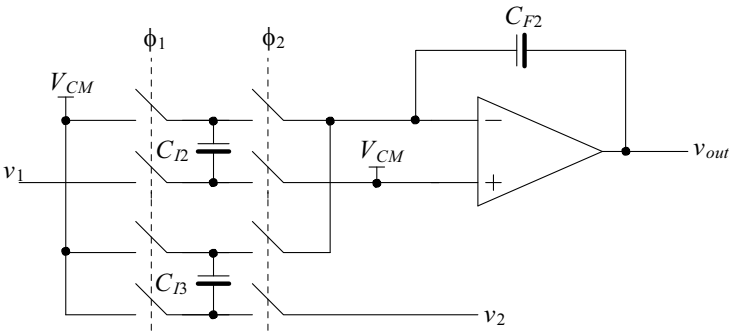
$$v_{out}(z) = v_1(z) \cdot \frac{C_{I2}}{C_{F2}} \cdot \frac{z^{-1/2}}{1 - z^{-1}} - v_2(z) \cdot \frac{C_{I3}}{C_{F2}} \cdot \frac{1}{1 - z^{-1}} \tag{7.65}$$

The block diagram of this topology is shown in Fig. 7.34a. We want to implement a block diagram like the one shown in Fig. 7.34b. Because we have already defined

$$G_2 = \frac{C_{I2}}{C_{F2}} \tag{7.66}$$

we define our feedback gain,  $G_3$ , as

$$G_3 = \frac{C_{I3}}{C_{F2}} \cdot \frac{1}{G_2} = \frac{C_{I3}}{C_{I2}} \tag{7.67}$$

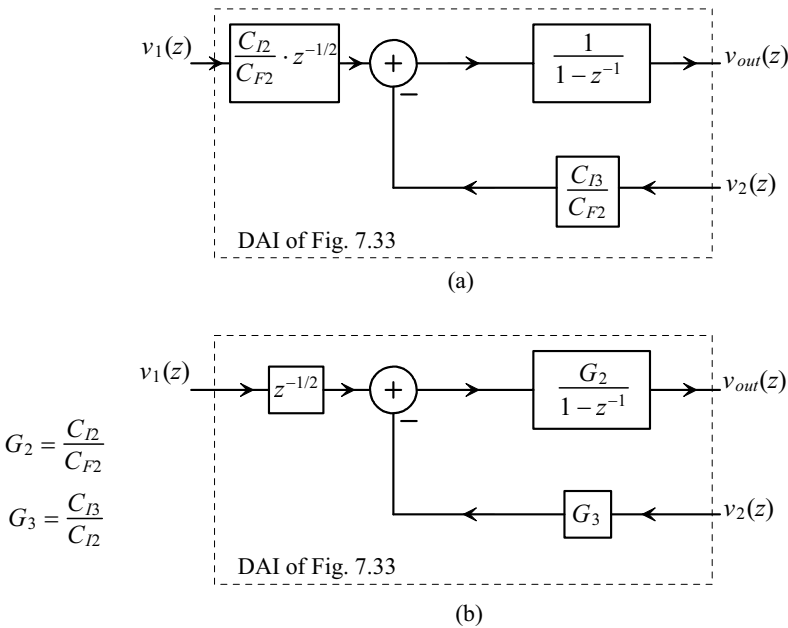


**Figure 7.33** Adding an additional gain setting to our DAI.

**Example 7.4**

Sketch the circuit implementation of a second-order NS modulator based on the topology of Fig. 7.32, where  $G_1 = G_2 = G_3 = 0.4$ . Comment on the stability of the resulting configuration. Simulate the design and show the integrator output swing.

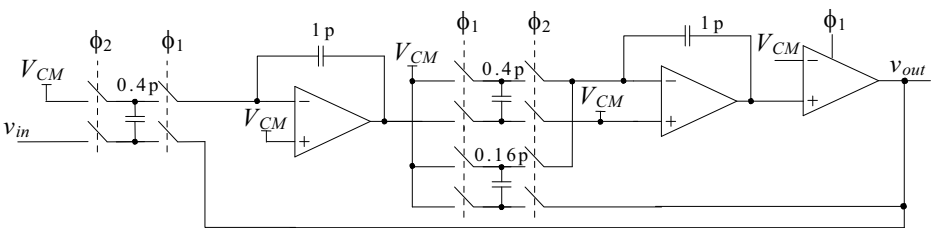
The implementation of the modulator is shown in Fig. 7.35. We could dissect Eq. (7.62) at this point to determine the transient properties of the modulator. However, before discussing the transient characteristics of the modulator, let's look at the integrator output swing.



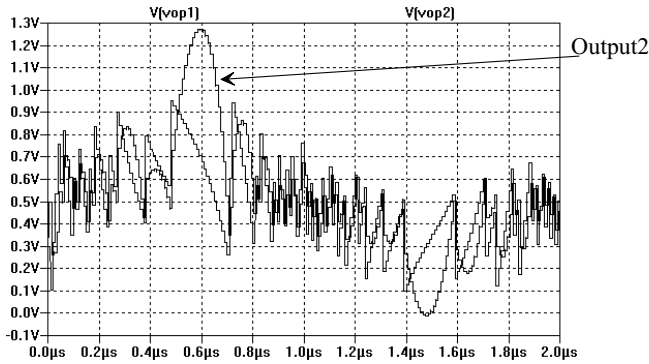
**Figure 7.34** Block diagram of a DAI.

Figure 7.36 shows the output swing of the integrators. This figure should be compared with Fig. 7.29. The output of the first integrator now falls within the power supply range. The output of the second integrator is reduced but still exceeds the power supply range. This, as discussed earlier, has less impact on performance in the actual transistor-based modulator because the integrator is followed by a comparator.

Let's attempt to get an idea for the stability of the modulator by adding LPFs, as seen in Fig. 7.31, to the simulation (with a DC input) to measure  $G_c$ . Figure 7.37 shows how we will implement the LPFs. The voltage-controlled voltage source is used to keep from loading the modulator with the RC circuit when it is added into the general simulation. In our ideal modulator shown in Fig. 7.35 both the comparator output and integrator outputs are ideal voltage sources, so we don't



**Figure 7.35** Implementation of a second-order modulator with feedback gain.

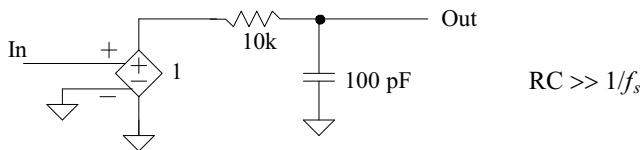


**Figure 7.36** Integrator output signals in the modulator shown in Fig. 7.35.

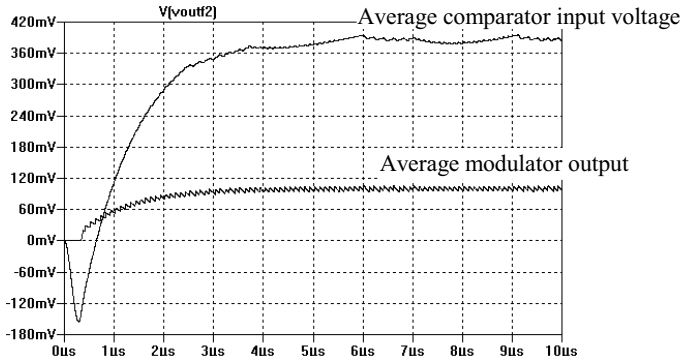
need the isolation (and therefore we can add the RC LPF directly into the simulation).

Figure 7.38 shows the comparator input and output, after lowpass filtering, for the modulator of Fig. 7.35 when the input signal is 0.1 V (DC). The average comparator input voltage is roughly 0.4 V. The resulting comparator gain is then only 0.25. Using Eq. (7.62) to calculate the location of the poles results in  $z_{p1,p2} = 0.96 \pm j \cdot 0.195$ . These poles are very close to the unit circle. Small shifts in the DAI gains can result in an unstable modulator. Increasing the input signal amplitude makes the modulator more stable. Increasing  $G_3$  also increases the modulator's stability.

The simulation that generated Fig. 7.38 can be very useful in understanding basic second-order modulator's stability criteria. Changing the simulation variables and looking at the resulting simulation outputs can be very instructional. Note that increasing the simulation time in the netlist that generated Fig. 7.38 would reveal that the comparator input actually has small amplitude oscillations. Also note that Fig. 7.36 shows the output of the second integrator going outside the power supply rails with variations in the input signal. This is related to the stability of the modulator being a function of the input voltage. An input signal close to  $V_{DD}$ , for example, causes the modulator to be less stable than an input signal close to  $V_{CM}$  ■



**Figure 7.37** SPICE implementation of a LPF for determining comparator gain.



**Figure 7.38** Average comparator input and output when using the modulator of Fig. 7.35 with an input signal of 0.1 V.

*Using Two Delaying Integrators to Implement the Second-Order Modulator*

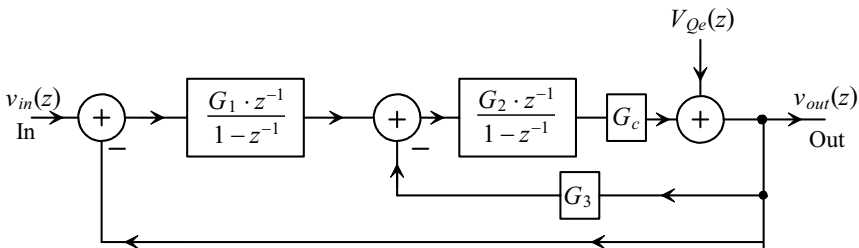
Consider the second-order modulator topology shown in Fig. 7.39. This topology can be implemented using the circuits in either Fig. 7.28 or Fig. 7.35 by simply switching the phases of the clocks in the first integrator (by making both integrators delaying). Without too much thought we know that adding gratuitous delay to the forward or feedback paths of a feedback system moves the system towards instability, however let's show this mathematically. The transfer function of this topology is

$$v_{out}(z) = \frac{G_1 G_2 G_c \cdot z^{-2} v_{in}(z) + (1 - z^{-1})^2 \cdot V_{Qe}(z)}{1 + z^{-1} \cdot (G_2 G_3 G_c - 2) + z^{-2} \cdot (1 - G_2 G_3 G_c + G_1 G_2 G_c)} \quad (7.68)$$

The poles are located at

$$z_{p1,p2} = \frac{2 - G_2 G_3 G_c \pm \sqrt{(2 - G_2 G_3 G_c)^2 - 4(1 - G_2 G_3 G_c + G_1 G_2 G_c)}}{2} \quad (7.69)$$

This equation should be compared to Eq. (7.62). Remembering that for a stable modulator the poles must be inside the unit circle, we see that using two delaying integrators will not result in a modulator that has as robust stability criteria as the general implementation of Fig. 7.27. The extra delay won't cause instability in modulators with large oversampling ratios (since the delay is then relatively small); however, for high-speed topologies or bandpass modulators excess forward (or feedback) delay can be a problem. Note that the benefit of this topology, and why it's used in many applications, is that it gives the comparator an extra half-clock cycle to make a decision.



**Figure 7.39** Second-order NS modulator using two delaying integrators.

### 7.2.3 Selecting Modulator (Integrator) Gains

Before leaving this section, let's discuss the general selection of modulator gains. In general, for good stability, the inner loop feedback gain,  $G_3$ , should be made as large as possible. For general design, set  $G_3 = 1$ . This simplifies the design of the modulator circuitry and provides good flexibility when selecting the values of  $G_1$  and  $G_2$ . If  $G_3 = 1$ , then Eq. (7.62) may be rewritten to show the location of the poles as

$$z_{p1,p2} = \frac{2 - G_1 G_2 G_c - G_2 G_c \pm \sqrt{(2 - G_1 G_2 G_c - G_2 G_c)^2 - 4(1 - G_2 G_c)}}{2} \quad (7.70)$$

Keeping in mind that the reason we are not setting all gains to one is to avoid integrator saturation, we can look at Eq. (7.70) as a guide to determine how we can reduce  $G_1$  and  $G_2$ . Since  $G_2$  is directly followed by the comparator, we can set its gain to 0.4 as discussed earlier. Practically then, we can reduce the value of  $G_1$  to a very small number and still have a stable modulator. At the same time, using a small  $G_1$  avoids integrator saturation. The practical problem with a small  $G_1$ , as discussed earlier, is the increase in the input-referred noise. Again trade-offs must be made for given design criteria. Figure 7.40 shows the integrator outputs for the modulator of Fig. 7.32 when  $G_1 = 0.2$ ,  $G_2 = 0.4$ , and  $G_3 = 1$ . Note that, when compared to Figs. 7.29 and 7.36, the outputs are very well behaved. We don't have the abnormal transitions above the power-supply rails indicating that the modulator stability is becoming marginal with input signal values close to the power-supply rails.

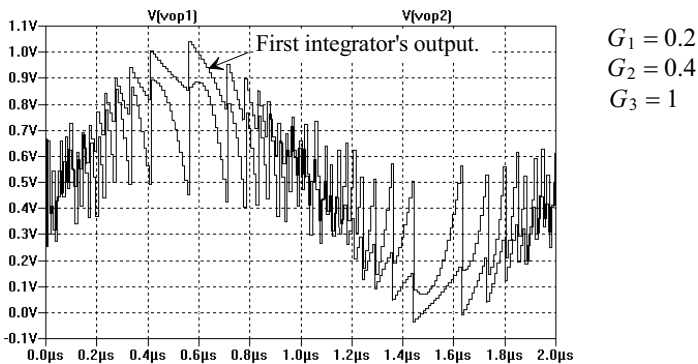


Figure 7.40 Integrator outputs for a modulator with first integrator gain of 0.2.

## 7.3 Noise-Shaping Topologies

The last section presented the fundamentals of NS data converters. It's important to understand this fundamental material before proceeding with the topics presented in this section.

In this section we cover (1) higher-order NS modulators, (2) NS modulators using multibit ADCs and DACs (multibit modulators), and (3) cascaded modulators (higher-order modulators built with a cascade of first- and/or second-order modulators).



### 7.3.1 Higher-Order Modulators

We can take the theory developed for our first- and second-order modulators in the last section and generalize it for an  $M^{\text{th}}$ -order modulator (a modulator having  $M$  integrators and  $M$  feedback loops). Rewriting Eqs. (7.8) and (7.50) for the general  $M^{\text{th}}$ -order modulator results in

$$|NTF(f)| \cdot |V_{Qe}(f)| = \frac{V_{LSB}}{\sqrt{12}f_s} \cdot \left[ 2 \sin \pi \frac{f}{f_s} \right]^M \quad (7.71)$$

The RMS noise in a bandwidth,  $B$ , can be written, see Eqs. (7.12) and (7.51), as

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\pi^M}{\sqrt{2M+1}} \cdot \frac{1}{K^{M+1/2}} \quad (7.72)$$

The ideal increase in the SNR can be written as

$$\text{SNR}_{ideal} = 6.02N + 1.76 - 20 \log \left[ \frac{\pi^M}{\sqrt{2M+1}} \right] + [20M + 10] \cdot \log K \quad (7.73)$$

or

$$\text{SNR}_{ideal} = 6.02(N + N_{inc}) + 1.76 \quad (7.74)$$

The increase in resolution,  $N_{inc}$ , is given by

$$N_{inc} = \frac{1}{6.02} \left[ (20M + 10) \cdot \log K - 20 \log \left( \frac{\pi^M}{\sqrt{2M+1}} \right) \right] \quad (7.75)$$

This equation shows that for every doubling in the oversampling ratio,  $K$ , the resolution increases by  $M + 0.5$  bits.

#### *$M^{\text{th}}$ -Order Modulator Topology*

Reviewing the general NS modulator topology of Fig. 7.25, we want to determine the forward transfer function,  $A(z)$ , and the feedback transfer function,  $B(z)$ , for an  $M^{\text{th}}$ -order NS modulator. The transfer function of a general  $M^{\text{th}}$ -order modulator is

$$v_{out}(z) = v_{in}(z) \cdot (z^{-1}) + V_{Qe}(z) \cdot (1 - z^{-1})^M \quad (7.76)$$

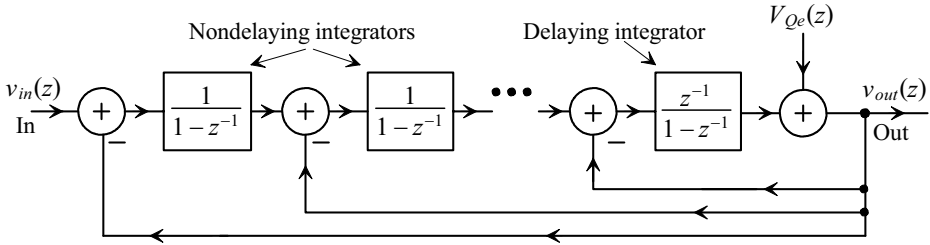
Using this equation together with Eq. (7.53) results in a forward modulator transfer function of

$$A(z) = \frac{z^{-1}}{(1 - z^{-1})^M} \quad (7.77)$$

and a feedback filter transfer function of

$$B(z) = \frac{1 - (1 - z^{-1})^M}{z^{-1}} \quad (7.78)$$

The block diagram of an  $M^{\text{th}}$ -order NS modulator is shown in Fig. 7.41. Note, as we'll see shortly, it's impossible (in an analog-to-digital converter) to implement this topology using only one delaying integrator.



**Figure 7.41** Generic block diagram of an  $M^{\text{th}}$ -order NS modulator.

### 7.3.2 Filtering the Output of an $M^{\text{th}}$ -Order NS Modulator

Let's revisit the derivation of Eq. (7.17). This equation states that the number of Sinc stages,  $L$ , used in cascade, for near optimum removal of the modulation noise, is one more than the order of the modulator ( $L = M + 1$ ). Rewriting Eq. (7.19)

$$V_{Qe,RMS}^2 = 2 \int_0^{f_s/2} |NTF(f)|^2 \cdot |V_{Qe}(f)|^2 \cdot |H(f)|^2 \cdot df \quad (7.79)$$

where the decimation filter's transfer function is given by

$$|H(f)|^2 = \left[ \frac{1}{K} \cdot \frac{\sin\left(K\pi\frac{f}{f_s}\right)}{\sin\left(\pi\frac{f}{f_s}\right)} \right]^{2(M+1)} \quad (7.80)$$

The mean-squared quantization noise is calculated by evaluating

$$V_{Qe,RMS}^2 = 2 \cdot \frac{V_{LSB}^2}{12f_s} \cdot \int_0^{f_s/2} \underbrace{\left[ \frac{|NTF(f)|^2}{2 \sin^2\left(\pi\frac{f}{f_s}\right)} \right]^{2M}}_{\text{}} \cdot \left[ \frac{1}{K} \cdot \frac{\sin\left(K\pi\frac{f}{f_s}\right)}{\sin\left(\pi\frac{f}{f_s}\right)} \right]^{2(M+1)} \cdot df \quad (7.81)$$

or

$$V_{Qe,RMS}^2 = 2 \cdot \frac{V_{LSB}^2}{12f_s} \cdot 2^{2M} \cdot \left[ \frac{1}{K} \right]^{2(M+1)} \cdot \int_0^{f_s/2} \frac{\sin^{2(M+1)}\left(K\pi\frac{f}{f_s}\right)}{\sin^2\left(\pi\frac{f}{f_s}\right)} \cdot df \quad (7.82)$$

If we let  $\theta = \pi\frac{f}{f_s}$ , then we get

$$V_{Qe,RMS}^2 = \frac{V_{LSB}^2}{12f_s} \cdot \left[ \frac{2}{K} \right]^{2(M+1)} \cdot \frac{f_s}{\pi} \cdot \underbrace{\int_0^{\frac{\pi}{2}} \frac{\sin^{2(M+1)}(K\theta)}{\sin^2\theta} \cdot d\theta}_{= \frac{K}{2}\pi \prod_{m=1}^M \frac{2m-1}{2m}} \quad (7.83)$$

Finally, the RMS quantization noise associated with an  $M^{\text{th}}$ -order modulator followed by an  $M + 1$  ( $= L$ ) Sinc averaging filter is

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}} \cdot \left[ \frac{2}{K} \right]^{M+1/2} \cdot \prod_{m=1}^M \frac{2m-1}{2m} \quad (7.84)$$

The change in  $SNR$ , when using the Sinc averaging filter decimator instead of the ideal filter with bandwidth,  $B$ , is given by looking at the ratio of Eq. (7.72) to Eq. (7.84)

$$\text{Increase in } SNR = -20 \log \left[ 2^{M+1/2} \cdot \prod_{m=1}^M \frac{2m-1}{2m} \cdot \frac{\sqrt{2M+1}}{\pi^M} \right] \quad (7.85)$$

For first-, second-, and third-order modulators, the improvement in the  $SNRs$  is 2.16, 6.35, and 10.39 dB, respectively. This shows that using a Sinc averager, theoretically, increases the  $SNR$  if we neglect the decrease in the desired signal amplitude because of the droop in the Sinc-filters response, Fig. 4.17. To avoid the droop, as discussed earlier, the desired signal content is often limited to frequencies well below  $f_s/2K (= B)$ . When the droop (reduction in the desired signal amplitude) is taken under consideration, the  $SNR$ , when using the Sinc averaging filter, is worse than the ideal filter with bandwidth  $B$ .

### 7.3.3 Implementing Higher-Order, Single-Stage Modulators

The single-stage, higher-order modulator of Fig. 7.41 can be difficult to implement directly. It is impossible to implement a higher-order modulator, when using DAIs, where all but the last integrator are nondelaying. However, as we saw with the second-order modulator using two delaying integrators in Fig. 7.39 and Eqs. (7.68) and (7.69), the stability criteria of a modulator using only delaying integrators is poorer than the criteria of the topology shown in Fig. 7.41 (where only the last integrator is delaying). While we can help the situation by staggering delaying and nondelaying integrators in a modulator, the point is that implementing a higher-order modulator without modifying our basic NS topology will result in an unstable circuit. Intuitively, we can understand this by noting that if the modulator's forward gain is too high and the delay through the forward path is too long (because of the large number of integrators), the signal fed back may add to the input signal instead of subtracting from it.

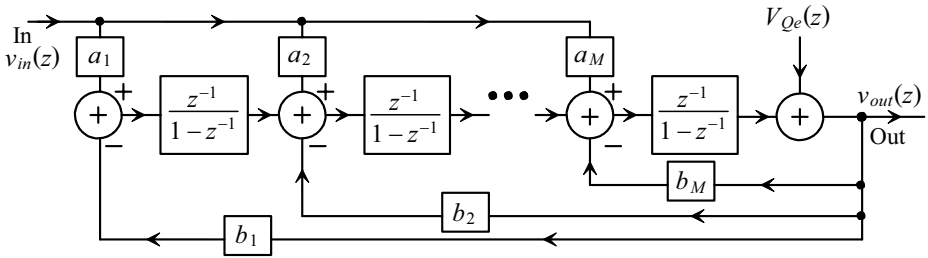
In order to help with the stability of a higher-order modulator a topology that feeds the input signal forward into additional points in the modulator (thereby reducing the forward gain and delay) and feeds the output signal back as discussed earlier (allowing scaling of amplitudes) is needed. In order to move towards this goal, consider the modified NS topology for higher-order modulators shown in Fig. 7.42. The forward and feedback transfer functions can be written as

$$A(z) = \frac{a_1 \cdot z^{-M}}{(1-z^{-1})^M} + \frac{a_2 \cdot z^{-(M-1)}}{(1-z^{-1})^{M-1}} + \frac{a_3 \cdot z^{-(M-2)}}{(1-z^{-1})^{M-2}} + \dots + \frac{a_M \cdot z^{-1}}{1-z^{-1}} = \sum_{i=1}^M a_i \cdot \left( \frac{z^{-1}}{1-z^{-1}} \right)^{M-i+1} \quad (7.86)$$

$$A(z) = (z-1)^{-M} \cdot \left[ a_1 + a_2(z-1)^1 + a_3(z-1)^2 + \dots + a_M(z-1)^{M-1} \right] \quad (7.87)$$

and

$$-A(z)B(z) = \frac{b_1 \cdot z^{-M}}{(1-z^{-1})^M} + \frac{b_2 \cdot z^{-(M-1)}}{(1-z^{-1})^{M-1}} + \frac{b_3 \cdot z^{-(M-2)}}{(1-z^{-1})^{M-2}} + \dots + \frac{b_M \cdot z^{-1}}{1-z^{-1}} = \sum_{i=1}^M b_i \cdot \left[ \frac{1}{z-1} \right]^{M-i+1} \quad (7.88)$$



**Figure 7.42** Block diagram of a modified  $M^{\text{th}}$ -order NS modulator.

or

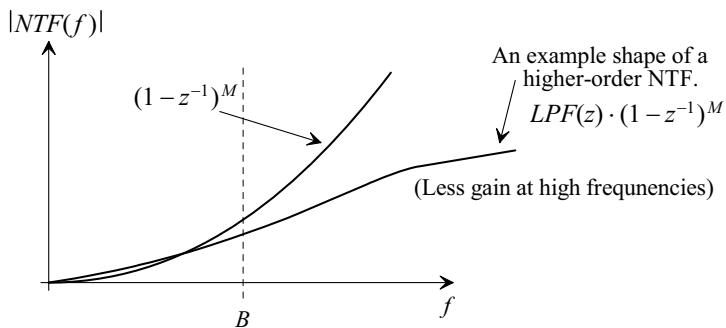
$$-A(z)B(z) = (z - 1)^{-M} \cdot [b_1 + b_2(z - 1) + b_3(z - 1)^2 + \dots + b_M(z - 1)^{M-1}] \tag{7.89}$$

Before going any further, let's explain what we are trying to do with the modified, higher-order, NS topology of Fig. 7.42. We know that the  $NTF(z)$ , for a general modulator, is of the form  $(1 - z^{-1})^M$  with a shape seen in Fig. 7.43. At high frequencies the modulation noise will get very large. At  $f_s/4$ , for example, the magnitude of the noise transfer function,  $|NTF(f)|$ , is  $(\sqrt{2})^M$  (see Fig. 1.20). For the modified NS modulator we will try to reduce the modulation noise at higher frequencies by changing the shape of the  $NTF(z)$ . Our modified  $NTF(z)$  will be of the form

$$NTF(z) = LPF(z) \cdot (1 - z^{-1})^M = LPF(z) \cdot \left(\frac{z-1}{z}\right)^M = HPF(z) \tag{7.90}$$

where  $LPF(z)$  [ $HPF(z)$ ] is a lowpass [highpass] filter implemented with the feedback coefficients  $b_x$ . The goal is to flatten out the higher frequency modulation noise (keep the noise from getting too large) thereby reducing the  $NTF(f)$  at high frequencies and keeping the modulator stable. One drawback of using this technique is that the signal no longer sees just a delay in its transfer function but rather it sees the lowpass response. The modified  $STF$  will be of the form

$$STF(z) = NTF(z) \cdot A(z) = LPF(z) \cdot \sum_{i=1}^M a_i \cdot (z - 1)^{i-1} \tag{7.91}$$



**Figure 7.43** Showing the change in the NTF in a higher-order modulator.

so that the feed forward coefficients,  $a_x$ , can be used to help make the  $STF(f)$  constant over the region of interest (the  $STF$  can be made to have an overall lowpass response). The  $NTF$  is given by

$$NTF(z) = \frac{1}{1 + A(z)B(z)} \quad (7.92)$$

or

$$NTF(z) = \frac{1}{1 - (z-1)^{-M} \cdot \sum_{i=1}^M b_i \cdot (z-1)^{i-1}} = HPF(z) \quad (7.93)$$

The coefficients,  $b_x$ , are selected for a highpass response. Note also that our coefficients are positive since the feedback paths, as seen in Fig. 7.42, are subtracting. The design of the modulator is performed by determining the feed-forward and feedback coefficients using basic digital-signal processing filter design (and, to keep the algebra simple, a computer program of some sort), then to simulate the design to see if it exceeds specifications. One challenge, among others, is to meet a given  $SNR$  without causing harmful integrator saturation.

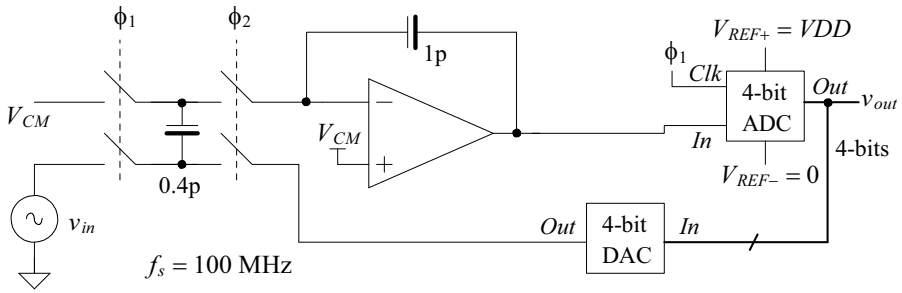
### 7.3.4 Multi-Bit Modulators

Throughout this chapter we have assumed  $N = 1$ ; that is, we have used a comparator for our quantizer in the forward path of our NS modulator. The main advantage of single-bit modulators, as discussed earlier, is the inherent linearity of the 1-bit feedback DAC. Feedback DAC linearity is important because the output of the DAC is directly subtracted from the input signal. Any distortion or nonlinearity (or noise) in the output of the DAC will directly affect the modulator's performance and, ultimately, limit the modulator's  $SNR$ . The benefits of using a multibit ( $N > 1$ ) quantizer in a NS modulator are increased  $SNR$  (see Eq. 7.73), better stability (the modulator behaves closer to the linearized theory developed in this chapter), fewer spectral tones, and simpler digital-decimation filter. The drawbacks of using multibit topologies, are the increase in ADC complexity (the ADC must be a flash converter) and the need for the DAC to be accurate to the final accuracy of the modulator. The ADC errors, like gain errors in the integrators, are less important since they are in the forward, high-gain path of the modulator.

#### *Simulating a Multibit NS Modulator Using SPICE*

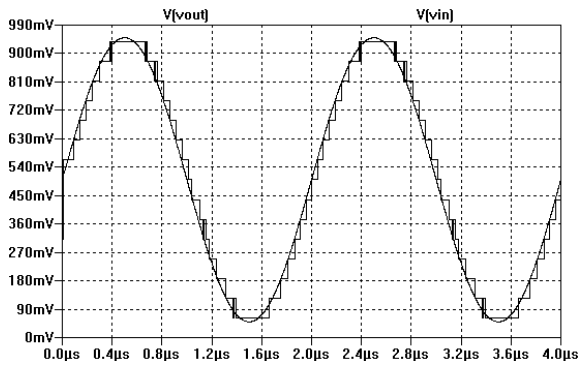
Figure 7.44 shows a circuit-level implementation of a first-order, multibit, NS modulator using a 4-bit ADC and DAC. Figure 7.45 shows the SPICE simulation outputs of this modulator. Most of the design effort, when developing multi-bit modulators, goes into the design of the feedback DAC. Because it is nearly impossible to design highly accurate (say 12-bits resolution or better) DACs without trimming, or some sort of error correction, methods have been developed that attempt to randomize DAC errors. If the errors appear as a random variable, they may appear as white noise in the output spectrum and not affect the  $SNR$  of the data converter.

Figure 7.46 shows one possible implementation of a DAC. This DAC utilizes resistive unit elements, resistors laid out in a square that connect, on one side, between  $VDD$  and ground while the other side connects to a rotating switch connected to the analog output. In other words, in one case we connect  $VDD$  to one corner of the resistor



**Figure 7.44** Circuit implementation of a first-order multi-bit NS modulator.

cube and ground to the opposite corner (assuming  $V_{REF+} = VDD$  and  $V_{REF-} = 0$ ). There exist two voltage dividers along each of the sides of the resistor square. The output of the DAC can change from zero, to  $(1/8)VDD$ , to  $(2/8)VDD$ , ... up to  $(8/8)VDD$ . Depending on the output of the decoder, one tap from each side is fed to the analog output. Because there are two sides, the outputs from each side are combined and effectively averaged.



**Figure 7.45** Output of the multi-bit modulator in Fig. 7.44.

The purpose of the counter is to vary the connections of  $VDD$  and ground around the outside of the resistive divider to randomize variations in the output voltage due to resistor mismatch. In order to understand this in more detail, consider a constant DAC output voltage of  $VDD/2$ . As the counter changes output values, so do the connections to  $VDD$  and ground in the resistor string. In order to keep a constant output voltage of  $VDD/2$  the switches in the center of the DAC move accordingly based on the output of the counter and the input to the decoder. In this way variations in the resistors, hopefully, average out to a constant value.

With a little thought the reader can think of other schemes to attempt to randomize the errors that are fed back and subtracted from the input. In all cases it's presumed, for these techniques to work correctly, that the DAC errors average to zero or a very small value.

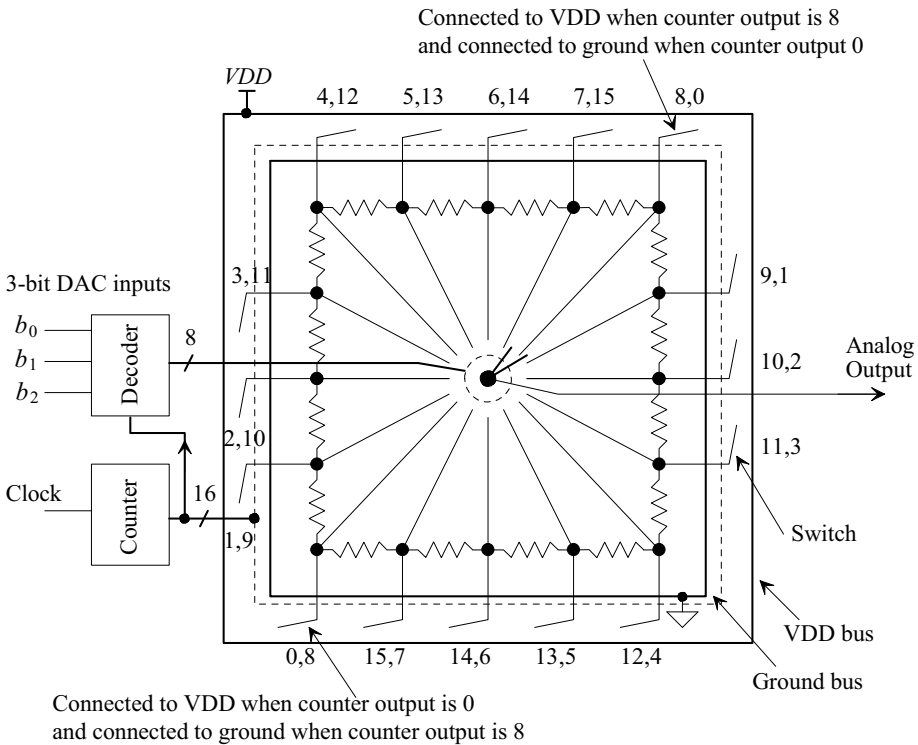


Figure 7.46 Implementation of a DAC for use in a multibit NS modulator.

### 7.3.5 Error Feedback

The NS topologies we've discussed so far are sometimes called *interpolative modulators* since the signal fed back is the average of the input signal interpolated between known values of the modulator output (the average of the modulator outputs is the input signal). However, NS modulators were first introduced (see C. C. Cutler, "Transmission systems employing quantization," 1960, U.S. Patent No. 2,927,962 [filed 1954]) using the error feedback topology shown in Fig. 7.47. Error feedback topologies are not used in analog input modulators because errors in the analog subtraction directly add to the input signal. We can use this topology, however, in the implementation of a digital input demodulator (sometimes also called a modulator), as the subtraction is digital.

Looking at Fig. 7.47 we note that by definition the difference between the input and the output of the quantizer is the quantization noise,  $V_{Qe}(z)$ . This noise is subtracted from the input after a delay (for a first-order modulator) resulting in

$$v_{out}(z) = v_{in}(z) - F(z) \cdot V_{Qe}(z) + V_{Qe}(z) = v_{in}(z) + V_{Qe}(z)[1 - F(z)] \quad (7.94)$$

Note that the signal transfer function for an error feedback-based modulator is simply one; that is,  $STF(f) = 1$ . For a first-order NS modulator we set  $F(z) = z^{-1}$  (a register), which results in

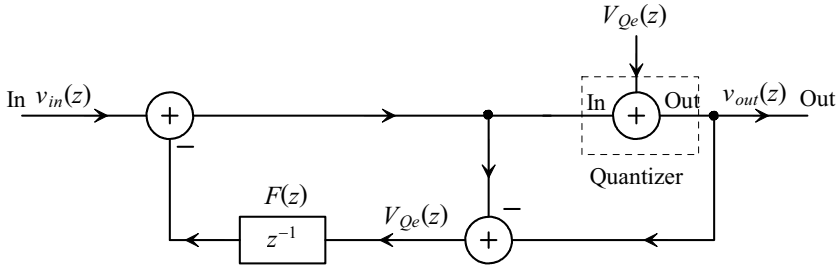


Figure 7.47 Block diagram of an error feedback modulator.

$$v_{out}(z) = v_{in}(z) + V_{Qe}(z) \cdot (1 - z^{-1}) \tag{7.95}$$

A second-order modulator with a  $NTF(f) = (1 - z^{-1})^2$  would use a feedback filter, noticing from Eq. (7.94) that  $NTF(f) = 1 - F(z)$ , of

$$F(z) = 1 - (1 - z^{-1})^2 = z^{-1} \cdot (2 - z^{-1}) \tag{7.96}$$

Implementation of a second-order NS modulator is shown in Fig. 7.48. Note that when trying to implement higher-order modulators using error feedback we run into the same problem we encountered when using an interpolative modulator, namely, instability resulting from a  $NTF$  that is too large at higher-frequencies. As with interpolative modulators, we can design the  $NTF$  to have a highpass response.

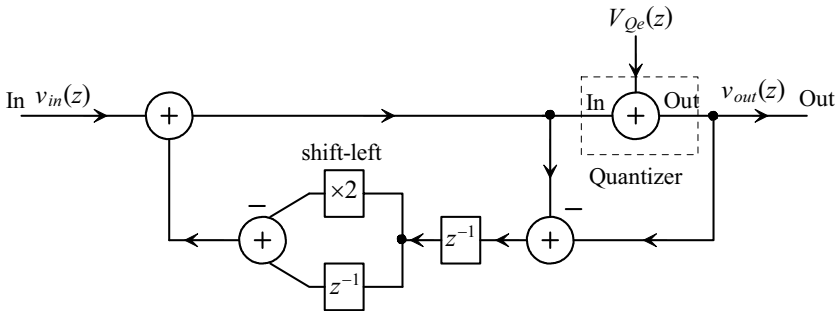
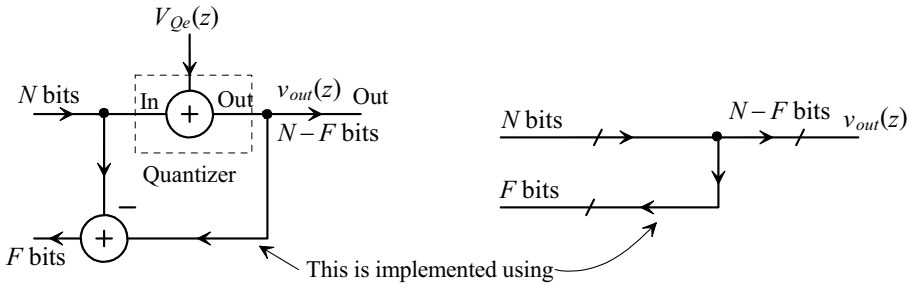


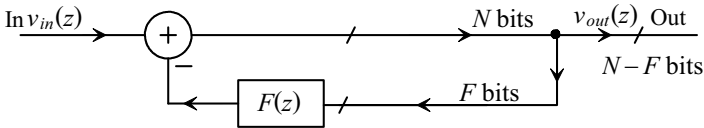
Figure 7.48 Block diagram of a second-order error feedback modulator.

We've introduced the error feedback topology with the idea that it can be used in a modulator (demodulator) that performs digital-to-analog conversion. We first introduced a modulator for use in a DAC back in Fig. 7.5. At this point we need to answer the question, "Why is the NS topology of Fig. 7.47 a better choice for DAC implementation, in general, than the topologies of Figs. 7.5 and 7.41?" The answer to this comes from the realization that the quantizer and difference block in Fig. 7.47 can be implemented by simply removing lower bits from the digital input words. This is illustrated in Fig. 7.49. The resulting error feedback modulator will be simpler to implement than the modulators based on interpolative topologies. Figure 7.50 shows Fig. 7.47 redrawn to show the simpler implementation.





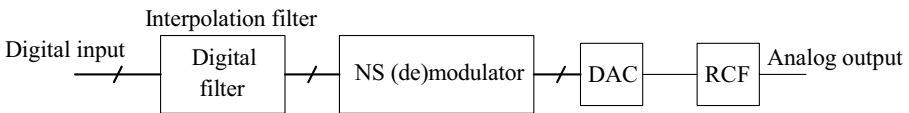
**Figure 7.49** Showing how the quantizer and difference block are implemented.



**Figure 7.50** Block diagram of an error feedback modulator.

The number of bits used in the modulator,  $N$ , is selected to avoid overflow when the maximum input signal and fed-back signal are subtracted. When using two's complement numbers, the words input to the adder must be the same length. The smaller word's MSB is used to increase the smaller word's size until the word lengths match. We'll comment more on this important concern in a moment.

Figure 7.51 shows the block diagram of an NS-based DAC. As we saw in Fig. 7.4, if a 1-bit output is used, the modulator can be connected directly to the reconstruction filter (RCF). The 1-bit DAC is perfectly linear so distortion concerns are reduced. Using a multibit modulator and DAC gives a better SNR, for a given oversampling ratio and modulator order, as well as easing the requirements placed on the RCF. The drawback, as discussed earlier, is that the DAC must be accurate to the final desired output resolution since it is in series with the output signal path.



**Figure 7.51** DAC using a NS modulator and digital filter.

Let's look at how to estimate the quantization noise added to the signal from the error feedback quantization process. Assuming we are using two's complement numbers we know that

$$\overbrace{0111111\dots}^{N \text{ bits}} = V_{REF+} - \overbrace{\frac{V_{REF+} - V_{REF-}}{2^N}}^{1 \text{ LSB}} \quad (7.97)$$

and

$$1000000\dots = V_{REF-} \quad (7.98)$$

For the DAC to function properly we must change the numbers back to binary offset (complement the left-most or most-significant bit) unless the DAC input uses two's complement format. This is easy to see if the output of the modulator is a single bit ( $N - F = 1$ ) since an MSB of 1 =  $V_{REF+}$  and a 0 =  $V_{REF-}$  where  $V_{LSB} = V_{REF+} - V_{REF-}$ . By dropping  $F$  bits the voltage weighting of an LSB in the modulator output can be written as

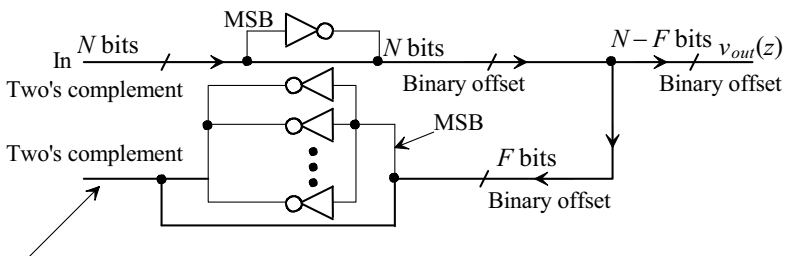
$$V_{LSB} = \frac{V_{REF+} - V_{REF-}}{2^{N-F}} \text{ if } N - F > 1 \quad (7.99)$$

This result is used in Eq. (7.6) to estimate the quantization noise spectrum in a NS modulator.

*Implementation Concerns*

We know from our discussions in the last chapter that most digital additions and subtractions utilize two's complement numbers because of the simplicity (see Sec. 4.1.3 and the associated discussion) in implementing the hardware. However, consider the two's complement  $N$ -bit input in Fig. 7.49. If we drop the lower  $F$  bits, the resulting number fed back to  $F(z)$  (the quantization noise) is not in two's complement format.

In order to circumvent these types of problems, the topology shown in Fig. 7.52 can be used. The input to the quantizer/subtractor is changed from two's complement format into binary offset format. (See Figs. 4.4 and 4.5 for a comparison of the formats.) Quantization is then performed; the lower bits are dropped from the output and fed back. The fed-back word (the quantization error) is then changed from a binary offset number back into a two's complement number. The size of the word fed back is adjusted to match the size of the modulator's input (knowing that the words used in two's complement arithmetic must be the same size so that the sign bit is in the same location in each word, see also Fig. 4.7).



Adjust the output word size so that it matches the modulator's input word size.

**Figure 7.52** Implementation of the quantizer and difference blocks.

### 7.3.6 Cascaded Modulators

The NS modulators discussed up to this point, in this chapter, have been single feedback loop topologies with the general form seen in Fig. 5.38. This includes the higher-order topologies discussed in Sec. 7.3.1 and the error-feedback topologies of the last section. In this section we discuss cascaded or multistage NS modulators. The cascaded modulators discussed here are sometimes called *Multistage noise SHaping or MASH modulators*. While our focus in this section is on modulators for ADCs, it is easy to extend the theory to modulators used in DACs.

We indicated, in the last section, that feeding back the quantization noise,  $V_{Qe}(z)$ , to the input isn't practical in analog implementations of NS modulators. The output of the analog subtraction,  $V_{Qe}(z)$ , would be added directly to the input signal. Instead of feeding  $V_{Qe}(z)$  back to the input, cascaded modulators feed it forward to the input of another modulator. The second modulator's output is then a delayed version of  $V_{Qe}(z)$  as well as its own unwanted modulation noise. If this output is subtracted from the output of the first modulator, we can effectively reduce the resulting overall quantization noise.

The major benefit of a cascaded topology is stability. Unconditionally stable first- and second-order loops can be cascaded to implement higher-order modulators. In addition, as we'll briefly discuss, modulators consisting of a first-stage modulator using a 1-bit ADC and DAC followed by a multibit modulator can provide reasonable resolutions with low oversampling ratio  $K$ .

#### Second-Order (1-1) Modulators

A second-order NS modulator can be implemented using a cascade of two first-order modulators (called a 1-1 modulator), as seen in Fig. 7.53. The output of the first modulator is given by

$$v_1(z) = z^{-1}v_{in}(z) + (1 - z^{-1})V_{Qe1}(z) \quad (7.100)$$

while the output of the second modulator is

$$v_2(z) = -z^{-1}V_{Qe1}(z) + (1 - z^{-1})V_{Qe2}(z) \quad (7.101)$$

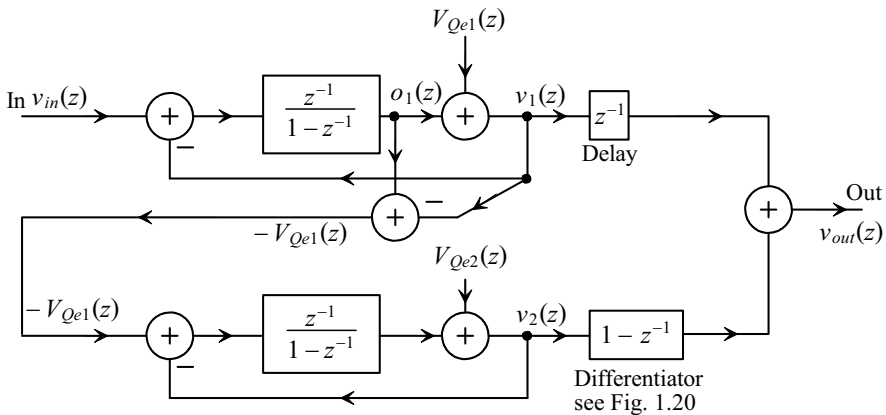


Figure 7.53 Second-order (1-1) cascaded modulator.

The overall modulator output is given by

$$\begin{aligned} v_{out}(z) &= z^{-1}v_1(z) + (1 - z^{-1})v_2(z) \\ &= z^{-2}v_{in}(z) + z^{-1}(1 - z^{-1})V_{Qe1}(z) - z^{-1}(1 - z^{-1})V_{Qe1}(z) + (1 - z^{-1})^2V_{Qe2}(z) \\ &= z^{-2}v_{in}(z) + (1 - z^{-1})^2V_{Qe2}(z) \end{aligned} \quad (7.102)$$

Note that the second modulator is used to subtract the first's quantization noise,  $V_{Qe1}(z)$ , from the final output. If all of the components are ideal, the resulting modulator has second-order noise shaping. In practice, however, the coefficients of  $V_{Qe1}(z)$  in Eq. (7.102) will not exactly cancel. When this occurs,  $V_{Qe1}(z)$  is said to *leak to the output of the modulator*. Differences in the coefficients are caused by gain errors in the first modulator's analog integrator when compared to the output of the digital differentiator.

Let's attempt to characterize the performance of the 1-1 modulator if the integrators have gain coefficients,  $G_I$ , other than one, as seen in Fig. 7.13. We can write the output of the first modulator's integrator in Fig. 7.53 as

$$o_1(z) = \frac{G_I \cdot z^{-1}}{1 + (G_F - 1)z^{-1}} \cdot v_{in}(z) - \frac{G_I \cdot z^{-1}}{1 + (G_F - 1)z^{-1}} \cdot V_{Qe1}(z) \quad (7.103)$$

Using Eq. (7.26) with this equation we can write

$$V_{Qe1out}(z) = v_1(z) - o_1(z) = \frac{(G_F - G_I) \cdot z^{-1}}{1 + (G_F - 1)z^{-1}} \cdot v_{in}(z) + \frac{1 - (1 - G_I) \cdot z^{-1}}{1 + (G_F - 1)z^{-1}} \cdot V_{Qe1}(z) \quad (7.104)$$

where, ideally, the output quantization noise of the first modulator,  $V_{Qe1out}(z)$ , is  $V_{Qe1}(z)$ . If the modulator is functioning properly, then  $G_F = 1$  independent of  $G_I$  as discussed earlier. Equation (7.104) can then be written as

$$V_{Qe1out}(z) = (1 - G_I) \cdot z^{-1} \cdot v_{in}(z) + [1 - (1 - G_I) \cdot z^{-1}] \cdot V_{Qe1}(z) \quad (7.105)$$

Using this equation in Eq. (7.101) while assuming the second modulator uses an integrator scaling factor,  $G_{I2}$ , and  $G_{F2}$  is one results in (rewriting Eq. [7.102])

$$\begin{aligned} v_{out}(z) &= z^{-2}v_{in}(z) + z^{-1}(1 - z^{-1})V_{Qe1}(z) - z^{-1}(1 - z^{-1})V_{Qe1out}(z) + (1 - z^{-1})^2V_{Qe2}(z) \\ &= \underbrace{z^{-2}v_{in}(z) + (1 - z^{-1})^2V_{Qe2}(z)}_{\text{Desired output}} + \underbrace{[V_{Qe1}(z) - v_{in}(z)] \cdot z^{-2}(1 - z^{-1}) \cdot (1 - G_I)}_{\text{Unwanted term}} \end{aligned} \quad (7.106)$$

While we can set the second modulator's integrator gain coefficient,  $G_{I2}$ , to 0.4 to avoid integrator saturation, as discussed earlier, we must set  $G_{I1}$  as close to unity as possible. Using a unity gain coefficient results in a reduction in the modulator's overall dynamic range (see Fig. 7.12 and the associated discussion). Note that the input signal appears in the unwanted term in Eq. (7.106). It should be obvious at this point that we can add scaling parameters at various points in the modulator to attempt to maximize the modulator's dynamic range. Also note that the number of bits in the 1-1 modulator's output will be more than one bit (two bits if comparators are used in each first-order modulator).

*Third-Order (1-1-1) Modulators*

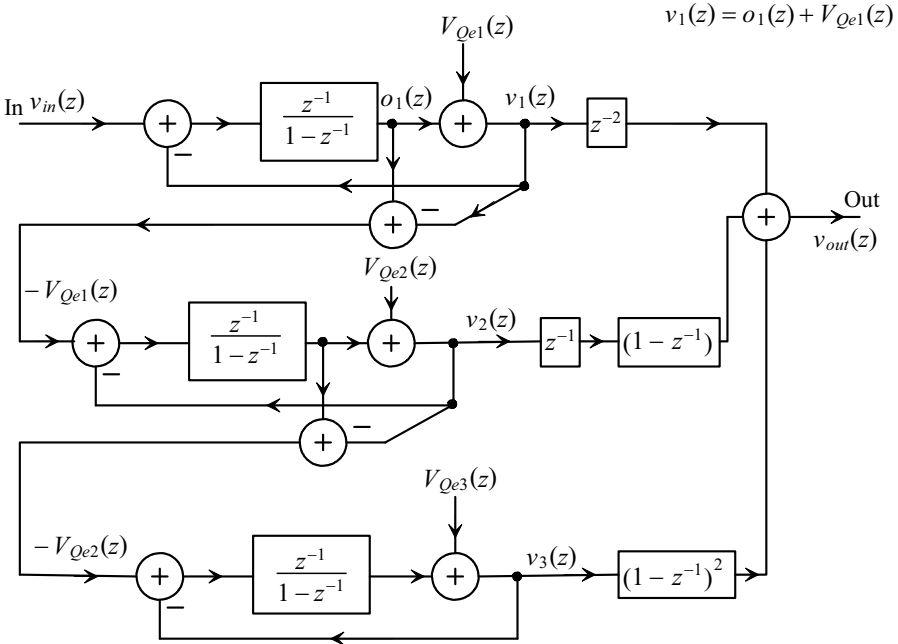
By adding a third first-order modulator to our 1-1 modulator of Fig. 7.53, we get a 1-1-1 or third order modulator, Fig. 7.54. The output of the added third modulator can be written as

$$v_3(z) = -z^{-1}V_{Qe2}(z) + (1 - z^{-1})V_{Qe3}(z) \tag{7.107}$$

while the ideal output of the 1-1-1 cascade is given by

$$v_{out}(z) = v_1(z) \cdot z^{-2} + v_2(z)(1 - z^{-1}) + v_3(z)(1 - z^{-1})^2 = z^{-3}v_{in}(z) + (1 - z^{-1})^3V_{Qe3}(z) \tag{7.108}$$

Again, as we saw in Eq. (7.106), noise from the first modulator can leak through to the output and spoil the overall cascade's SNR. Indeed, if the leakage from the first modulator is large enough, we get no benefit from adding the third modulator. Notice, in Eq. (7.106), that the unwanted term exhibits first-order differentiation,  $(1 - z^{-1})$ . We might expect better overall performance, that is, less leakage if the first modulator is second order. The unwanted term would then exhibit second-order differentiation.

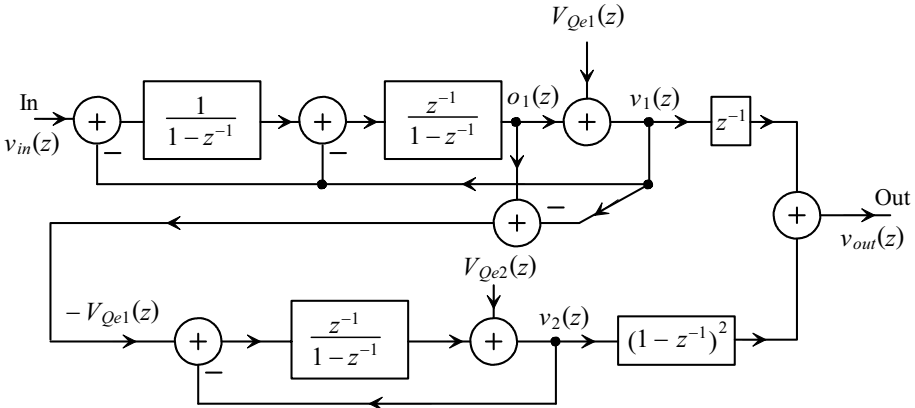


**Figure 7.54** Third-order (1-1-1) cascaded modulator.

*Third-Order (2-1) Modulators*

A third-order modulator formed by using a second-order modulator followed by a first-order modulator is shown in Fig. 7.55. The output of the first modulator is given by

$$v_1(z) = z^{-1}v_{in}(z) + (1 - z^{-1})^2V_{Qe1}(z) \tag{7.109}$$



**Figure 7.55** Third-order (2-1) cascaded modulator.

while the output of the second modulator is

$$v_2(z) = -z^{-1}V_{Qe1}(z) + (1 - z^{-1})V_{Qe2}(z) \quad (7.110)$$

The output of the 2-1 modulator is then, ideally,

$$v_{out}(z) = v_1(z)z^{-1} + (1 - z^{-1})^2 v_2(z) = z^{-2}v_{in}(z) + (1 - z^{-1})^3 V_{Qe2}(z) \quad (7.111)$$

Let's attempt to characterize the leakage to the output by first determining the output of the second integrator  $o_1(z)$  (the input to the comparator). We'll use the topology shown in Fig. 7.32, with  $G_3 = 1$ , to define our gains. The output,  $o_1(z)$ , is (assuming that  $G_F = G_1 G_2 G_c = 1$ )

$$o_1(z) = \frac{G_1 G_2 \cdot z^{-1} v_{in}(z) - [(G_1 G_2 + G_2) - G_2 z^{-1}] \cdot z^{-1} V_{Qe1}(z)}{1 + z^{-1} \cdot (G_2 G_c - 1) + z^{-2}(1 - G_2 G_c)} \quad (7.112)$$

Again, writing the input to the second modulator as (using Eq. [7.61])

$$\begin{aligned} V_{Qe1out}(z) &= v_1(z) - o_1(z) \\ &= \frac{(1 - G_1 G_2) \cdot z^{-1} v_{in}(z) + [(1 - z^{-1})^2 + (G_1 G_2 + G_2) \cdot z^{-1} - G_2 z^{-2}] V_{Qe1}(z)}{1 + z^{-1} \cdot (G_2 G_c - 1) + z^{-2}(1 - G_2 G_c)} \end{aligned} \quad (7.113)$$

noting that if  $G_1 = G_2 = G_c = 1$  then  $V_{Qe1out}(z) = V_{Qe1}(z)$ . If we write the output of the cascade as

$$v_{out}(z) = z^{-2}v_{in}(z) + z^{-1}(1 - z^{-1})^2 V_{Qe1}(z) - z^{-1}(1 - z^{-1})^2 V_{Qe1out}(z) + (1 - z^{-1})^3 V_{Qe2}(z) \quad (7.114)$$

then

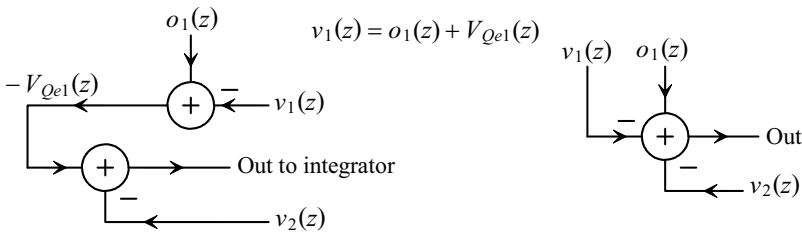
$$\begin{aligned} v_{out}(z) &= \overbrace{z^{-2}v_{in}(z) + (1 - z^{-1})^3 V_{Qe2}(z)}^{\text{Desired output}} + \\ & z^{-1}(1 - z^{-1})^2 \left[ \overbrace{\frac{(1 - G_1 G_2) \cdot z^{-1} v_{in}(z) + [(1 - G_2) - (G_2 G_c - G_2)z^{-1}] \cdot z^{-1} V_{Qe1}(z)}{1 + z^{-1} \cdot (G_2 G_c - 1) + z^{-2}(1 - G_2 G_c)}}^{\text{Undesired term}} \right] \end{aligned} \quad (7.115)$$

When this equation is compared to Eq. (7.106), we see that the undesired term is second-order differentiated. Also, we have more control over the integrator gains. Third-order modulators using the 2-1 topology are much more robust than the 1-1-1-based topology and can provide output signals free of unwanted tones. Again, if integrator saturation (and thus dynamic range) isn't a concern, then we can set  $G_1 = G_2 = 1$ .

One of the interesting uses of the 2-1 modulator is the configuration where the first (second-order) modulator utilizes a 1-bit ADC and DAC, while the second (first-order) modulator utilizes a multibit ADC and DAC. The overall linearity of this topology is dominated by the second-order modulator, while the multibit modulator provides an enhancement in dynamic range for a given oversampling ratio. These very interesting data converters are discussed in greater detail in [7].

*Implementing the Additional Summing Input*

Before leaving our introduction to cascaded converters, let's discuss the implementation of the extra summing block used to generate the quantization noise,  $V_{Qe}(z)$ . Figure 7.56 shows the topology of the two summing blocks and how they can be combined.



**Figure 7.56** Showing implementation of the dual summing block as a single block.

One way to implement the extra subtracting input and the integrator is shown in Fig. 7.57. This DAI is a modification of the DAI shown in Fig. 7.33. The output of this integrator is related to the inputs by

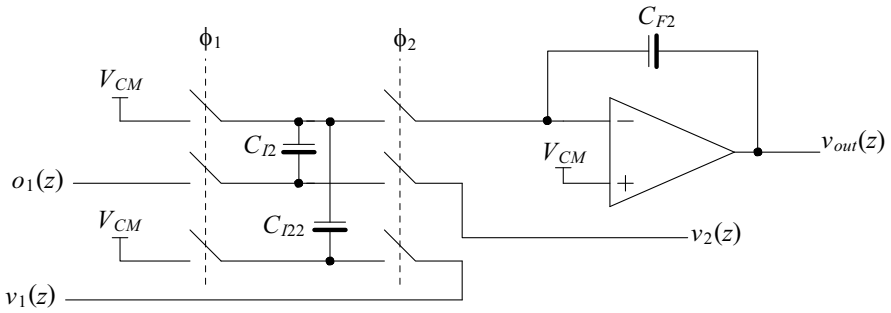
$$v_{out}(z) = o_1(z) \cdot \frac{C_{I2}}{C_{F2}} \cdot \frac{z^{-1/2}}{1-z^{-1}} - v_2(z) \cdot \frac{C_{I2}}{C_{F2}} \cdot \frac{1}{1-z^{-1}} - v_1(z) \cdot \frac{C_{I22}}{C_{F2}} \cdot \frac{1}{1-z^{-1}} \quad (7.116)$$

If we set  $C_{I2} = C_{I22} = C_{F2}$  and we realize that the comparator in the second modulator, assuming it is clocked with the rising edge of  $\phi_1$  (or the falling edge of  $\phi_2$ ), adds a half-clock cycle delay in series with the  $o_1(z)$  input and a full clock cycle delay in series with  $v_1(z)$  and  $v_2(z)$ , then we can write

$$v_{out}(z) = [o_1(z) - v_1(z) - v_2(z)] \cdot \frac{z^{-1}}{1-z^{-1}} \quad (7.117)$$

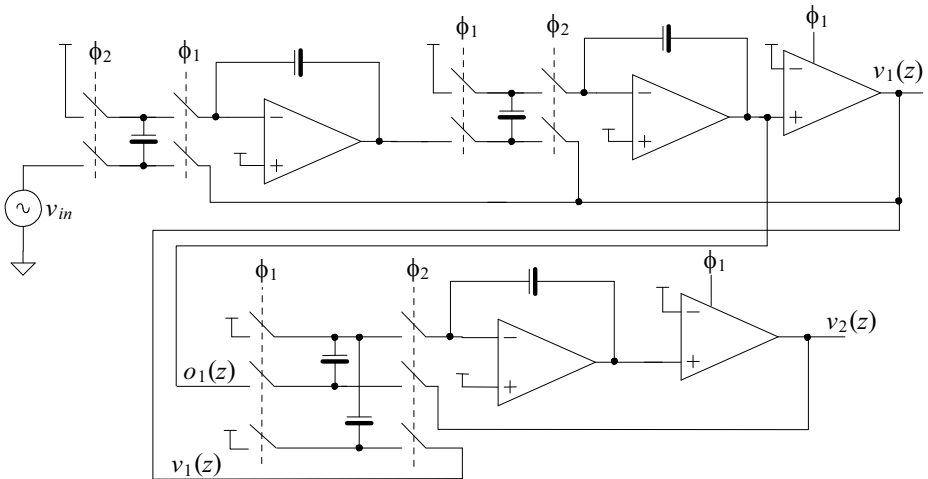
Figure 7.58 shows the implementation of a 2-1 modulator.

We could also use the topology shown in Fig. 7.59 to implement the summing block of Fig. 7.56. This topology has the benefit of using a single capacitor for a simpler circuit and no matching differences between  $C_{I2}$  and  $C_{I22}$ . Unfortunately, the topology is no longer insensitive to the parasitic capacitance on the top plate of the switched capacitor. In the parasitic insensitive topologies, Fig. 7.57 for example, the top plate of



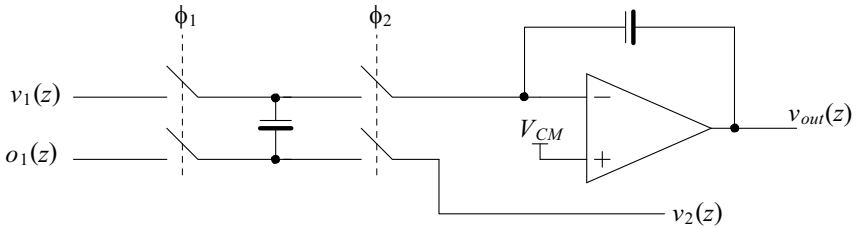
**Figure 7.57** Implementing the dual summing block for a cascaded modulator.

the capacitor is always held at the common-mode voltage,  $V_{CM}$ . In the topology of Fig. 7.59 the top plate is charged to  $v_1(t)$  when the  $\phi_1$  switches are closed and discharged to  $V_{CM}$  when the  $\phi_2$  switches are closed. The difference between these voltages combined with the value of the unwanted parasitic capacitance to ground on the top plate causes unwanted charge to transfer to the feedback capacitor and a gain error. This by itself isn't too bad. However, the unwanted capacitance can have a large depletion capacitance component, resulting in a voltage-dependent capacitance and thus nonlinear gain. Nevertheless, in some applications this topology may still prove useful.



**Figure 7.58** Implementation of a 2-1 NS modulator.





**Figure 7.59** Implementing the dual summing block with a single capacitor results in sensitivity to the top plate parasitic capacitance.

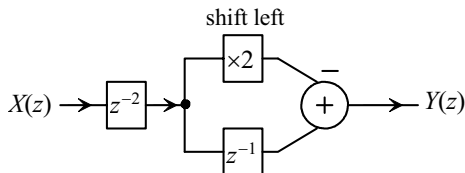
### ADDITIONAL READING

- [1] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, Wiley-IEEE Press, 2005. ISBN 978-0471465850
- [2] S. K. Dunlap and T.S. Fiez, "A Noise-Shaped Switching Power Supply using a Delta-Sigma Modulator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 51, No. 6, pp. 1051 - 1061, June 2004
- [3] A. Eshraghi and T.S. Fiez, "A Comparative Analysis of Parallel Delta-Sigma ADC Architectures," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 51, No. 3, pp. 450 - 458, March 2004
- [4] S. R. Norsworthy, R. Schreier, and G. C. Temes (eds.), *Delta-Sigma Data Converters: Theory, Design, and Simulation*, Wiley-IEEE Press, 1997. ISBN 978-0780310452
- [5] R. T. Baird and T. S. Fiez, "Linearity Enhancement of Multibit  $\Delta\Sigma$  A/D and D/A Converters using Data Weighted Averaging," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 42, No. 12, pp. 753 - 762, December 1995
- [6] J. C. Candy and G. C. Temes (eds.), *Oversampling Delta-Sigma Data Converters*, Wiley-IEEE Press, 1992. ISBN 978-0879422851
- [7] B. P. Brandt and B. A. Wooley, "A 50-MHz Multibit Sigma-Delta Modulator for 12-b 2-MHz A/D Conversion," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 12, pp. 1746 - 1756, December 1991
- [8] B. E. Boser and B. A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 12, pp. 1298 - 1308, December 1988
- [9] B. E. Boser, K. P. Karmann, H. Martin, and B. A. Wooley, "Simulating and Testing Oversampled Analog-to-Digital Converters," *IEEE Transactions on Computer-Aided Design*, Vol. 7, pp. 668 - 674, June 1988
- [10] J. C. Candy, B. A. Wooley, and O. J. Benjamin, "A Voiceband Codec with Digital Filtering," *IEEE Transactions on Communications*, Vol. 29, pp. 815 - 830, June 1981

**QUESTIONS**

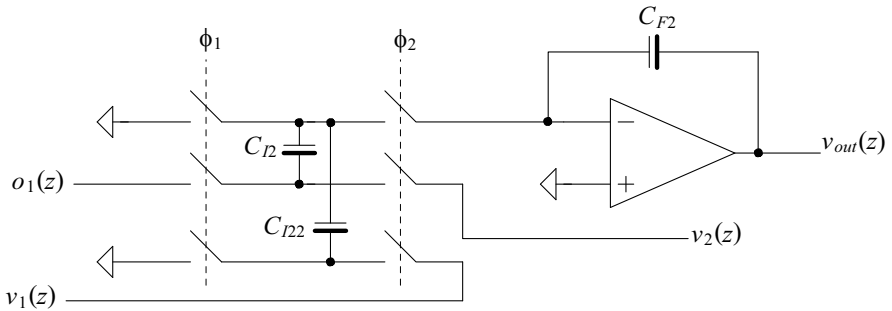
- 7.1** Show how to derive Eqs. (7.1) and (7.2) from the block diagram seen in Fig. 7.1.
- 7.2** After reviewing Sec. 2.2.3, would it be possible to replace the delaying integrator seen in Fig. 7.2 with a non-delaying integrator? If so, what is the *NTF* and *STF* of the modulator? Is the modulator stable?
- 7.3** Using SPICE simulations, show how passing the digital signal seen in Fig. 7.3 through an RC lowpass filter will reduce the modulation noise in the signal and help to recover the original analog input signal. What happens to the original signal's amplitude if it's filtered, by the added RC filter, too much?
- 7.4** Show the spectrums (modulator input, digital output, and analog output after filtering) of the signals in question 7.3. Discuss what the spectrums indicate.
- 7.5** If an extra delay,  $z^{-1}$ , was added to the forward path of the modulator in Fig. 7.2 would the resulting topology be stable? Why or why not?
- 7.6** Show, using timing diagrams, how Eq. (7.3) is correct.
- 7.7** For the NS modulator shown in Fig. 7.5 used for digital to analog conversion, what component serves as the ADC? What component serves as the DAC?
- 7.8** Explain how the quantizer in Fig. 7.5 functions.
- 7.9** What are we assuming about an input signal if the modulation noise follows Eq. (7.5)?
- 7.10** What is the magnitude of Eq. (7.5) (plot it against frequency)?
- 7.11** What is the difference between quantization noise and modulation noise?
- 7.12** Show the steps and assumptions leading to Eq. (7.12).
- 7.13** Is the statement on page 238 that "every doubling in the oversampling ratio results in 1.5 bits increase in resolution" really true if  $K$  is small? Explain.
- 7.14** Does noise-shaping work for DC input signals? If so, how?
- 7.15** Show the steps leading up to Eq. (7.22).
- 7.16** What is the difference between a NS ADC and a Nyquist ADC?
- 7.17** In your own words, describe ripple in the output of a digital filter connected to an NS modulator.
- 7.18** Does adding a dither signal to the input of a NS modulator help reduce the peak-to-peak ripple in the digital filter output? Does it help to break up tones in the filter's output?
- 7.19** Derive Eq. (7.26).
- 7.20** Repeat Ex. 7.3 if the integrator's gain is set to 0.5.
- 7.21** Estimate the range of  $G_c$  for the quantizer seen in Fig. 7.16. How does this compare to the range of  $G_c$  for the 1-bit quantizer seen in Fig. 7.15? Name two benefits of the 1-bit quantizer over multi-bit quantizers.

- 7.22** Verify that Eq. 7.30 is correct. Use pictures if needed.
- 7.23** In your own words, and without equations, describe integrator leakage. How would you relate integrator leakage, found in integrators that use an active element as seen in the NS modulators found in this chapter, to the passive integrators used in the NS modulators discussed in the last chapter?
- 7.24** Would large parasitic op-amp input capacitance affect the settling time of a DAI? Verify your answer using simulations with ideal op-amps (infinite open-loop gain) and non-ideal op-amps (open-loop gains around the oversampling ratio,  $K$ ).
- 7.25** In your own words, how does oversampling affect input-referred offset/noise and the effects of a jittery clock on an NS data converter?
- 7.26** Determine the transfer function of the DAI shown in Fig. 7.20.
- 7.27** Derive Eq. (7.51).
- 7.28** Sketch the implementation of the fully-differential second-order NS modulator.
- 7.29** Derive Eq. (7.61).
- 7.30** Sketch the fully-differential equivalent of Fig. 7.33.
- 7.31** Resimulate the modulator in Ex. 7.4 if the gains are set to one. Comment on the stability of the resulting circuit.
- 7.32** Resimulate the modulator in Ex. 7.4 if the input is only 50 mV. Comment on the stability of the resulting circuit.
- 7.33** Regenerate Fig. 7.40 by selecting integrator gains so that the maximum output swing of any op-amp is 800 mV peak-to-peak.
- 7.34** Comment, in your own words, on why the actual SNR of a NS-based data converter can be worse than the ideal values calculated in the chapter.
- 7.35** Derive Eq. (7.75). Make sure each step of the derivation includes comments.
- 7.36** Resimulate Fig. 7.44 using two-bit ADC and DAC.
- 7.37** Sketch a possible implementation of a quantizer for the error feedback modulator shown in Fig. 7.48.
- 7.38** What transfer function does the following block diagram implement?



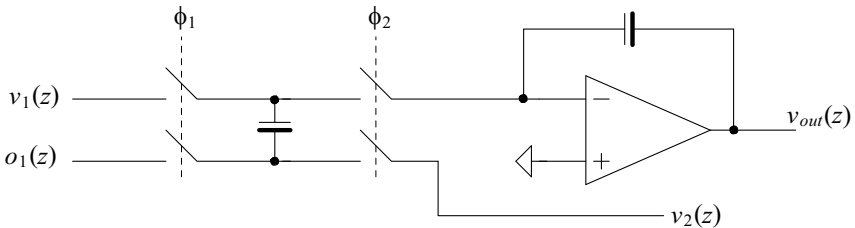
**Figure 7.60** Circuit for question 7.38.

- 7.39** In Fig. 7.54 sketch the block diagram implementation of the circuit in series with the  $v_2(z)$  output.
- 7.40** Derive the transfer function of the topology seen in Fig. 7.61 (show details of your derivation). What is the input common-mode voltage of the op-amp? Is this a concern when not using a negative supply voltage? If the input signals have a common-mode of  $VDD/2$ , does this affect the common-mode voltage of the circuit's output (remember that the op-amp is part of an integrator). Would it be a good idea, now that the inputs of the op-amp and the top plates of the capacitors are tied to ground or the virtual ground of the op-amp, to swap the bottom and top plates of the capacitors? Why or why not? Use SPICE to support your answers.



**Figure 7.61** Circuit used in question 7.40.

- 7.41** Repeat question 7.40 for the op-amp circuit seen in Fig. 7.62.



**Figure 7.62** Circuit used in question 7.41.