Chapter

8

Bandpass Data Converters

The data converter topologies we've covered in the last few chapters have performed analog-to-digital conversion on a range of frequencies extending from DC to some frequency, *B*. These topologies are sometimes called lowpass data converters. In this chapter we develop the idea that we can perform data conversion on a bandwidth of frequencies that doesn't include DC. The topologies developed in this chapter are called bandpass data converters. Bandpass data converters are useful in communication circuits, especially wireless communications, where the information is modulated up to some higher frequency and thus contained in some fixed bandwidth in the frequency spectrum.

Before developing the idea of a bandpass data converter, let's review, on pages 4 through 6, why in-phase (*I*) and quadrature (*Q*) signals are used in communication systems. In simple terms, *I*/*Q* signals are used because we can send more information without increasing the bandwidth of the transmission channel. Note that other schemes that use several phase-shifted sinewaves (e.g., 0, 30, 60, and 90 degrees) may also be employed to further increase the information transmitted without increasing the channel bandwidth. In this chapter, however, we focus only on 0 and 90 degree phase-shifted (*I*/*Q*) sinewaves.

As seen in Fig. 1.6 and Eq. (1.11), summing *I* and *Q* components results in the *I*/*Q* signal. Figure 8.1 shows time-domain, equal amplitude, *I* and *Q* signals and their sum (the *I*/*Q* signal). The phase shift of the *I*/*Q* signal leads the *Q* component by 45 degrees while lagging the *I* component by 45 degrees when equal amplitude *I* and *Q* signals are used. By varying the amplitude of either (or both) the *I* or *Q* signals we vary the phase shift and amplitude of the *I*/*Q* signal (this variation in amplitude and phase shift represent the information we are transmitting). Note that this modulation scheme is often called *quadrature amplitude modulation* (*QAM*).

In order to recover the information from the *I* and *Q* components in the *I*/*Q* signal let's first write, see Eq. (1.10),

$$S_{IQ}(t) = A_I \cdot \cos 2\pi f_c \cdot t + A_Q \cdot \sin 2\pi f_c \cdot t \qquad (8.1)$$

where f_c represents the frequency of a carrier signal while A_I and A_Q represent the information we are transmitting. Both A_I and A_Q vary with time and thus have some

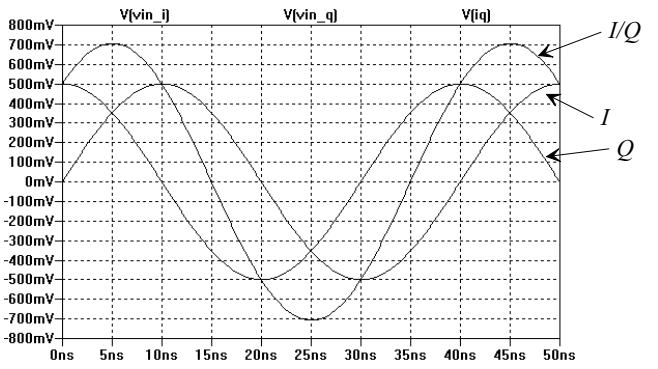


Figure 8.1 In-phase (I), quadrature (Q) signals, and I/Q signals.

spectral representation, $A_I(f)$ and $A_Q(f)$. The A_I component amplitude modulates the cosine term while the A_Q component amplitude modulates the sine term.

In order to recover the A_I and A_Q in the receiver we can multiply the received signal, ideally a scaled version of $S_{IQ}(t)$, by cosine and sine signals. For A_I,

$$S_{IQ}(t) \cdot \cos 2\pi f_c \cdot t = (A_I \cdot \cos 2\pi f_c \cdot t + A_Q \cdot \sin 2\pi f_c \cdot t) \cdot \cos 2\pi f_c \cdot t \tag{8.2}$$

Knowing

$$\cos A \cdot \sin B = \tfrac{1}{2}(\sin [B - A] + \sin [A + B]) \tag{8.3}$$

$$\cos A \cdot \cos B = \tfrac{1}{2}(\cos [B - A] + \cos [A + B]) \tag{8.4}$$

we get

$$S_{IQ}(t) \cdot \cos 2\pi f_c \cdot t = \underbrace{\frac{A_I(f)}{2}}_{\text{Desired signal}} + \underbrace{\frac{A_I}{2} \cdot \cos 2\pi 2 f_c \cdot t + \frac{A_Q}{2} \cdot \sin 2\pi 2 f_c \cdot t}_{\text{Remove by passing through a lowpass filter}} \tag{8.5}$$

The A_I component can be recovered by passing this signal through a lowpass filter to remove the higher frequency components. Note that it's assumed the maximum frequency of interest in $A_I(f)$ is less than f_c.

In order to recover A_Q from the received signal we multiply by a sinewave or

$$S_{IQ}(t) \cdot \sin 2\pi f_c \cdot t = (A_I \cdot \cos 2\pi f_c \cdot t + A_Q \cdot \sin 2\pi f_c \cdot t) \cdot \sin 2\pi f_c \cdot t \tag{8.6}$$

Knowing

$$\sin A \cdot \sin B = \tfrac{1}{2}(\cos [B - A] + \cos [A + B]) \tag{8.7}$$

we get

$$S_{IQ}(t) \cdot \sin 2\pi f_c \cdot t = \underbrace{\frac{A_Q(f)}{2}}_{\text{Desired signal}} + \underbrace{\frac{A_Q}{2} \cdot \cos 2\pi 2 f_c \cdot t + \frac{A_I}{2} \cdot \sin 2\pi 2 f_c \cdot t}_{\text{Remove by passing through a lowpass filter}} \tag{8.8}$$

We'll use these results later in the chapter in Sec. 8.2.4.

8.1 Continuous-Time Bandpass Noise-Shaping

When we developed the (lowpass) passive noise-shaping modulator back in Sec. 6.1 we used a capacitor to sum (sigma) the difference (delta) between the input and the fed back signals. The result was an absence of noise in the modulator's output signal, Fig. 6.5, at DC where the impedance of the capacitor is infinite. In order to implement a bandpass modulator let's replace the capacitor in Fig. 6.4 with an LC tank circuit, Fig. 3.39. Following the same reasoning, the output of our bandpass modulator should have no noise at the resonant frequency of the tank where its impedance is infinite, $f_0 = 1/2\pi\sqrt{LC}$.

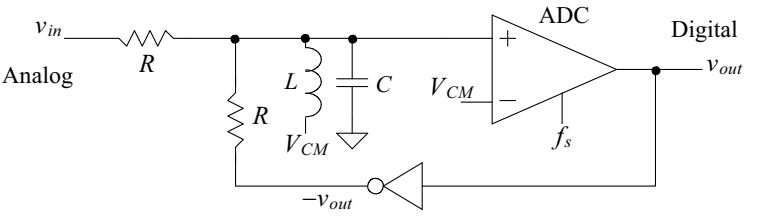
8.1.1 Passive-Component Bandpass Modulators

Figure 8.2a shows the implementation of a passive-component bandpass noise-shaping modulator using this approach. To determine the transfer function of this topology let's use Fig. 8.2b. We can write, following what we did in Sec. 6.1 for the lowpass topologies,

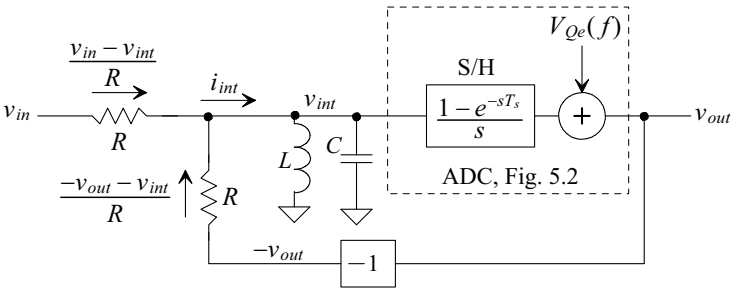
$$\left[\left(\frac{v_{in}-v_{int}}{R}+\frac{-v_{out}-v_{int}}{R}\right)\cdot\frac{sL}{1+s^2LC}\right]\cdot\frac{1-e^{-sT_s}}{s}+V_{Qe}(f)=v_{out} \qquad (8.9)$$

and

$$\left(v_{in}\cdot\frac{sL}{R}-v_{int}\cdot 2\frac{sL}{R}-v_{out}\cdot\frac{sL}{R}\right)\cdot\overbrace{\left(\frac{1-e^{-sT_s}}{s}\right)}^{SH(s)}+V_{Qe}(f)\cdot(1+s^2LC)=v_{out}\cdot(1+s^2LC) \qquad (8.10)$$



(a) Circuit implementation of a bandpass modulator.



(b) Block diagram

Figure 8.2 A bandpass passive NS modulator.

$$v_{out} = v_{in} \cdot \frac{s\frac{L}{R} \cdot SH(s)}{1 + s\frac{L}{R}SH(s) + s^2LC} + V_{Qe}(f) \cdot \frac{1 + s^2LC}{1 + s\frac{L}{R}SH(s) + s^2LC} - v_{int} \cdot \frac{2s\frac{L}{R} \cdot SH(s)}{1 + s\frac{L}{R}SH(s) + s^2LC} \tag{8.11}$$

and finally (see Fig. 3.39 and then Eq. [6.12] for the analogy with the lowpass passive modulator) neglecting the effects of the S/H (what happens at f_0?) we get

$$v_{out} = \overbrace{\frac{s\frac{1}{RC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}}}^{STF(f)} \cdot v_{in} + \overbrace{\frac{s^2 + \frac{1}{LC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}}}^{NTF(f)} \cdot V_{Qe}(f) + \underbrace{\frac{-2v_{int} \cdot s\frac{1}{RC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}C}}_{\text{Extra noise/distortion term}} \tag{8.12}$$

The *STF* shows a bandpass response while the *NTF* shows a band reject response, Fig. 8.3. Like the lowpass modulator we have the extra noise/distortion term that causes the modulator to deviate from the ideal behavior. We know, at this point, that we can drive v_{int} to zero by using an active element (amplifier). This is discussed in the next section.

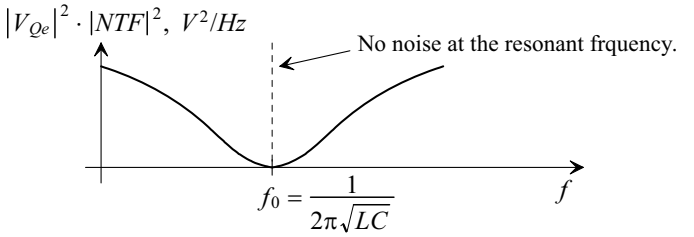


Figure 8.3 Modulation noise spectral density for a bandpass modulator.

Example 8.1
Simulate the operation of the NS modulator seen in Fig. 8.2 when R is 1k, C is 10 pF, L is 4.06 μH, and the clocking frequency is 100 MHz. Comment on the resulting simulation results and the operation/limitations of the circuit.

The conversion is centered around, from Fig. 8.3, 25 MHz. What this means is if our input signal is a sinewave at 25 MHz we should be able recover an exact replica of this input after removing the modulation noise. If a DC signal is applied to the modulator we should get out no signal (actually the modulator should output a sequence, like 101010101 that averages to V_{CM} or, for a mixed-signal system, no signal).

Figure 8.4 shows the simulation results. Note the ripple in the output, after filtering, amplitude. This variation can be removed by more filtering (increasing the Q of the simple filter used in the simulation by increasing the resistor) to remove noise. It should be noted that an ideal comparator was used in this simulation. As mentioned on page 207 a practical concern in a CT modulator is the effects of varying comparator delay which result in *amplitude modulation* in the output. Finally, Fig. 8.5 shows the spectrum of the modulator's output when a 25 MHz input tone is applied. Again, as in the passive noise-shaping lowpass topology, the extra, unwanted, term in Eq. (8.12) limits the *SNR*. ■

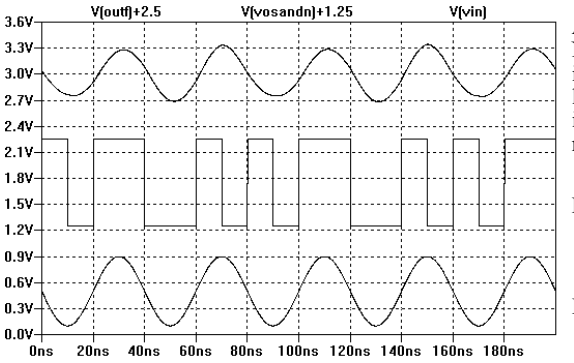


Figure 8.4 Simulation results for the modulator discussed in Ex. 8.1.

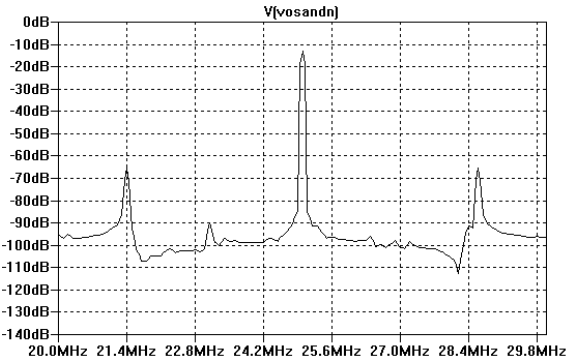


Figure 8.5 Spectrum of the modulator's output in Ex. 8.1.

An Important Note

Notice that the value of the inductor we used in Ex. 8.1 is too big to be integrated with the modulator. If one understands the concepts in this section we see that the *LC* tank can be replaced with an active circuit, like a g_m-*C* filter, that has a high-impedance over a range of frequencies (the range we want to convert from an analog representation to a digital representation).

8.1.2 Active-Component Bandpass Modulators

To remove the extra noise/distortion term in Eq. (8.12) we can use, as we did back in Sec. 6.2.4, an active circuit. Figure 8.6 shows one such implementation. Noting that the variation in v_{int} is zero when the op-amp's gain is infinite we can rewrite Eq. (8.12) for this topology as

$$v_{out} = \overbrace{\frac{s\frac{1}{RC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}}}^{STF(f)} \cdot v_{in} + \overbrace{\frac{s^2 + \frac{1}{LC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}}}^{NTF(f)} \cdot V_{Qe}(f) \qquad (8.13)$$

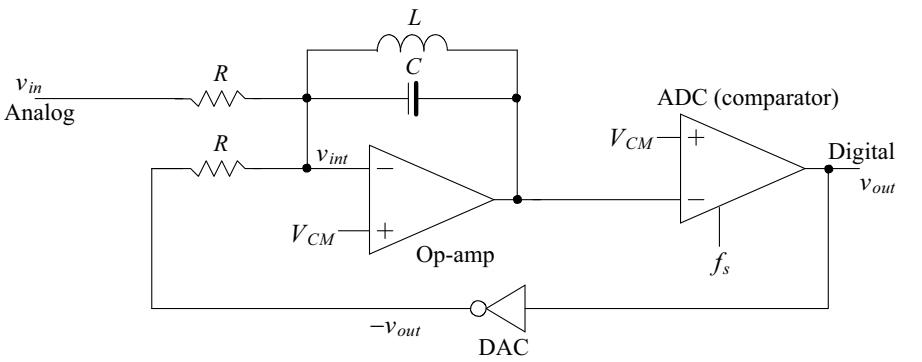


Figure 8.6 An active-integrator bandpass NS modulator.

Simulations demonstrating the operation of this topology are found at CMOSedu.com.

Signal-to-Noise Ratio

The output of the bandpass modulator can be passed through a bandpass filter, Sec. 4.2.3, with a bandwidth 2*B* to remove the modulation noise, Fig. 8.7. The smaller *B*, the lower the noise in the final digital output word and the larger the *SNR*. Again, the trade-off with using smaller filter bandwidth is that the allowable input signal frequency range shrinks.

Let's use the results in Sec. 6.1.1 (or Sec. 7.1.2) to help with our *SNR* estimate here. When we compare Fig. 6.8 (which doesn't show the noise power contributed from the negative components of the frequency spectrum) to Fig. 8.7, we see exactly the same shape (note that for large *Q*, as used in Ex. 8.1, this isn't true). Therefore we can use the equations derived earlier for the lowpass modulators to estimate the *SNR* in the bandpass topologies. Notice that if f_0 is 25 MHz and B is 100 kHz then the oversampling ratio, *K*, is 125.

Notice that the bandpass modulator seen in Fig. 8.6 has a second-order response, two poles in the *NTF*, so it's called a *second-order bandpass modulator* (even though its *SNR* is similar to a first-order lowpass response). A *fourth-order bandpass modulato*r, Fig. 8.8 (again see simulations at CMOSedu.com), has behavior (an *SNR)* similar to the second-order noise shaping topology discussed in Secs. 6.2.4 and 7.2.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$B = \frac{f_s}{2K}$$

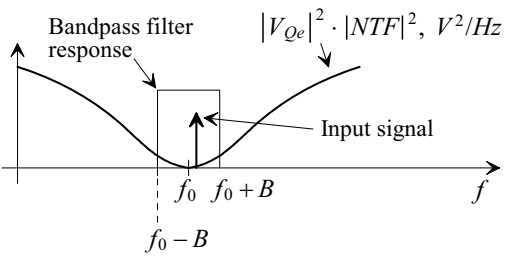


Figure 8.7 Filtering out modulation noise to calculate SNR.

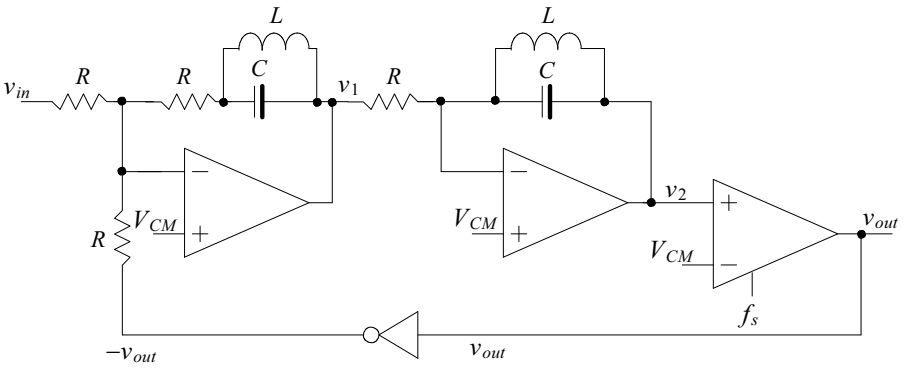


Figure 8.8 Fourth-order bandpass noise-shaping modulator.

8.1.3 Modulators for Conversion at Radio Frequencies

One area, at the time of this writing, that still has substantial room for development is the use of bandpass data converters for wireless (narrowband or radio frequency [RF]) communications. Currently mixing (down converting the transmitted information centered around some carrier frequency) into an intermediate frequency (or to baseband) is performed using a multiplier. A multiplier is an analog circuit (e.g., a Gilbert multiplier) with both continuous-time inputs and output. By using a bandpass converter for mixing we can go directly to digital format (the bandpass converter's input is analog, its output is digital, and it is clocked with a local oscillator). *The key to a successful* modulator design at high operating frequencies is minimizing the delay in both the forward and feedback paths of the converter (to ensure a stable converter). Thus the topology seen in Fig. 8.2 is more likely to be successful at the high conversion rates required in an RF circuit than the topologies seen in Figs. 8.6 and 8.8.

Figure 8.9 shows a topology built from the concepts used in the simple passive modulator in Fig. 8.2. The low-noise amplifier (LNA) isn't part of the modulator and is used to provide gain and isolation for the RF input signal (the noise performance of the receiver is dominated by the performance of this first stage). The output of the LNA is a current, $g_m v_{in}$ (this is the input to the modulator). A portion of the current fed back, I_{FB}, must, on average, equal this input current. The output of the modulator, even though a digital voltage value, can be thought of as the current fed back, i_{out}, to the resonator (which is equal, on average, to $N \cdot I_{FB}$ where N is the number of times the comparator output goes low). Deriving the *STF* and *NTF*, similar to Eq. (8.12) (but with an input current, $i_{in} = g_m v_{in}$, output current, i_{out}, and quantization noise current, $I_{Qe}(f)$) would show that we don't get an extra noise/distortion term. Note that increases in the *SNR* must employ *K*-path sampling, Fig. 6.24, rather than topologies that result in an increase in the modulator's forward delay. The use of *K*-path sampling is also required to ensure that an adequate oversampling ratio can be achieved when the carrier frequency is large. In addition, it's used to ensure the inherent lowpass filtering we get (the path filter seen in Fig. 6.24) when combining the comparator's outputs doesn't affect the desired signal (of course we can combine the comparator outputs so that they have a bandpass response, as discussed in Sec. 4.2.3, rather than a lowpass Sinc response). We leave the detailed implementations of these topologies to the refereed literature.

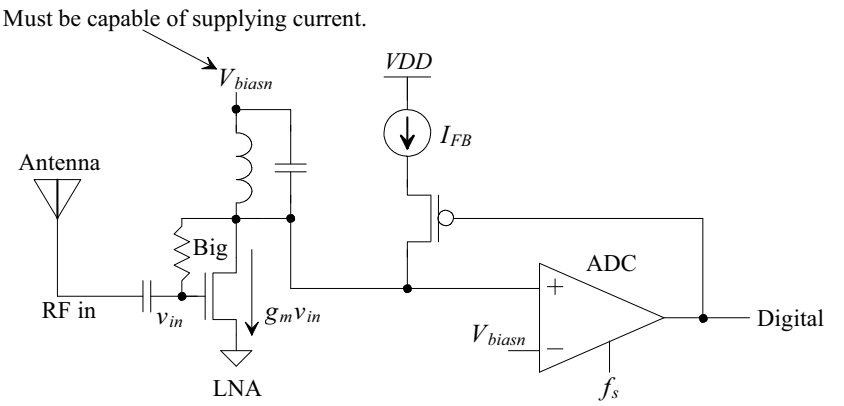


Figure 8.9 Design of a bandpass modulator for data conversion at RF.

8.2 Switched-Capacitor Bandpass Noise-Shaping

In Sec. 4.2.3 we discussed the idea that we can implement a Sinc-shaped averaging bandpass filter centered around $f_s/4$ (or $f_s/6$) having a transfer function, Eq. (4.25), of

$$H(z) = \frac{1 - z^{-K}}{1 + z^{-2}} \tag{8.14}$$

Comparing this equation to the equation for the equivalent lowpass averaging filter, Eq. (4.10), we see that transforming our lowpass modulator topologies into bandpass modulator topologies with bandpass responses centered at $f_s/4$ can be accomplished by

$$\text{Substituting } z^{-2} \text{ for } -z^{-1} \tag{8.15}$$

The discrete-analog integrator (DAI) discussed in Sec. 2.2.3 is the basic building block used in lowpass, switched-capacitor, modulator implementations. In order to implement a bandpass modulator at $f_s/4$ we need to replace the DAI used in the lowpass topologies with an $f_s/4$ resonator, an analog implementation of Fig. 4.23, or

$$\text{Replace } \frac{1}{1 - z^{-1}} \text{ with } \frac{1}{1 + z^{-2}} \tag{8.16}$$

or, when we can't avoid a delay in the implementation of the building block,

$$\text{Replace } \frac{z^{-1}}{1 - z^{-1}} \text{ with } \frac{z^{-1}}{1 + z^{-2}} \tag{8.17}$$

8.2.1 Switched-Capacitor Resonators

In order to move towards implementing a switched-capacitor $f_s/4$ resonator, consider the circuit in Fig. 8.10. The top portion of the circuit is simply the DAI discussed in Sec. 2.2.3 (Fig. 2.54). The bottom portion provides the positive feedback needed for the addition (instead of subtraction) of the delayed output. The transfer function of this circuit is

$$v_{out}(z) = \frac{v_1(z) \cdot z^{-1/2} - v_2(z)}{1 + z^{-1}} \cdot \frac{C_I}{C_F} \tag{8.18}$$

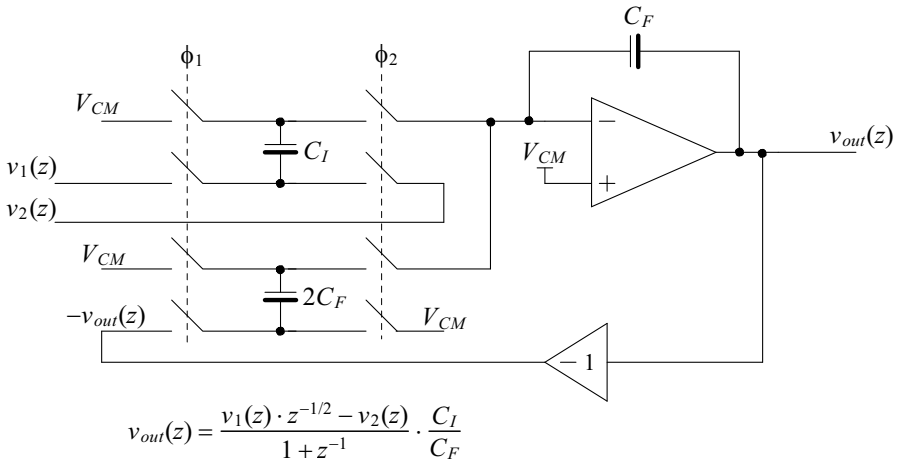


Figure 8.10 Implementing an $f_s/2$ resonator for use in a bandpass modulator.

or an $f_s/2$ resonator (the pole is located at $f_s/2$). In order to implement an $f_s/4$ resonator we'll need to use two delays in the feedback path. Implementing two (analog) delays, with any reasonable level of precision, in the feedback path is challenging.

In order to implement an $f_s/4$ resonator, we'll take two $f_s/2$ resonators, put them in parallel (see Eq. [2.56] in the *K*-path sampling discussion found in Sec. 2.1.6), and switch the phases of the clocks in each topology. So, for example, if we clock two of the resonators in Fig. 8.10 connected in parallel (see Fig. 2.37) at 50 MHz then the output word rate is 100 MHz (the output of the topology changes each time either ϕ_1 or ϕ_2 goes high). Reviewing Eq. (2.56) for two paths, $z \rightarrow z^2$, we can then re-write Eq. (8.18) as

$$v_{out}(z) = \frac{v_1(z) \cdot z^{-1} - v_2(z)}{1 + z^{-2}} \cdot \frac{C_I}{C_F} \tag{8.19}$$

or our desired $f_s/4$ resonator transfer function. Note that in this equation the v_1 input is delayed by a full clock cycle (see Fig. 2.55 to see how this is modeled for the DAI). We'll see that this delay means that we can't design a two stage bandpass modulator (a fourth-order modulator) using two non-delaying resonators. This shouldn't be a surprise since we also couldn't design a second-order lowpass modulator, Fig. 7.27c, with two non-delaying DAIs.

Example 8.2

Simulate the operation of the resonator in Fig. 8.10, clocked at 50 MHz, if $C_I = C_F = 1\ pF$. Comment on the stability of the resonator. Verify your comments using a SPICE simulation.

The pole of the resonator is located at $z = -1$, right on the unit circle (located at a frequency of $f_s/2$). We know, from Sec. 4.3.1, that for a discrete-time circuit to be stable its poles must lie inside the unit circle. We, therefore, expect the resonator to oscillate (become unstable), Fig. 8.11. ■

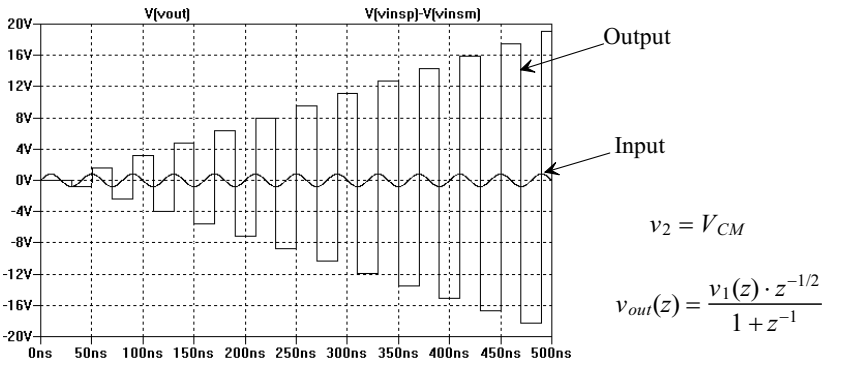


Figure 8.11 Simulating the operation of the resonator in Fig. 8.10.

Example 8.3

Suggest a modification to the resonator in Fig. 8.10 to eliminate the need for the gain of −1 block. Verify your circuit modification with SPICE.

Reviewing Fig. 2.56 we see that if we connect the fed back output signal to the top plate of the $2C_F$ capacitor, Fig. 8.12, then the signal is inverted when it's transferred to the output of the resonator. Simulation files for this circuit verifying correct operation are available at CMOSedu.com. Note that we'll use the topology seen in Fig. 8.10 since it is more tolerant of charge injection errors on the $2C_F$ capacitor than the topology seen in Fig. 8.12. ■

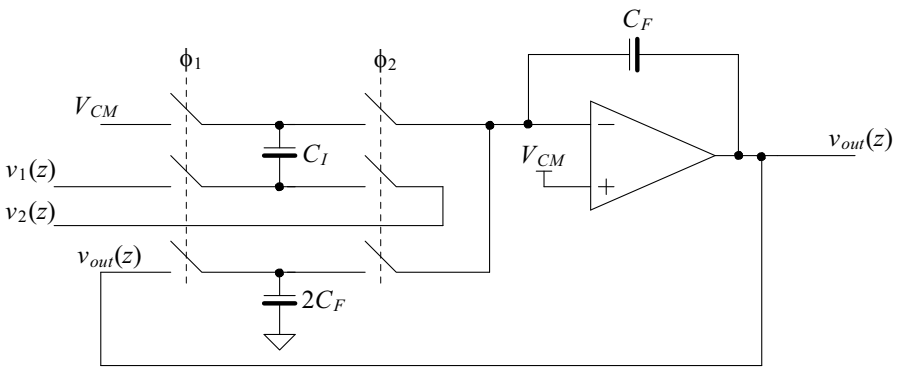


Figure 8.12 Implementing a resonator for use in a bandpass modulator.

8.2.2 Second-Order Modulators

Figure 8.13 shows the implementation of a second-order modulator based on the first-order lowpass topology seen in Fig. 7.1. Remembering, from page 290, that a second-order bandpass modulator's *SNR* is similar to (calculated in the same way as) the first-order lowpass modulator's *SNR* we can write

$$v_{out} = V_{Qe}(z) + (v_{in} - v_{out}) \cdot G_1 G_c \cdot \frac{-z^{-2}}{1+z^{-2}} \tag{8.20}$$

or, assuming $G_1 G_c = 1$ (as discussed in Sec. 7.1.5),

$$v_{out} = v_{in} \cdot \overbrace{(-z^{-2})}^{STF} + V_{Qe}(z) \cdot \overbrace{(1+z^{-2})}^{NTF} \tag{8.21}$$

Note the inversion in the signal transfer function. This is trivial to remove; for an analog signal see Fig. 3.6 and, for a digital signal, see Fig. 6.3. The noise transfer function, $1+z^{-2}$, has the shape seen in Fig. 8.7. At $f_s/4$ the modulation noise is zero increasing as we move away from $f_s/4$. Note that this topology is second-order because the number of poles in the *NTF* is two (a first-order lowpass modulator has one pole in its *NTF*).

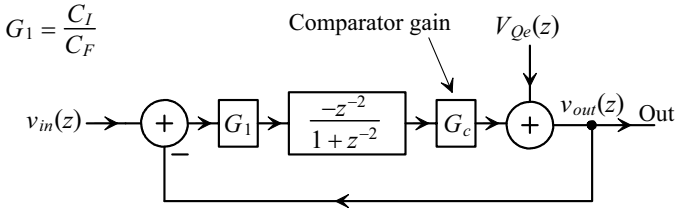


Figure 8.13 Block diagram of a second-order bandpass modulator.

Example 8.4

Simulate the operation of the second-order modulator seen in Fig. 8.13 (show the modulator's output spectrum) with a clocking frequency of 50 MHz (data coming out of the modulator at a rate of 100 MHz because of the 2-paths used) and an input frequency of 25.1 MHz. If the digital output of the modulator is run through an ideal digital bandpass filter with a pass frequency range of 25 $MHz \pm 390\ kHz$ then estimate the final SNR_{ideal}.

Figure 8.14 shows the modulator's output spectrum. Notice how the modulation noise increases as the frequency moves away from $f_s/4$ (25 MHz here). The oversampling ratio, *K*, can be calculated using, once again,

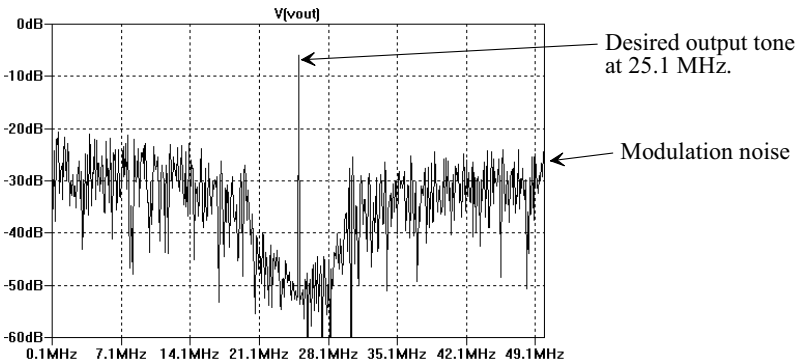


Figure 8.14 Spectrum of the modulator's output discussed in Ex. 8.4.

$$K = \frac{f_s}{2B} \tag{8.22}$$

For the present example f_s = 100 MHz and B = 390 kHz so K = 128. From Eq. (7.14) the SNR_{ideal} is 66 dB. ■

8.2.3 Fourth-Order Modulators

Figure 8.15 shows the block diagram of a fourth-order bandpass modulator formed by transforming the lowpass second-order modulator seen in Fig. 7.26c. Again, the bandpass topology is now called a fourth-order modulator because the number of poles in the *NTF* is four. The transfer function for this, f_s /4, bandpass modulator (sometimes called a *quadrature modulator*) is

$$v_{out}(z) = v_{in}(z)\cdot\overbrace{(-z^{-2})}^{STF} + V_{Qe}(z)\cdot\overbrace{(1+z^{-2})^2}^{NTF} \tag{8.23}$$

Again, as discussed in Sec. 8.1.2, the fourth-order bandpass modulator's *SNR* can be estimated using the same approach that we used for the second-order lowpass modulator discussed in Sec. 7.2.

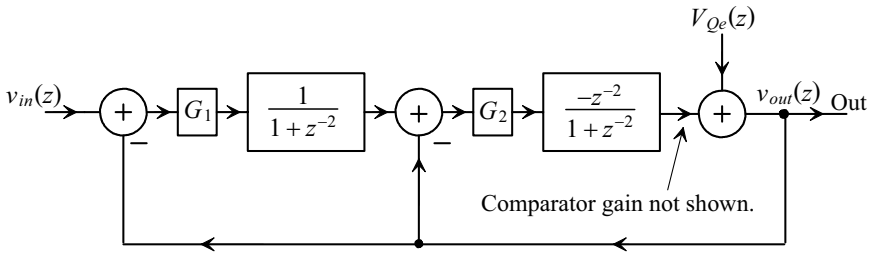


Figure 8.15 A fourth-order bandpass modulator.

Example 8.5

Repeat Ex. 8.4 using the fourth-order topology seen in Fig. 8.15.

Figure 8.16 shows the modulator's output spectrum. The oversampling ratio, K, is again 128 so using Eq. (7.52) the SNR_{ideal} is 100 dB. ■

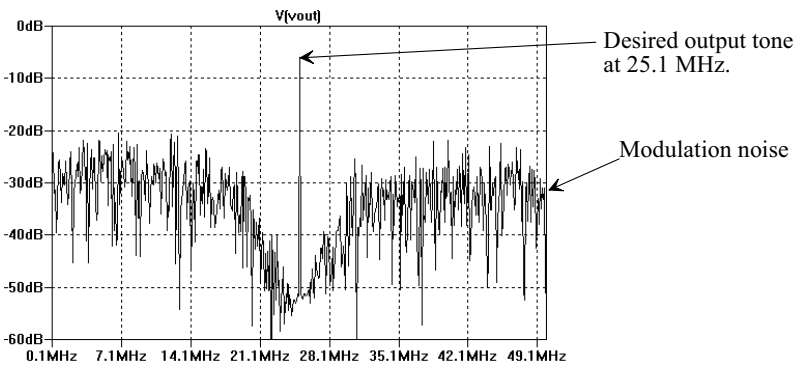


Figure 8.16 Spectrum of the modulator's output discussed in Ex. 8.5.

A Common Error

Back in Fig. 7.39 and the associated text we discussed that adding gratuitous delay to the forward path of the modulator would move it towards instability. Consider using a delaying resonator, Fig. 8.17, for the first stage of the fourth-order modulator. The first stage is made delaying by simply switching the phases of the clock signals used in this circuit. Unfortunately, the added two clock cycle delay in the forward path, for a total of four clock cycles of delay, makes the topology unstable. Simulation examples at CMOSedu.com, for Fig. 8.17, can be used to help show that this modulator *is always unstable*. The output of the modulator oscillates at $f_s/4$ regardless of the input signal.

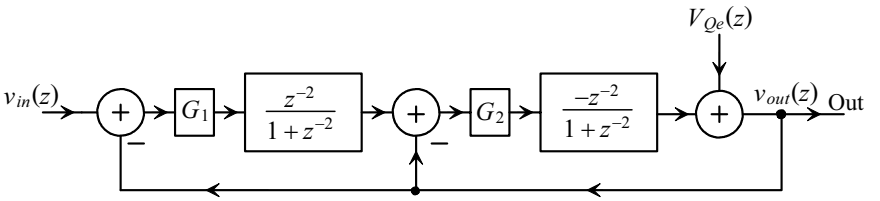


Figure 8.17 A fourth-order bandpass modulator using two delaying resonators (bad).

A Comment about 1/*f Noise*

Notice that in the bandpass modulators we've discussed 1/*f* noise isn't a concern. The 1/*f* noise doesn't have a significant effect on the signal at $f_s/4$ (assuming $f_s/4$ is a relatively large frequency). At lower frequencies the digital filter connected to the modulator's output removes both the modulation noise and the 1/*f* noise.

8.2.4 Digital *I/Q* Extraction to Baseband

One of the benefits of digitizing the signal around $f_s/4$ is the ease with which we can extract the *I* and *Q* components in the transmitted signal (see the first few pages of this chapter). The multiplication by the sine and cosine terms, see Eqs (8.2) and (8.6), used to recover the original signals simplifies to multiplying by either +1, −1, or 0, Fig. 8.18. Extracting the *I/Q* components digitally eliminates the *I* and *Q* channel phase response mismatch (difference in delay through each path) encountered in typical baseband demodulators. Figure 8.19 shows the simulation results showing how the 100 kHz (offset from 25 MHz) signal seen in Fig. 8.16 is demodulated to baseband. Note that the input in the simulation is simply a 25.1 MHz sinewave, not an *I/Q* generated signal (see simulation example at CMOSedu.com using an *I/Q* signal).

After looking at Fig. 8.18 we might wonder how we multiply the modulator output, a 1-bit word, by 1, 0, and −1. As seen in Fig. 6.3, a 1 coming out of the modulator corresponds to 01 (+1) in two's complement while a 0 corresponds to 11 (−1). Multiplying these outputs by 0 results in an output of 00 (0) in two's complement. Multiplication by +1 or −1 results in 01 × (+1) = 01, 01 × (−1) = 11, 11 × (+1) = 11, and 11 × (−1) = 01. A data selector and a multiplexer with some logic for output selection can be used to implement the multiplier (see the simulation example used to generate Fig. 8.19 at CMOSedu.com for one example).

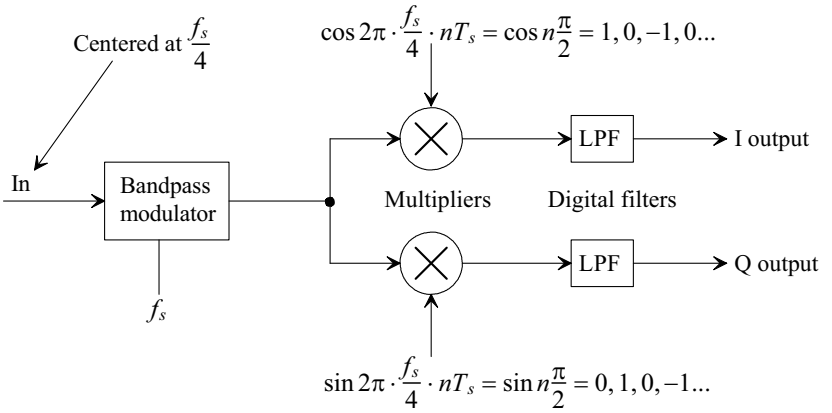


Figure 8.18 Digital I/Q demodulation.

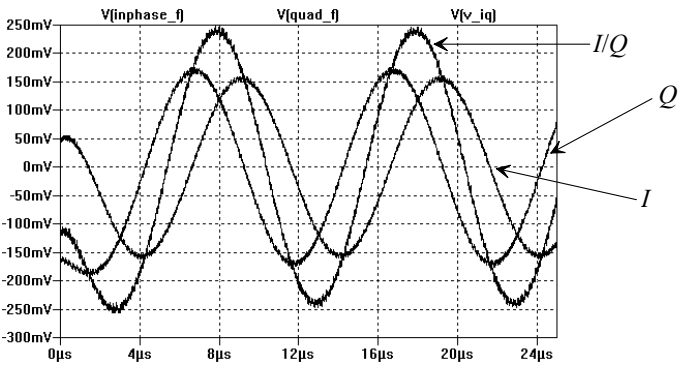


Figure 8.19 Showing how I and Q components of a signal can be extracted digitally.

ADDITIONAL READING

[1] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, Wiley-IEEE Press, 2005. ISBN 978-0471465850

[2] A. I. Hussein and W.B. Kuhn, "Bandpass ΣΔ Modulator Employing Undersampling of RF Signals for Wireless Communication," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 47, No. 7, pp. 614 - 620, July 2000

[3] A. Jayaraman, P.F. Chen, G. Hanington, L. Larson, and P. Asbeck, "Linear High-Efficiency Microwave Power Amplifiers using Bandpass Delta-Sigma Modulators," *IEEE Microwave and Guided Wave Letters*, Vol. 8, No. 3, pp. 121 - 123 March 1998

[4] A. K. Ong and B. A. Wooley, "A Two-Path Bandpass SD Modulator for Digital IF Extraction at 20 MHz," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, pp. 1920-1934, December 1997

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[6] B.-S. Song, "A 4th-Order Bandpass ΔΣ Modulator with Reduced Number of Op-Amps," *IEEE Solid-State Circuits Conference*, pp. 204-205, 367, February 1995

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[8] D. B. Ribner, "Multistage Bandpass Delta Sigma Modulators," *IEEE Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 41, No. 6, pp. 402 - 405, June 1994

[9] S.A. Jantzi, W.M. Snelgrove, and P.F. Ferguson Jr., "A Fourth-Order Bandpass Sigma-Delta Modulator," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 3, pp. 282 - 291, March 1993

[10] J. C. Candy and G. C. Temes (eds.), *Oversampling Delta-Sigma Data Converters*, Wiley-IEEE Press, 1992. ISBN 978-0879422851

QUESTIONS

8.1 Show, using SPICE, how to adjust the phase and amplitude of the *I* and *Q* signals discussed in the beginning of the chapter to modulate the amplitude and phase of the resulting *I*/*Q* to construct a constellation diagram for 8-level rectangular *QAM*.

8.2 Suggest a topology for the bandpass passive-integrator NS modulator where the input and fed back signals are currents. Derive a transfer function for your design. Does your topology have the extra noise/distortion term seen in Eq. (8.12)? Why or why not? Simulate the operation of your design.

8.3 Show the details of deriving the transfer function for the modulator in Fig. 8.6.

8.4 Repeat question 8.3 for the modulator seen in Fig. 8.8.

8.5 Derive the transfer function for the modulator seen in Fig. 8.9.

8.6 Sketch the implementation of a modulator, based on the topology seen in Fig. 8.9, but using a multi-bit quantizer and feedback DAC.

8.7 Show the details of how Eq. (8.18) is derived.

8.8 Derive the transfer function of the modulator seen in Fig. 8.12.

8.9 Using the modulator topology in Ex. 8.4, show that if we apply a 25 MHz input sinusoid to the modulator we can recover this input signal by passing the output digital data through a bandpass filter with a very small bandwidth (show that the input and output signal amplitudes are equal).

8.10 Derive the transfer function of the topology seen in Fig. 8.17. Verify that the topology is unstable by determining the location of the topology's poles.

8.11 Using a bandpass modulator and digital demodulation (sketch the schematic of your design) show how to recover a 10 kHz sinewave that is amplitude modulated with a carrier frequency of 1 MHz. Use SPICE to verify the operation of your design.